SBAS230B – AUGUST 2002 – REVISED OCTOBER 2002

Dual, 500kSPS, 16-Bit, 2 + 2 Channel, Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 2 SIMULTANEOUS 16-BIT DACs
- 4 FULLY DIFFERENTIAL INPUT CHANNELS
- 2µs THROUGHPUT PER CHANNEL
- 4µs TOTAL THROUGHPUT FOR FOUR CHANNELS
- LOW POWER: 150mW
- INTERNAL REFERENCE
- FLEXIBLE SERIAL INTERFACE
- 16-BIT UPGRADE TO THE 12-BIT ADS7861
- PIN COMPATIBLE WITH THE ADS7861

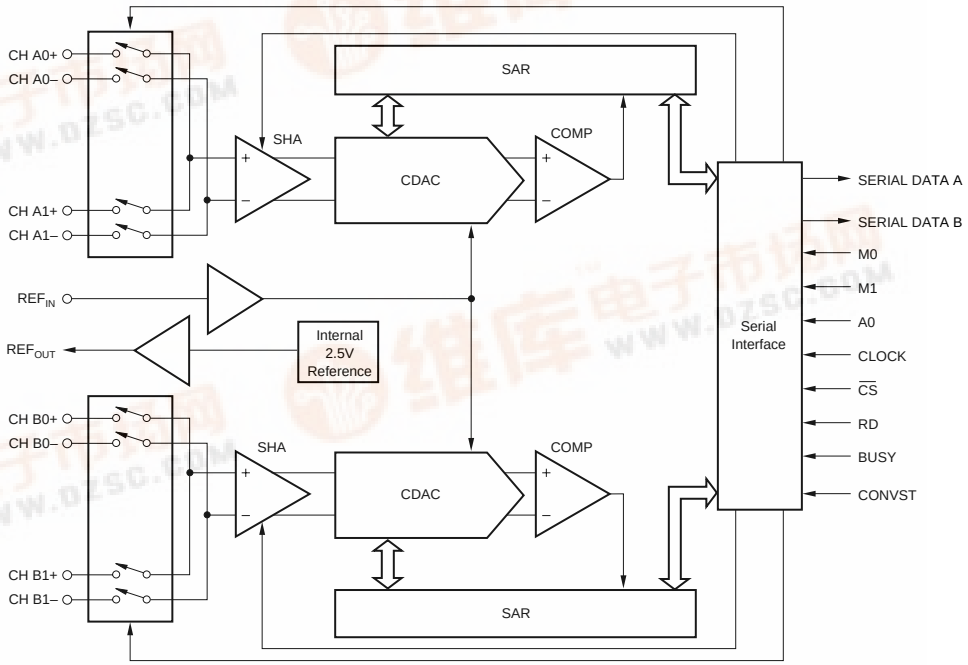
APPLICATIONS

- MOTOR CONTROL
- MULTI-AXIS POSITIONING SYSTEMS
- 3-PHASE POWER CONTROL

DESCRIPTION

The ADS8361 is a dual, 16-bit, 500kSPS, Analog-to-Digital (A/D) converter with four fully differential input channels grouped into two pairs for high-speed, simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differentially to the input of the A/D converter. This provides excellent common-mode rejection of 80dB at 50kHz, which is important in high-noise environments.

The ADS8361 offers a high-speed, dual serial interface and control inputs to minimize software overhead. The output data for each channel is available as a 16-bit word. The ADS8361 is offered in an SSOP-24 package and is fully specified over the –40°C to +85°C operating range.



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings over operating free-air temperature (unless otherwise noted)[1].

Supply Voltage, AGND to AV_{DD}	–0.3V to 7V
Supply Voltage, BGND to BV_{DD}	–0.3V to 7V
Analog Input Voltage	AGND – 0.3V to AV_{DD} + 0.3V
Reference Input Voltage	AGND – 0.3V to AV_{DD} + 0.3V
Digital Input Voltage	BGND – 0.3V to BV_{DD} + 0.3V
Ground Voltage Differences, AGND to BGND	±0.3V
Voltage Differences, BV_{DD} to AGND	–0.3V to 7V
Input Current to Any Pin Except Supply	–20mA to 20mA
Power Dissipation	See Dissipation Rating Table
Operating Virtual Junction Temperature Range, T_J	–40°C to 150°C
Operating Free-Air Temperature Range, T_A	–40°C to 85°C
Storage Temperature Range, T_{STG}	–65°C to 150°C
Lead Temperature 1.6mm (1/16 inch) from Case for 10s	260°C

NOTE: (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions of extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8361	±8	14	SSOP-24	DBQ	–40°C to +85°C	ADS8361IDBQ	Rails, 56
"	"	"	"	"	"	ADS8361IDBQR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

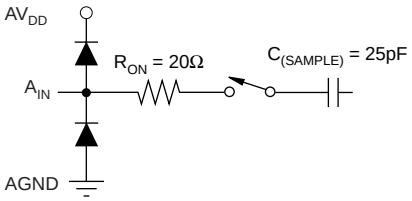
RECOMMENDED OPERATING CONDITIONS

	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Voltage, AGND to AV_{DD}		4.75	5	5.25	V
Supply Voltage, BGND to BV_{DD}	Low-Voltage Levels	2.7		3.6	V
	5V Logic Levels	4.5	5	5.5	V
Reference Input Voltage		1.2	2.5	2.6	V
Operating Common-Mode Signal	–IN	2.2	2.5	2.8	V
Analog Inputs	+IN – (–IN)	0		$\pm V_{REF}$	V
Operating Junction Temperature Range T_J		–40		105	°C

PACKAGE DISSIPATION RATING

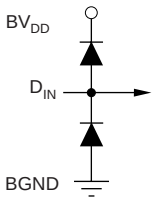
PACKAGE	$R\theta_{JC}$	$R\theta_{JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \leq 25°C$ POWER RATING	$T_A \leq 70°C$ POWER RATINGQ	T_A = 85°C POWER RATING
DBQ	28.5°C/W	88°C/W	11.364.mW/°C	1420mW	909mW	738mW

EQUIVALENT INPUT CIRCUIT



Diode Turn on Voltage: 0.35V

Equivalent Analog Input Circuit



Equivalent Digital Input Circuit

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at –40°C to 85°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 10MHz, and f_{SAMPLE} = 500 kSPS, unless otherwise noted.

PARAMETER	CONDITIONS	ADS8361 MIN	ADS8361 TYP[1]	ADS8361 MAX	UNITS
ANALOG INPUT					
Full-Scale Range[2] (FSR)	+IN – (–IN)			$\pm V_{REF}$	V
Operating Common-Mode Signal		2.2		2.8	V
Input Switch Resistance	–IN = V_{REF}		20		Ω
Input Capacitance	–IN = V_{REF}		25		pF
Input Leakage Current	–IN = V_{REF}		±1		nA
Differential Input Switch Resistance			40		Ω
Differential Input Capacitance			15		pF
Common-Mode Rejection Ratio (CMRR)	At DC		84		dB
	V_{IN} = ±1.25Vp-p at 50kHz		80		dB
DC ACCURACY					
Resolution		16			Bits
No Missing Code (NMC)		14			Bits
Integral Linearity Error (INL)			±3	±8	LSB[3]
Integral Linearity Match	Channel 0/1, Same A/D		4		LSB
Differential Nonlinearity (DNL)			+1.5[4]		LSB
Bipolar Offset Error (V_{OS})			±0.5	±2	mV
Bipolar Offset Error Match	Channel 0/1, Same A/D		0.5	1	mV
Bipolar Offset Error Drift (TCV_{OS})			0.4		ppm/°C
Gain Error[6] (G_{ERR})			±0.05	±0.5	%
Gain Error Match			0.05	0.15	%
Gain Error Drift (TCG_{ERR})			20		ppm/°C
Noise			60		µVrms
Power-Supply Rejection Ratio (PSRR)	4.75V < AV_{DD} < 5.25V, with External Reference, at DC		–70		dB
SAMPLING DYNAMICS					
Conversion Time per A/D (t_{CONV})	100kHz ≤ f_{CLK} ≤ 10MHz	1.6		160	µs
Acquisition Time (t_{AQ})	f_{CLK} = 10MHz	400			ns
Throughout Rate				500	kSPS
Aperture Delay				5	ns
Aperture Delay Matching			100		ps
Aperture Jitter			50		ps
Clock Frequency		0.1		10	MHz
AC ACCURACY					
Total Harmonic Distortion (THD)	V_{IN} = ±2.5Vp-p at 10kHz		–94		dB
Spurious-Free Dynamic Range (SFDR)	V_{IN} = ±2.5Vp-p at 10kHz		94		dB
Signal-to-Noise Ratio (SNR)	V_{IN} = ±2.5Vp-p at 10kHz		83		dB
Signal-to-Noise + Distortion (SINAD)	V_{IN} = ±2.5Vp-p at 10kHz		83		dB
Channel-to-Channel Isolation	V_{IN} = ±2.5Vp-p at 10kHz		96		dB
VOLTAGE REFERENCE OUTPUT					
Reference Voltage Ouput (V_{OUT})		2.475	2.5	2.525	V
Initial Accuracy				±1	%
Output Voltage Temperature Drift (dV_{OUT}/dT)			±20		ppm/°C
Output Voltage Noise	f = 0.1Hz to 10Hz, C_L = 10µF		10		µVp-p
	f = 10Hz to 10kHz, C_L = 10µF		12		µVrms
Power-Supply Rejection Ratio (PSRR)			60		dB
Output Current (I_{OUT})			10		µA
Short-Circuit Current (I_{SC})			0.5		mA
Turn On Settling Time	to 0.1% at C_L = 0		100		µs
VOLTAGE REFERENCE INPUT					
Reference Voltage Input (V_{IN})		1.2	2.5	2.6	V
Reference Input Resistance		100			MΩ
Reference Input Capacitance			5		pF
Reference Input Current				1	µA

NOTES: (1) All Values are at T_A = 25°C. (2) Ideal input span; does not include gain or offset error. (3) LSB means Least Significant Bit, with V_{REF} equal to +2.5V; 1LSB = 76µV. (4) Specified for 14-bit no missing code. (5) Specified for 15-bit no missing code. (6) Measured relative to an ideal, full-scale input (+IN – (–IN)) of 4.9999V. Thus, gain error does not include the error of the internal voltage reference.

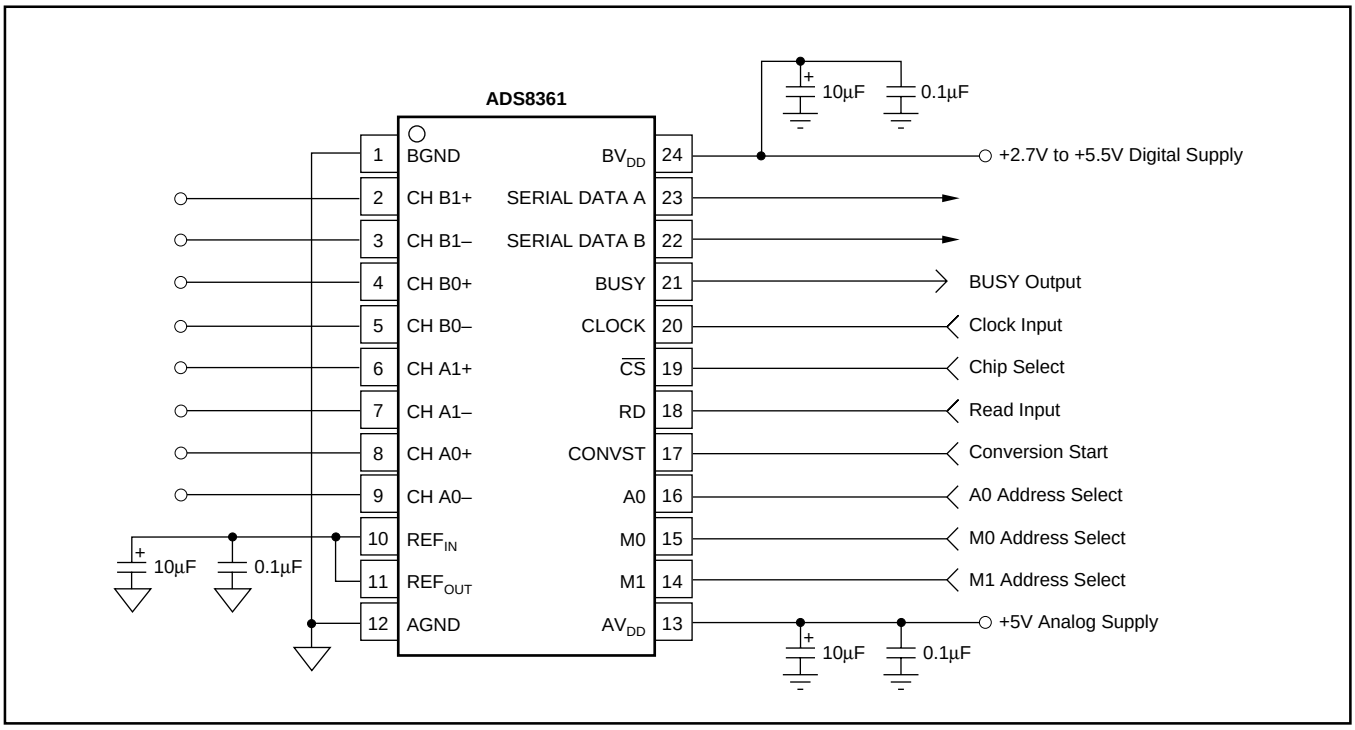
ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at –40°C to 85°C, AV_{DD} = 5V, V_{REF} = internal +2.5V, f_{CLK} = 10MHz, and f_{SAMPLE} = 500 kSPS, unless otherwise noted.

PARAMETER	CONDITIONS	ADS8361 MIN	ADS8361 TYP[1]	ADS8361 MAX	UNITS
DIGITAL INPUTS[2]					
Logic Family			CMOS		
High-Level Input Voltage (V_{IH})		0.7 • V_{DD}		V_{DD} + 0.3	V
Low-Level Input Voltage (V_{IL})		–0.3		0.3 • V_{DD}	V
Input Current (I_{IN})	V_I = BV_{DD} or BGND			±50	nA
Input Capacitance (C_I)			5		pF
DIGITAL OUTPUTS[2]					
Logic Family			CMOS		
High-Level Output Voltage (V_{OH})	BV_{DD} = 4.5V, I_{OH} = –100µA	4.44			V
Low-Level Output Voltage (V_{OL})	BV_{DD} = 4.5V, I_{OH} = –100µA			0.5	V
High-Impedance-State Output Current (I_{OZ})	$\overline{CS}$ = BV_{DD}, V_I = BV_{DD} or BGND			±50	nA
Output Capacitance (C_O)			5		pF
Load Capacitance (C_L)				30	pF
Data Format			Binary Two's Complement		pF
DIGITAL INPUTS[3]					
Logic Family			LVCMOS		
High-Level Input Voltage (V_{IH})	BV_{DD} = 3.6V	2		V_{DD} + 0.3	V
Low-Level Input Voltage (V_{IL})	BV_{DD} = 2.7V	–0.3		0.8	V
Input Current (I_{IN})	V_I = BV_{DD} or BGND			±50	nA
Input Capacitance (C_I)			5		pF
DIGITAL OUTPUTS[3]					
Logic Family			LVCMOS		
High-Level Output Voltage (V_{OH})	BV_{DD} = 2.7V, I_{OH} = –100µA	V_{DD} – 0.2			V
Low-Level Output Voltage (V_{OL})	BV_{DD} = 2.7V, I_{OH} = –100µA			0.2	V
High-Impedance-State Output Current (I_{OZ})	$\overline{CS}$ = BV_{DD}, V_I = BV_{DD} or BGND			±50	nA
Output Capacitance (C_O)			5		pF
Load Capacitance (C_L)				30	pF
Data Format			Binary Two's Complement		pF
POWER SUPPLY					
Analog Supply Voltage (AV_{DD})		4.75		5.25	V
Digital Supply Voltage (BV_{DD})	Low-Voltage Levels	2.7		3.6	V
	5V Logic Levels	4.5		5.5	V
Analog Operating Supply Current (AI_{DD})				35	mA
Digital Operating Supply Current (BI_{DD})	BV_{DD} = 3V			1[4]	µA
	BV_{DD} = 5V			1[4]	µA
Power Dissipation	BV_{DD} = 3V		150	200	mW
	BV_{DD} = 5V		150	200	mW

NOTES: (1) All Values are at T_A = 25°C. (2) Applies for 5.0V nominal supply: BV_{DD} (min) = 4.5V and BV_{DD} (max) = 5.5V. (3) Applies for 3.0V nominal supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V. (4) No clock active (static).

BASIC CIRCUIT CONFIGURATION



TRUTH TABLE

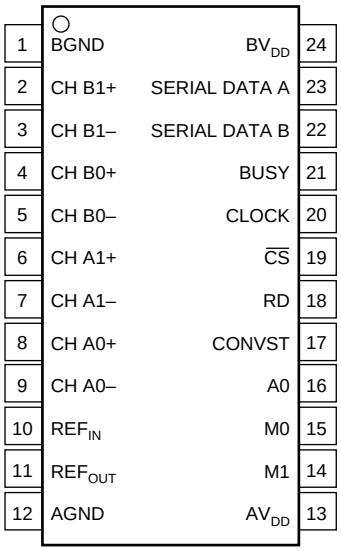
M0	M1	A0	TWO-CHANNEL/FOUR-CHANNEL OPERATION	DATA ON SERIAL OUTPUTS	CHANNELS CONVERTED
0	0	0	Two-Channel	A and B	A0 and B0
0	0	1	Two-Channel	A and B	A1 and B1
0	1	0	Two-Channel	A Only	A0 and B0
0	1	1	Two-Channel	A Only	A1 and B1
1	0	X	Four-Channel	A and B	Sequential
1	1	X	Four-Channel	A Only	Sequential

NOTE: X = Don't Care.

PIN CONFIGURATION

Top View **SSOP**

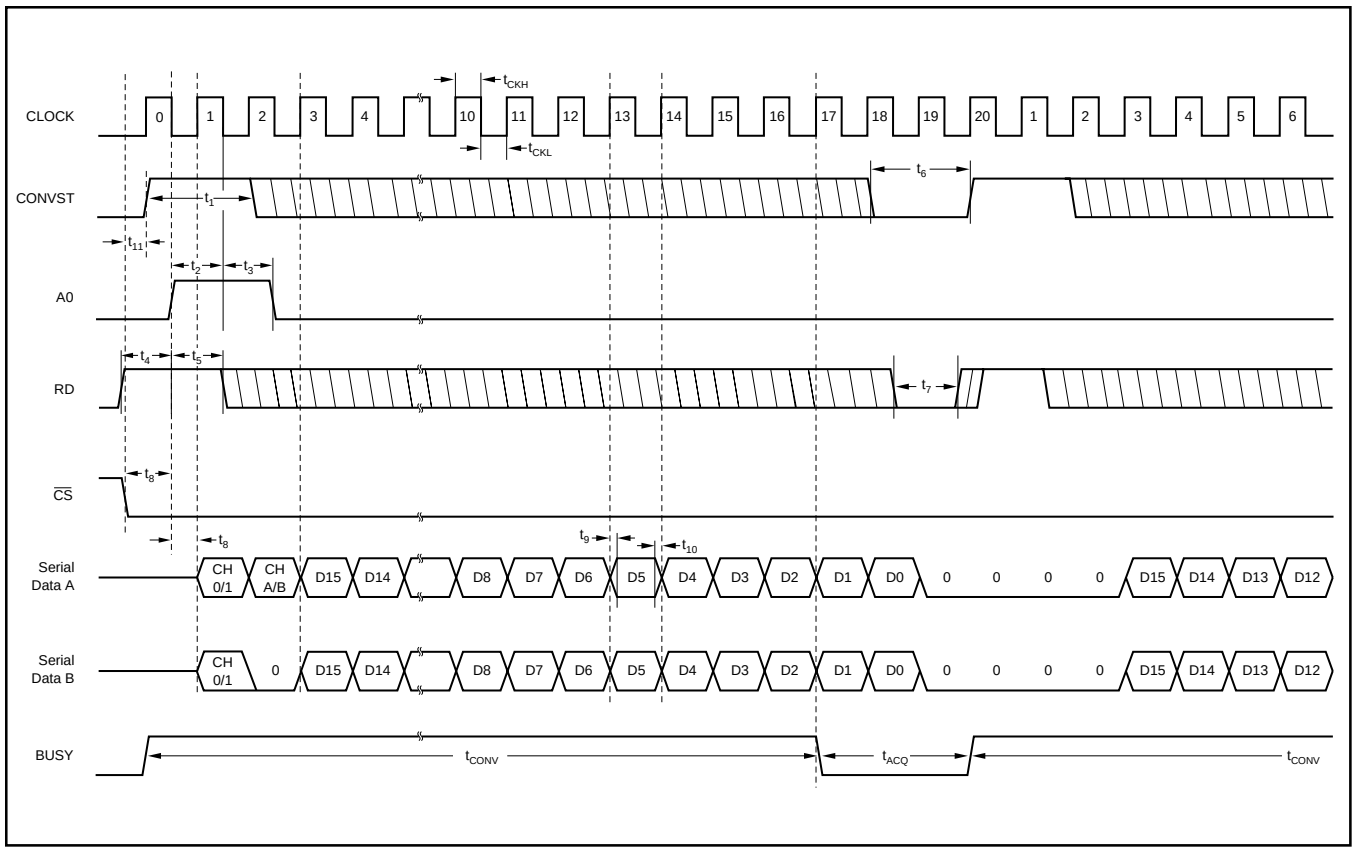
ADS8361



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	BGND	Digital I/O Ground. Connect directly to analog ground (pin 12).
2	CH B1+	Noninverting Input Channel B1
3	CH B1–	Inverting Input Channel B1
4	CH B0+	Noninverting Input Channel B0
5	CH B0–	Inverting Input Channel B0
6	CH A1+	Noninverting Input Channel A1
7	CH A1–	Inverting Input Channel A1
8	CH A0+	Noninverting Input Channel A0
9	CH A0–	Inverting Input Channel A0
10	REF_{IN}	Reference Input
11	REF_{OUT}	2.5V Reference Output
12	AGND	Analog Ground. Connect directly to digital ground (pin 1).
13	AV_{DD}	Analog Power Supply, $+5V_{DC}$. Decouple to analog ground with a 0.1µF ceramic capacitor and a 10µF tantalum capacitor.
14	M1	Selects between the Serial Outputs. When M1 is LOW, both Serial Output A and Serial Output B are selected for data transfer. When M1 is HIGH, Serial output A is configured for both Channel A data and Channel B data; Serial Output B goes into tri-state (i.e., high impedance).
15	M0	Selects between two-channel and four-channel operation. When M0 is LOW, two-channel operation is selected and operates in conjunction with A0. When A0 is HIGH, Channel A1 and Channel B1 are being converted. When A0 is LOW, Channel A0 and Channel B0 are being converted. When M0 is HIGH, four-channel operation is selected. In this mode, all four channels are converted in sequence starting with Channels A0 and B0, followed by Channels A1 and B1.
16	A0	A0 operates in conjunction with M0. With M0 LOW and A0 HIGH, Channel A1 and Channel B1 are converted. With M0 LOW and A0 LOW, Channel A0 and Channel B0 are converted.
17	CONVST	Convert Start. When CONVST switches from LOW to HIGH, the device switches from the sample to hold mode, independent of the status of the external clock.
18	RD	Synchronization Pulse for the Serial Output.
19	$\overline{CS}$	Chip Select. When LOW, the Serial Output A and Serial Output B outputs are active; when HIGH, the serial outputs are tri-stated.
20	CLOCK	An external CMOS-compatible clock can be applied to the CLOCK input to synchronize the conversion process to an external source. The CLOCK pin controls the sampling rate by the equation: f_{SAMPLE}(max) = CLOCK/20.
21	BUSY	BUSY goes HIGH during a conversion and returns LOW after the third LSB has been transmitted on either the Serial A or Serial B output pin.
22	SERIAL DATA B	The Serial Output data word is comprised of channel information and 16 bits of data. In operation, data is valid on the falling edge of DCLOCK for 20 edges after the rising edge of RD.
23	SERIAL DATA A	The Serial Output data word is comprised of channel information and 16 bits of data. In operation, data is valid on the falling edge of DCLOCK for 20 edges after the rising edge of RD. When M1 is HIGH, both Channel A data and Channel B data are available.
24	BV_{DD}	Digital I/O Power Supply, 2.7V to 5.5V

TIMING CHARACTERISTICS



TIMING CHARACTERISTICS

Timing Characteristics over recommended operating free-air temperature range T_{MIN} to T_{MAX}, AV_{DD} = 5V, REF_{IN} = REF_{OUT} internal reference +2.5V, f_{CLK} = 10MHz, f_{SAMPLE} = 500kSPS, and BV_{DD} = 2.7 ÷ 5.5V (unless otherwise noted).

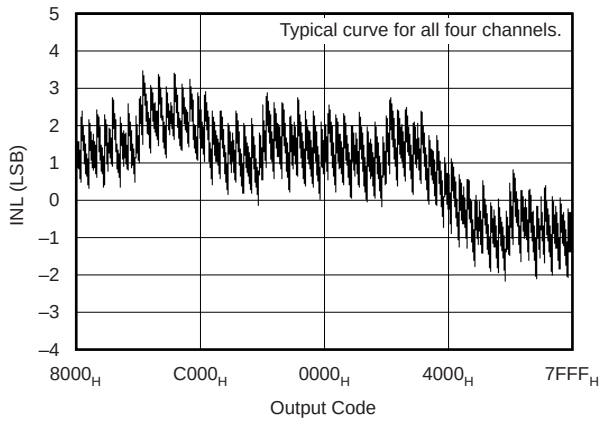
SYMBOL	DESCRIPTION	MIN	MAX	UNITS	COMMENTS
t_{CONV}	Conversion Time	1.6		µs	When T_{CKP} = 100ns
t_{ACQ}	Acquisition Time	0.4		µs	When T_{CKP} = 100ns
t_{CKP}	Clock Period	100	10,000	ns	
t_{CKL}	Clock LOW	40		ns	
t_{CKH}	Clock HIGH	40		ns	
t_F	DOUT Fall Time		25	ns	
t_R	DOUT Rise Time		30	ns	
t_1	CONVST HIGH	15		ns	
t_2	Address Setup Time	15		ns	Address latched on falling edge of CLK cycle ‘2’.
t_3	Address Hold Time	15			
t_4	RD Setup Time	15		ns	Before falling edge of CLOCK.
t_5	RD to $\overline{CS}$ Hold Time	15		ns	After falling edge of CLOCK.
t_6	CONVST LOW	20		ns	
t_7	RD LOW	20		ns	
t_8	$\overline{CS}$ Setup Time	15		ns	Before falling edge of CLOCK (for RD).
t_9	CLOCK to Data Valid Delay		30	ns	Maximum delay following rising edge of CLOCK.
t_{10}	Data Valid After CLOCK(3)		1	ns	Time data is valid after second rising edge of CLOCK.
t_{11}	$\overline{CS}$ Setup Time	0		ns	Before CONVST

NOTES: (1) All input signals are specified with tr = tf = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. (2) See timing diagram above. (3) ‘n – 1’ data will remain valid 1ns after rising edge of next CLOCK cycle.

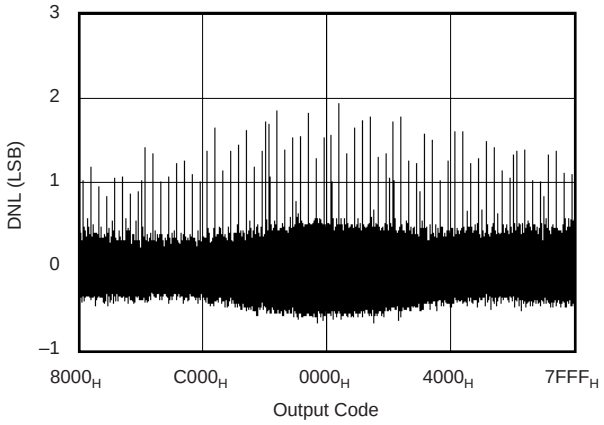
TYPICAL CHARACTERISTICS

At T_A = +25°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 10MHz, and f_{SAMPLE} = 500kHz, unless otherwise noted.

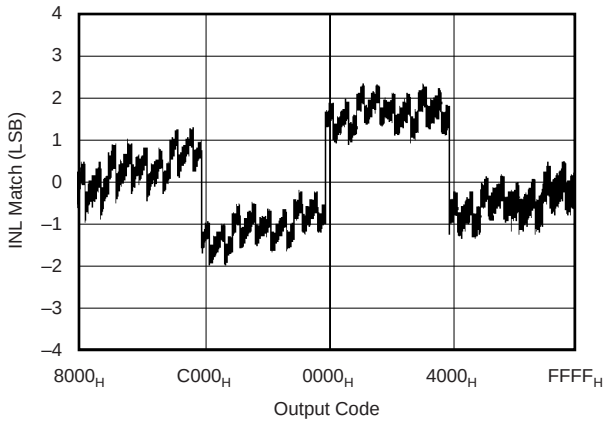
INTEGRAL LINEARITY ERROR vs CODE



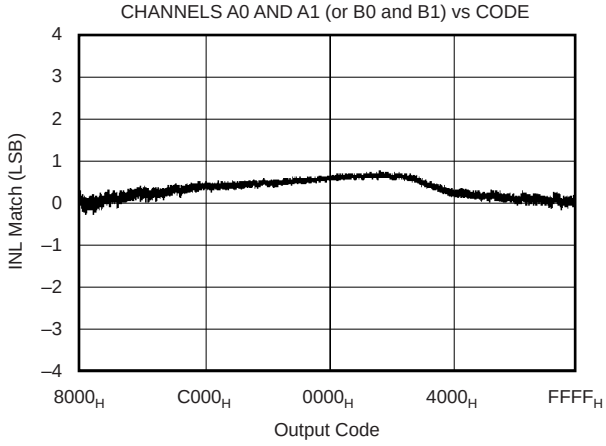
DIFFERENTIAL LINEARITY ERROR vs CODE



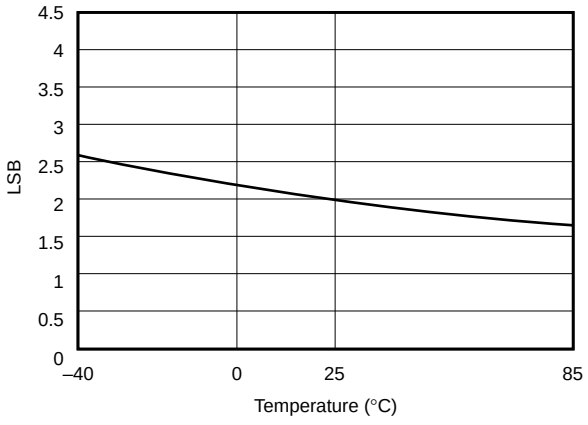
INTEGRAL LINEARITY MATCH OF CHANNELS A0 AND B0 vs CODE



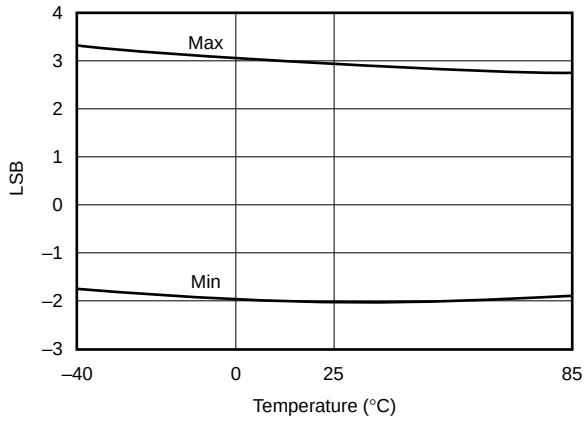
INTEGRAL LINEARITY MATCH OF CHANNELS A0 AND A1 (or B0 and B1) vs CODE



DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE



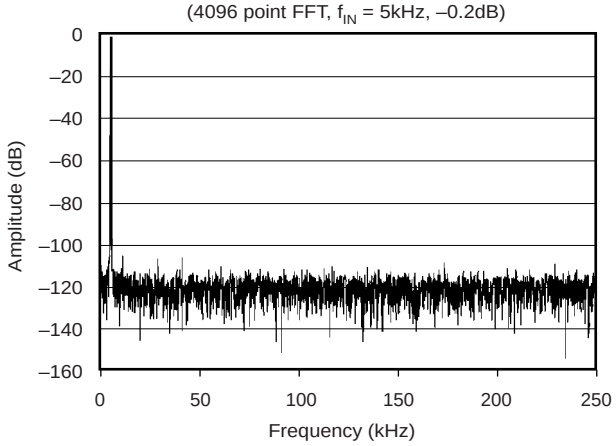
INTEGRAL LINEARITY ERROR MATCH vs TEMPERATURE



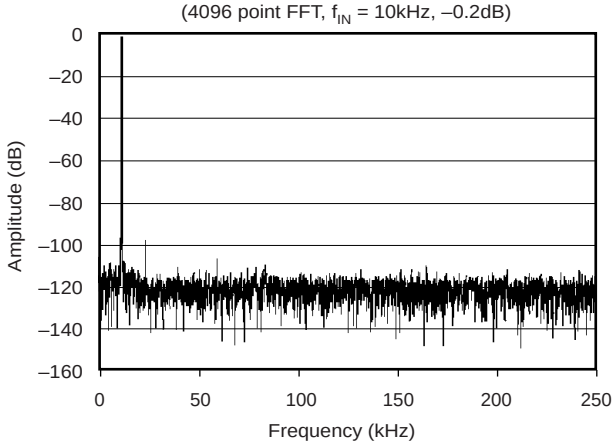
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 10MHz, and f_{SAMPLE} = 500kHz, unless otherwise noted.

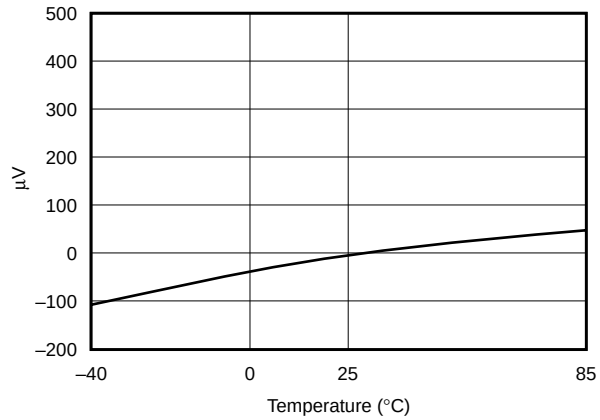
FREQUENCY SPECTRUM
(4096 point FFT, f_{IN} = 5kHz, –0.2dB)



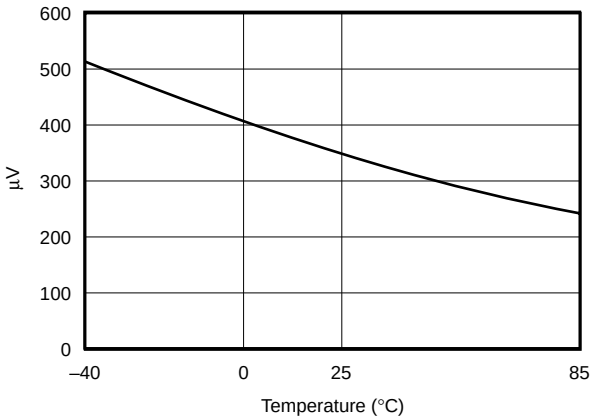
FREQUENCY SPECTRUM
(4096 point FFT, f_{IN} = 10kHz, –0.2dB)



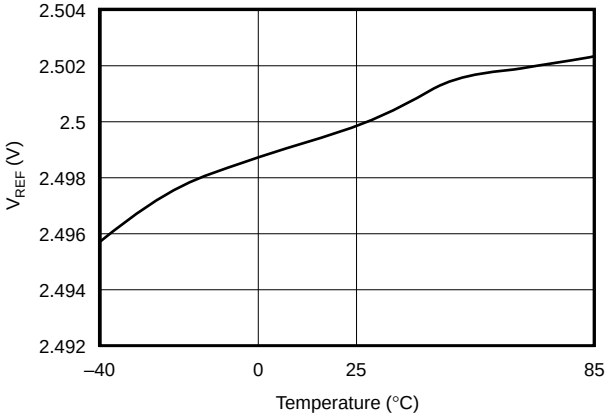
CHANGE IN BIPOLAR OFFSET vs TEMPERATURE



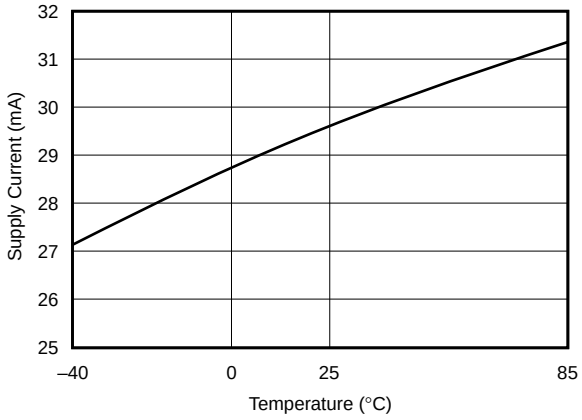
BIPOLAR OFFSET MATCH vs TEMPERATURE
Channel A0/Channel B0



REFERENCE VOLTAGE vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



INTRODUCTION

The ADS8361 is a high-speed, low-power, dual, 16-bit A/D converter that operates from +3V/+5V supply. The input channels are fully differential with a typical common-mode rejection of 80dB. The part contains dual, 4µs successive approximation A/D converter, two differential sample-and-hold amplifiers, an internal +2.5V reference with REF_{IN} and REF_{OUT} pins, and a high-speed serial interface. The ADS8361 requires an external clock. In order to achieve the maximum throughput rate of 500kHz, the master clock must be set at 10MHz. A minimum of 20 clock cycles are required for each 16-bit conversion.

There are four analog inputs that are grouped into two channels (A and B). Channel selection is controlled by the M0 (pin 14), M1 (pin 15), and A0 (pin 16) pins. Each channel has two inputs (A0, A1 and B0, B1) that are sampled and converted simultaneously, thus preserving the relative phase information of the signals on both analog inputs. The part accepts an analog input voltage in the range of $-V_{REF}$ to $+V_{REF}$, centered around the internal +2.5V reference. The part will also accept bipolar input ranges when a level shift circuit is used at the front end (see Figure 7).

All conversions are initiated on the ADS8361 by bringing the CONVST pin HIGH for a minimum of 15ns. CONVST HIGH places both sample-and-hold amplifiers in the hold state simultaneously and the conversion process is started on both channels. The RD pin (pin 18) can be connected to CONVST to simplify operation. Depending on the status of the M0, M1, and A0 pins, the ADS8361 will (a) operate in either two-channel or four-channel mode and (b) output data on both the Serial A and Serial B output or both channels can be transmitted on the A output only.

NOTE: See the Timing and Control section of this data sheet for more information.

SAMPLE-AND-HOLD SECTION

The sample-and-hold amplifiers on the ADS8361 allow the A/D converter to accurately convert an input sine wave of full-scale amplitude to 16-bit accuracy. The input bandwidth of the sample-and-hold is greater than the Nyquist rate (Nyquist equals one-half of the sampling rate) of the A/D converter even when the A/D converter is operated at its maximum throughput rate of 500kHz.

Typical aperture delay time, or the time it takes for the ADS8361 to switch from the sample to the hold mode following the CONVST pulse, is 3.5ns. The average delta of repeated aperture delay values is typically 50ps (also known as aperture jitter). These specifications reflect the ability of the ADS8361 to capture AC input signals accurately at the exact same moment in time.

REFERENCE

Under normal operation, the REF_{OUT} pin (pin 2) should be directly connected to the REF_{IN} pin (pin 1) to provide an internal +2.5V reference to the ADS8361. The ADS8361 can operate, however, with an external reference in the range of 1.2V to 2.6V for a corresponding full-scale range of 2.4V to 5.2V.

The internal reference of the ADS8361 is buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to pin 2 (the internal reference can typically source 10µA of current—load capacitance should be 0.1µF and 10µF). If an external reference is used, the second buffer provides isolation between the external reference and the Capacitve Digital-to-Analog Converter (CDAC). This buffer is also used to recharge all of the capacitors of both CDACs during conversion.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS8361: single-ended or differential (see Figures 1 and 2). When the input is single-ended, the –IN input is held at the common-mode voltage. The +IN input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode + V_{REF}) and the (common-mode – V_{REF}). The value of V_{REF} determines the range over which the common-mode voltage may vary (see Figure 3).

When the input is differential, the amplitude of the input is the difference between the +IN and –IN input, or (+IN) – (–IN). The peak-to-peak amplitude of each input is ±1/2 V_{REF} around this common voltage. However, since the inputs are 180° out-of-phase, the peak-to-peak amplitude of the differential voltage is $+V_{REF}$ to $-V_{REF}$. The value of V_{REF} also determines the range of the voltage that may be common to both inputs (see Figure 4).

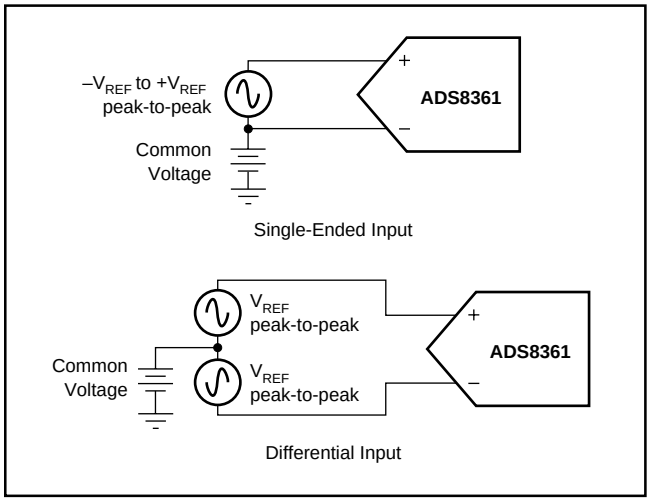
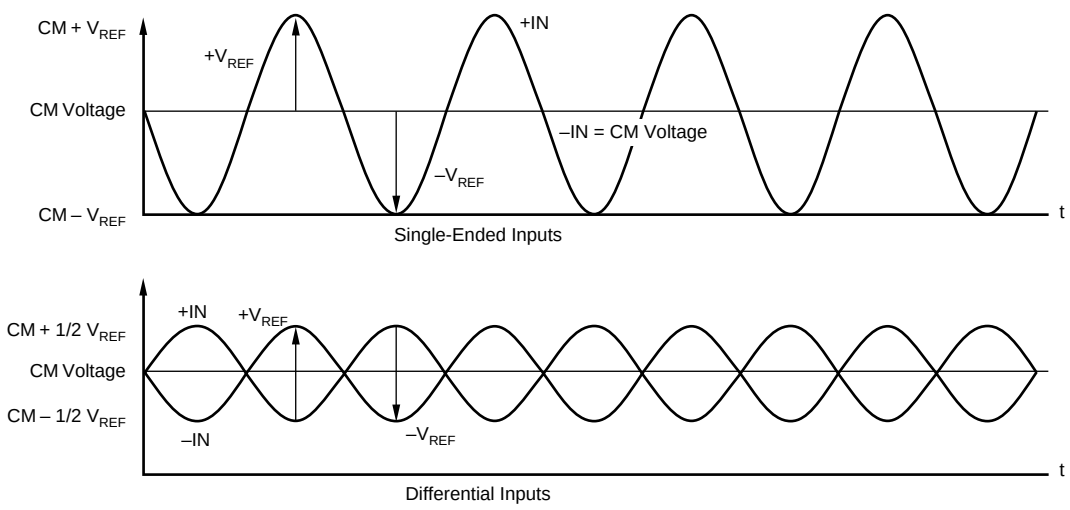


FIGURE 1. Methods of Driving the ADS8361 Single-Ended or Differential.



NOTES: Common-Mode Voltage (Differential Mode) = $\frac{(+IN) + (-IN)}{2}$, Common-Mode Voltage (Single-Ended Mode) = IN–.

The maximum differential voltage between +IN and –IN of the ADS8361 is V_{REF}. See Figures 3 and 4 for a further explanation of the common voltage range for single-ended and differential inputs.

FIGURE 2. Using the ADS8361 in the Single-Ended and Differential Input Modes.

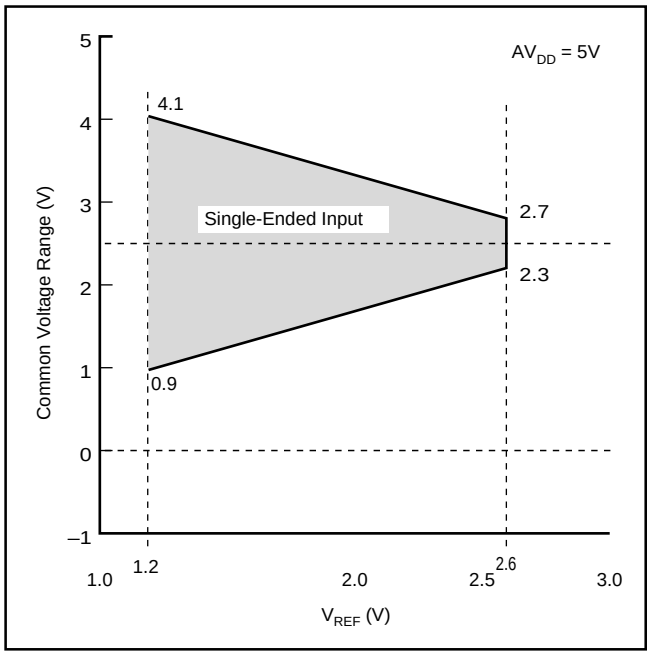


FIGURE 3. Single-Ended Input: Common-Mode Voltage Range vs V_{REF}.

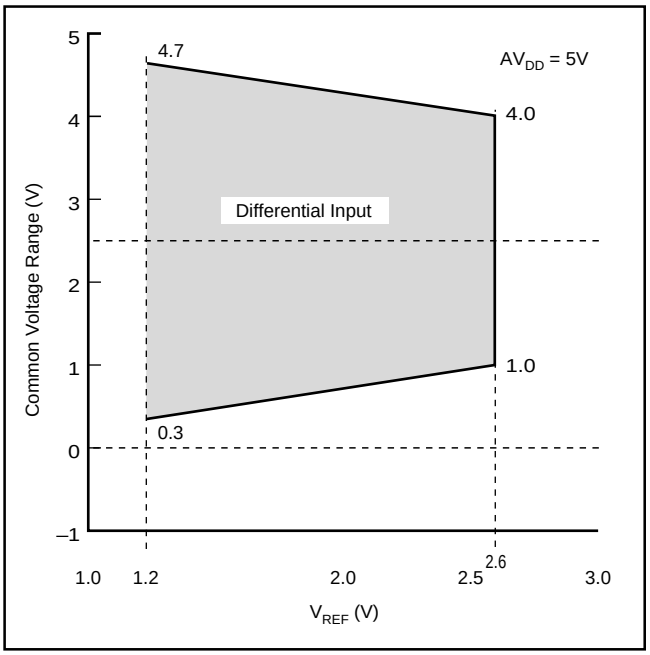


FIGURE 4. Differential Input: Common-Mode Voltage Range vs V_{REF}.

In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. Otherwise, this may result in offset error, gain error, and linearity error which will change with both temperature and input voltage.

The input current on the analog inputs depend on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8361 charges the internal capacitor array during the sampling period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25pF) to a 16-bit settling level within 4 clock cycles. When the converter goes into the hold mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. The +IN and –IN inputs should always remain within the range of AGND – 0.3V to AV_{DD} + 0.3V.

TRANSITION NOISE

The transition noise of the ADS8361 itself is low, as shown in Figure 5. These histograms were generated by applying a low-noise DC input and initiating 8000 conversions. The digital output of the A/D converter will vary in output code due to the internal noise of the ADS8361. This is true for all 16-bit, Successive Approximation Register (SAR-type) A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ, and ±3σ distributions will represent the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this will yield the ±3σ distribution, or 99.7%, of all codes. Statistically, up to three codes could fall outside the distribution when executing 1000 conversions. Remember, to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be < 50µV.

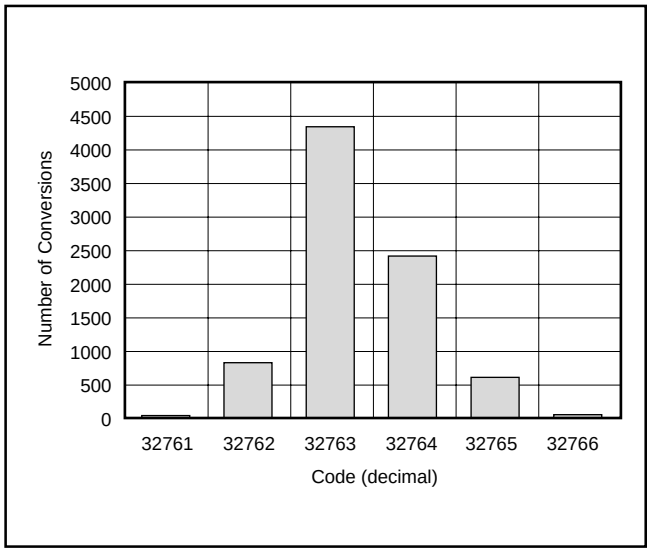


FIGURE 5. Histogram of 8000 Conversions of a DC Input.

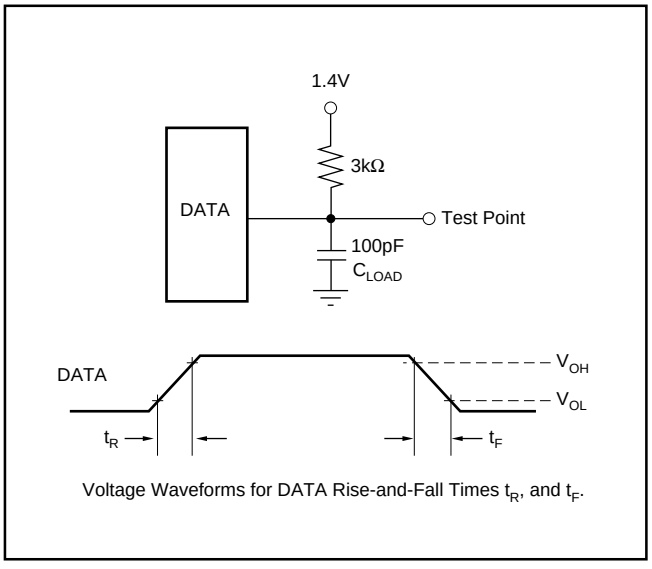
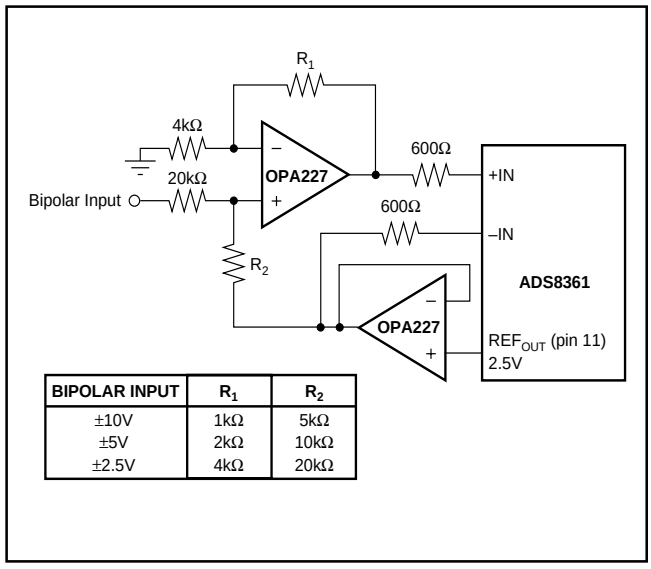


FIGURE 6. Test Circuits for Timing Specifications.

BIPOLAR INPUTS

The differential inputs of the ADS8361 were designed to accept bipolar inputs ($-V_{REF}$ and $+V_{REF}$) around the internal reference voltage (2.5V), which corresponds to a 0V to 5V input range with a 2.5V reference. By using a simple op amp circuit featuring a single amplifier and four external resistors, the ADS8361 can be configured to except bipolar inputs. The conventional ±2.5V, ±5V, and ±10V input ranges can be interfaced to the ADS8361 using the resistor values shown in Figure 7.



BIPOLAR INPUT	R_1	R_2
±10V	1kΩ	5kΩ
±5V	2kΩ	10kΩ
±2.5V	4kΩ	20kΩ

FIGURE 7. Level Shift Circuit for Bipolar Input Ranges.

TIMING AND CONTROL

The operation of the ADS8361 can be configured in four different modes by using the address pins M0 (pin 14), M1 (pin 15), and A0 (pin 16).

The M0 pin selects between two- and four-channel operation (in two-channel operation, the A0 pin selects between Channels 0 and 1; in four-channel operation the A0 pin is ignored and the channels are switched automatically after each conversion). The M1 pin selects between having serial data transmitted simultaneously on both the Serial A data output (pin 23) and the Serial B data output (pin 22) or having both channels output data through the Serial A port. The A0 pin selects either Channel 0 or Channel 1 (see Pin Descriptions and Serial Output Truth Table for more information).

The next four sections will explain the four different modes of operation.

Mode I (M0 = 0, M1 = 0)

With the M0 and M1 pins both set to '0', the ADS8361 will operate in two-channel operation (the A0 pin must be used to switch between Channels A and B). A conversion is initiated by bringing CONVST HIGH for a minimum of 15ns. It is very important that CONVST be brought HIGH a minimum of 10ns prior to a falling edge of the external clock or 5ns after the falling edge. If CONVST is brought HIGH within this window, it is then uncertain as to when the ADS8361 will initiate conversion (see Figure 9 for a more detailed descrip-

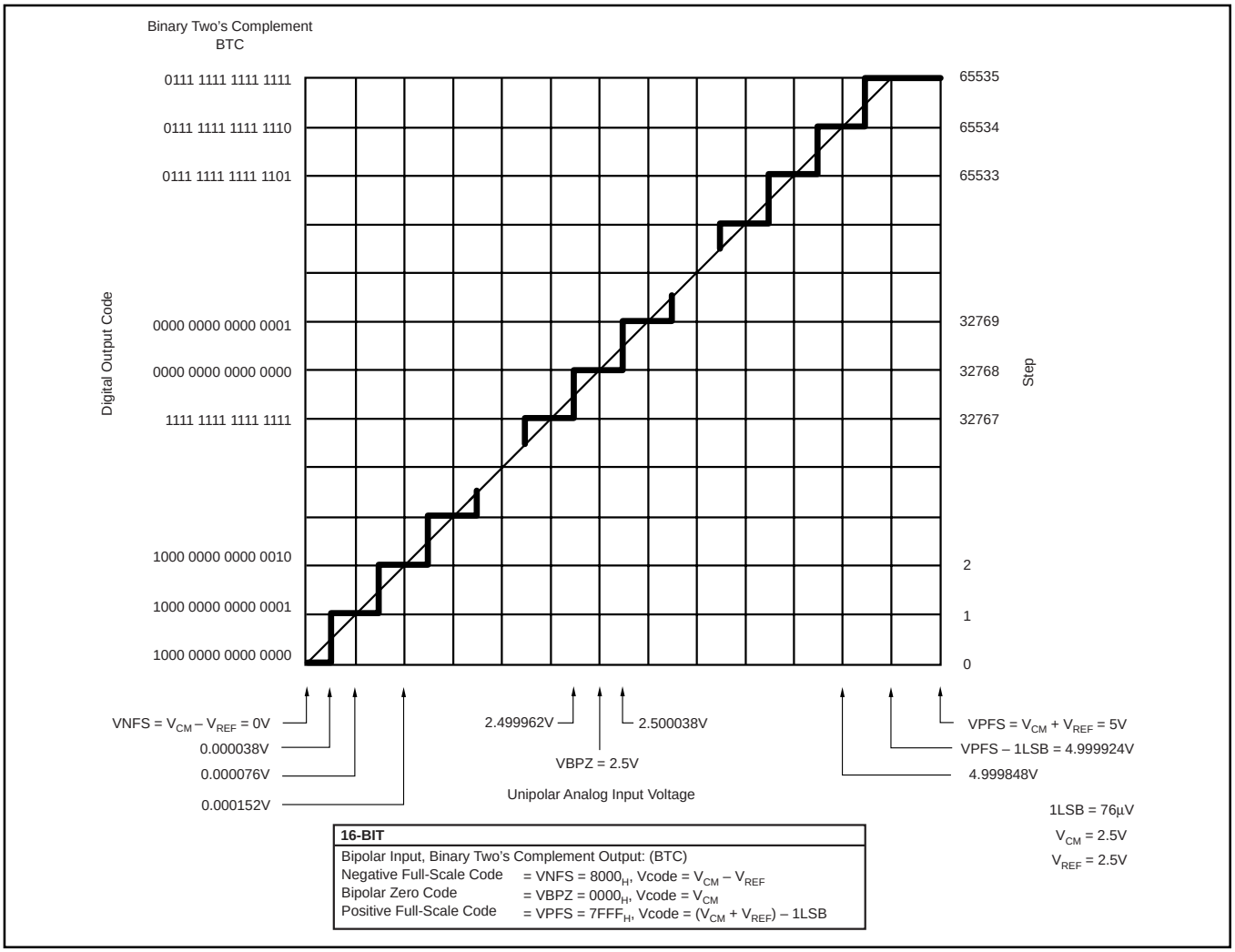


FIGURE 8. Ideal Conversion Characteristics (Condition: Single Ended, VCM = chXX– = 2.5V, V_{REF} = 2.5V)

tion). Twenty clock cycles are required to perform a single conversion. Immediately following CONVST switching to HIGH, the ADS8361 will switch from the sample mode to the hold mode asynchronous to the external clock. The BUSY output pin will then go HIGH and remain HIGH for the duration of the conversion cycle. On the falling edge of the first cycle of the external clock, the ADS8361 will latch in the address for the next conversion cycle depending on the status of the A0 pin (HIGH = Channel 1, LOW = Channel 0). The address must be selected 15ns prior to the falling edge of cycle one of the external clock and must remain 'held' for 15ns following the clock edge. For maximum throughput time, the CONVST and RD pins should be tied together. CS must be brought LOW to enable the CONVST and RD inputs. Data will be valid on the falling edge of all 20 clock cycles per conversion. The first bit of data will be a status flag for either Channel 0 or 1, the second bit will be a second status flag for either Channel A or B. First and second bit will be 0 in Mode I. See Table II below. The subsequent data will be MSB-first through the LSB, followed by two zeros (see Table III and Figures 9 and 10).

MODE	M0	BIT 1 M1	BIT 2 CH0/1	CHA/B	CHANNEL SELECTION	DATA OUTPUT
1	0	0	0	0	Ch0/1 Selected by A0	On Data A and B
2	0	1	0	0 = A/1 = B	Ch0/1 Selected by A0	Sequentially on Data A
3	1	0	0/1	0	Ch0/1 Alternating	On Data A and B
4	1	1	0/1	0 = A/1 = B	Ch0/1 Alternating	Sequentially on Data A

TABLE II. Mode Selection.

CLOCK CYCLE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SERIAL DATA	CH0 OR CH1	CHA OR CHB	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0

TABLE III. Serial Data Output Format.

Mode II (M0 = 0, M1 = 1)

With M1 set to '1', the ADS8361 will output data on the Serial Data A pin only. All other pins function in the same manner as Mode I except that the Serial Data B output will tri-state (i.e., high impedance) after a conversion following M1 going HIGH. Another difference in this mode involves the CONVST pin. Since it takes 40 clock cycles to output the results from both A/D converters (rather than 20 when M1 = 0), the ADS8361 will take 4µs to complete a conversion on both A/D converters (See Figure 11).

Mode III (M0 = 1, M1 = 0)

With M0 set to '1', the ADS8361 will cycle through Channels 0 and 1 sequentially (the A0 pin is ignored). At the same time, setting M1 to '0' places both Serial Outputs, A and B, in the active mode (See Figure 12).

Mode IV (M0 = 1, M1 = 1)

Similar to Mode II, Mode IV uses the Serial A output line to transmit data exclusively. Following the first conversion after M1 goes HIGH, the serial B output will go into tri-state. See Figure 13. As in Mode II, the second CONVST command is always ignored when M1 = 1.

READING DATA

In all four timing diagrams, the CONVST pin and the RD pins are tied together. If so desired, the two lines can be separated. Data on the Serial Output pins (A and B) will become valid following the third rising SCLK edge following RD rising edge. Refer to Table III for data output format.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8361 circuitry. This is particularly true if the CLOCK input is approaching the maximum throughput rate.

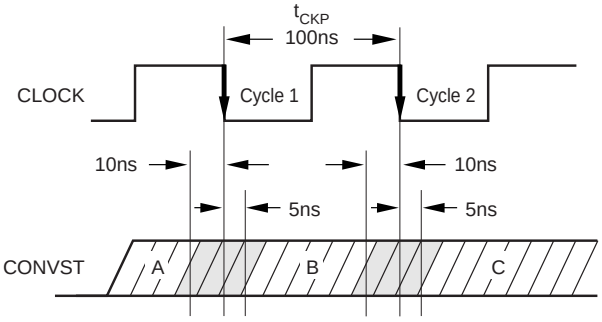
The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. Their error can change if the external event changes in time with respect to the CLOCK input.

With this in mind, power to the ADS8361 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply. On average, the ADS8361 draws very little current from an external reference as the reference voltage is internally buffered. However, glitches from the conversion process appear at the V_{REF} input and the reference source must be able to handle this. Whether the reference is internal or external, the V_{REF} pin should be bypassed with a 0.1µF capacitor. An additional larger capacitor may also be used, if desired. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. No bypass capacitor is necessary when using the internal reference (tie pin 10 directly to pin 11).

The GND pin should be connected to a clean ground point. In many cases, this will be the 'analog' ground. Avoid connections which are too near the grounding point of a microcontroller or Digital Signal Processor (DSP). If required, run a ground trace directly from the converter to the power-supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

APPLICATION INFORMATION

In Figures 14 through 17, different connection diagrams to DSPs or microcontrollers are shown.



NOTE: All CONVST commands which occur more than 10ns before the falling edge before cycle '1' of the external clock (Region 'A') will initiate a conversion on the rising edge of cycle '1'. All CONVST commands which occur 5ns after the falling edge before cycle '1' or 10ns before the falling edge before cycle 2 (Region 'B') will initiate a conversion on the rising edge of cycle '2'. All CONVST commands which occur 5ns after the falling edge of cycle '2' (Region 'C') will initiate a conversion on the rising edge of the next clock period. The CONVST pin should never be switched from LOW to HIGH in the region 10ns prior to the falling edge of the CLOCK and 5ns after the falling edge (gray areas). If CONVST is toggled in this gray area, the conversion could begin on either the same rising edge of the CLOCK or the following edge.

FIGURE 9. Conversion Mode.

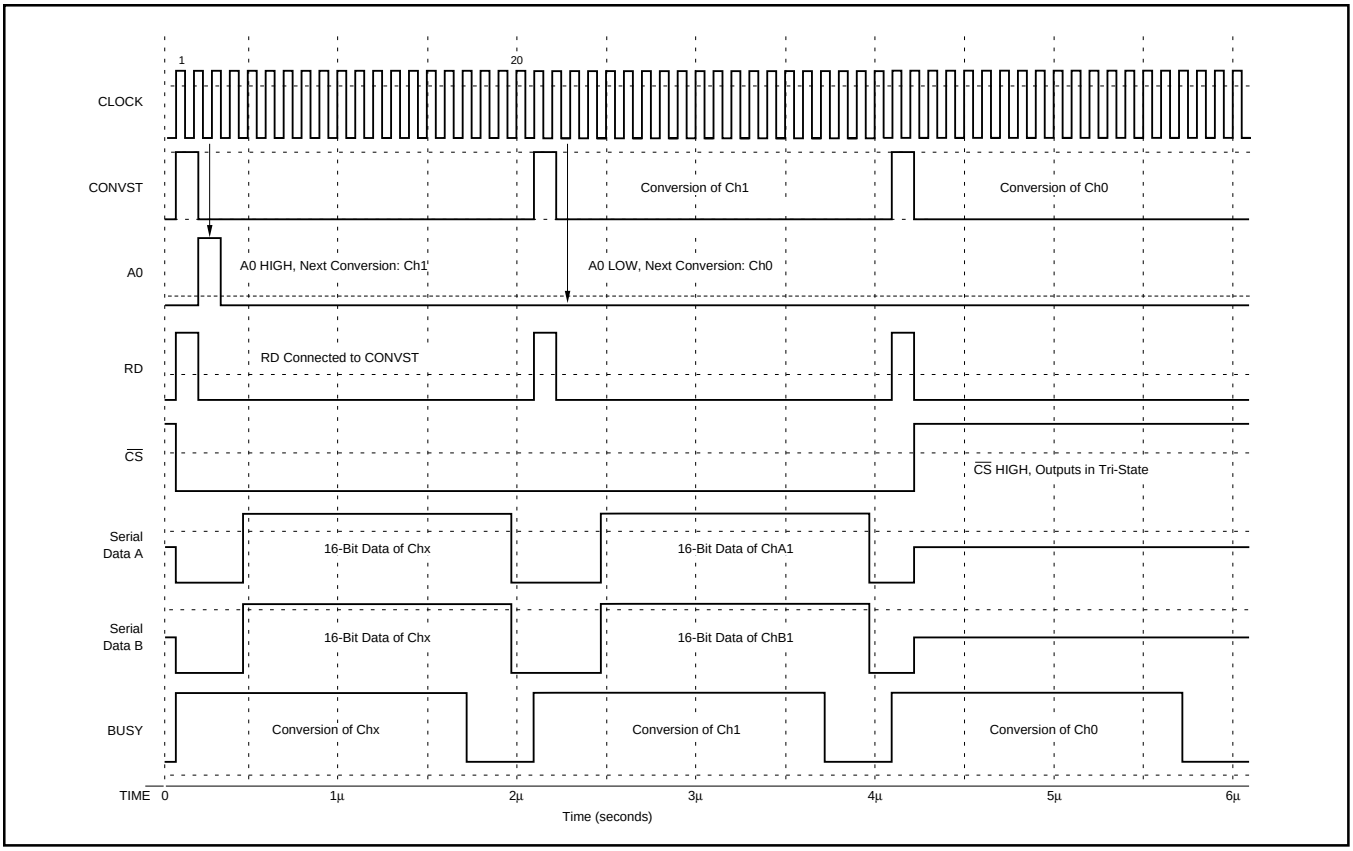


FIGURE 10. Mode I, Timing Diagram for M0 = 0 and M1 = 0.

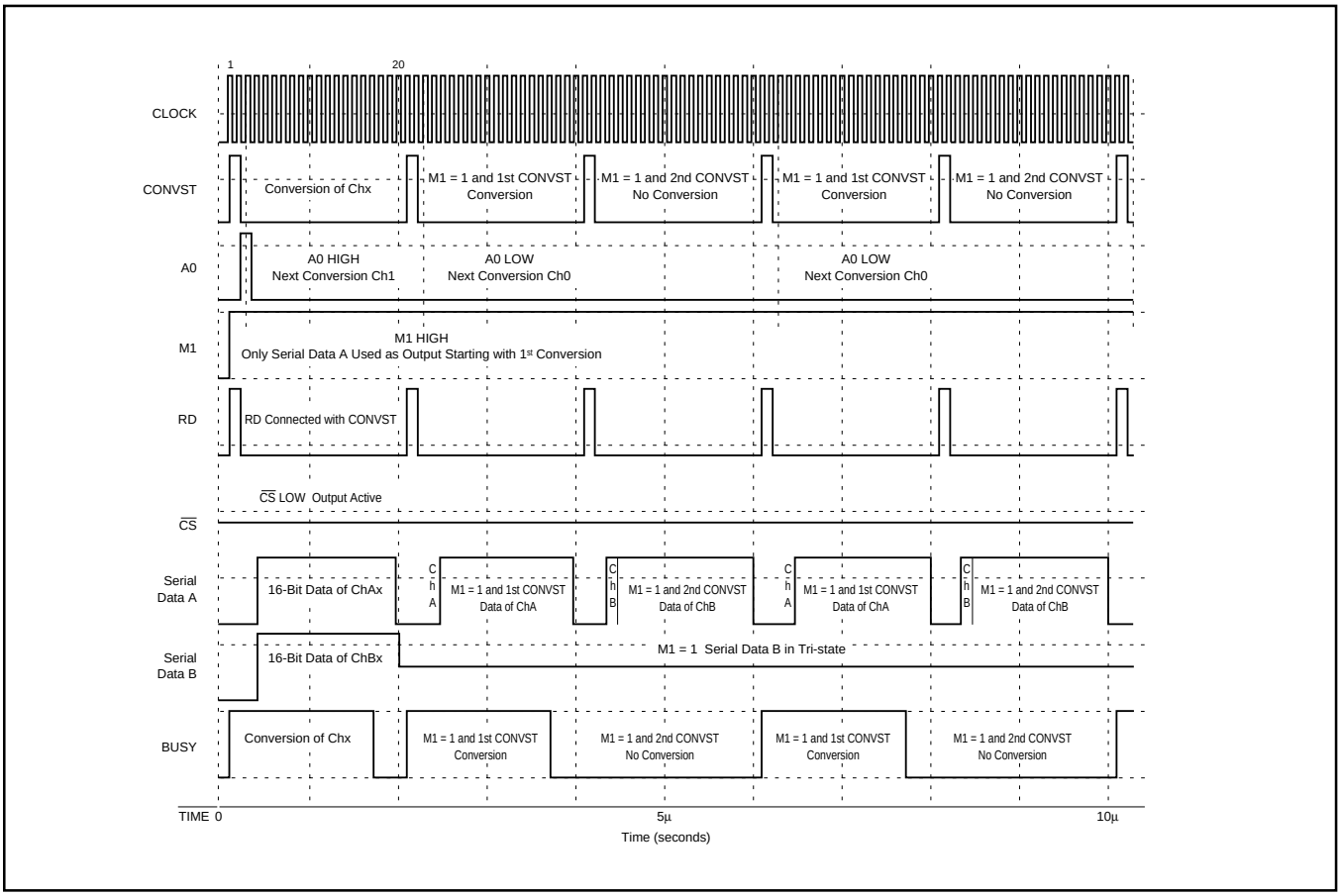


FIGURE 11. Mode II, Timing Diagram for M0 = 0 and M1 = 1.

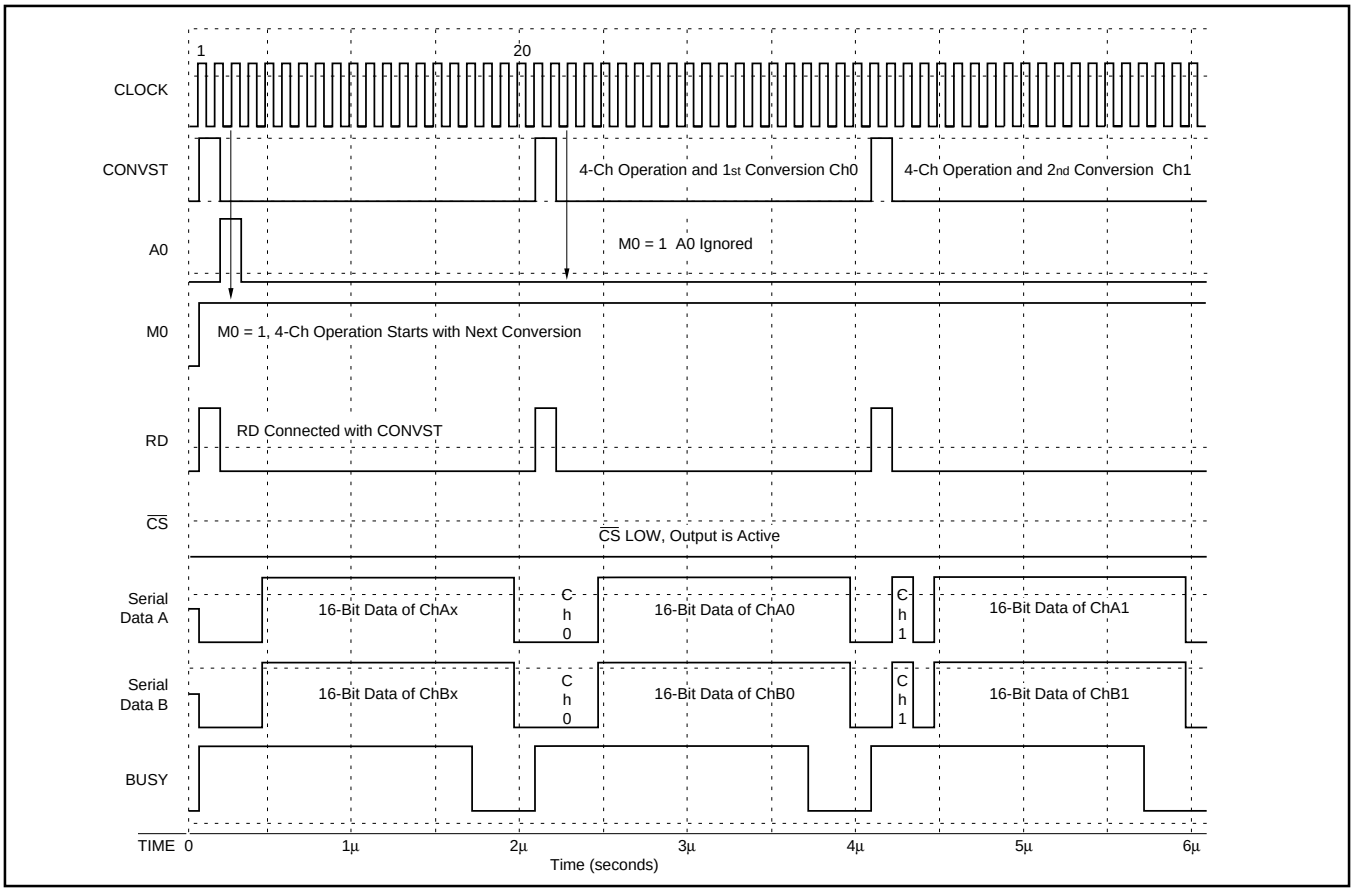


FIGURE 12. Mode III, Timing Diagram for M0 = 1 and M1 = 0.

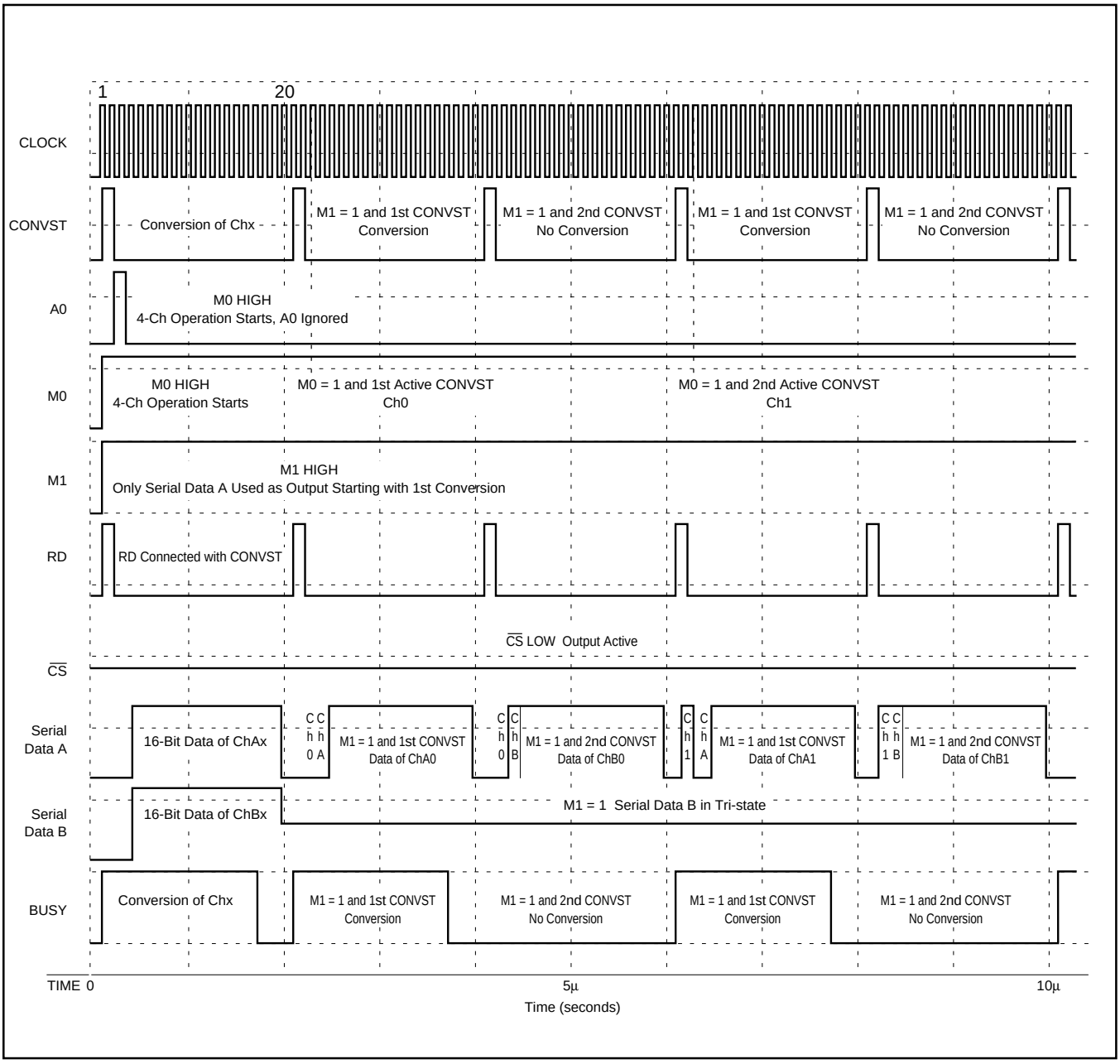


FIGURE 13. Mode IV, Timing Diagram for M0 = 1 and M1 = 1.

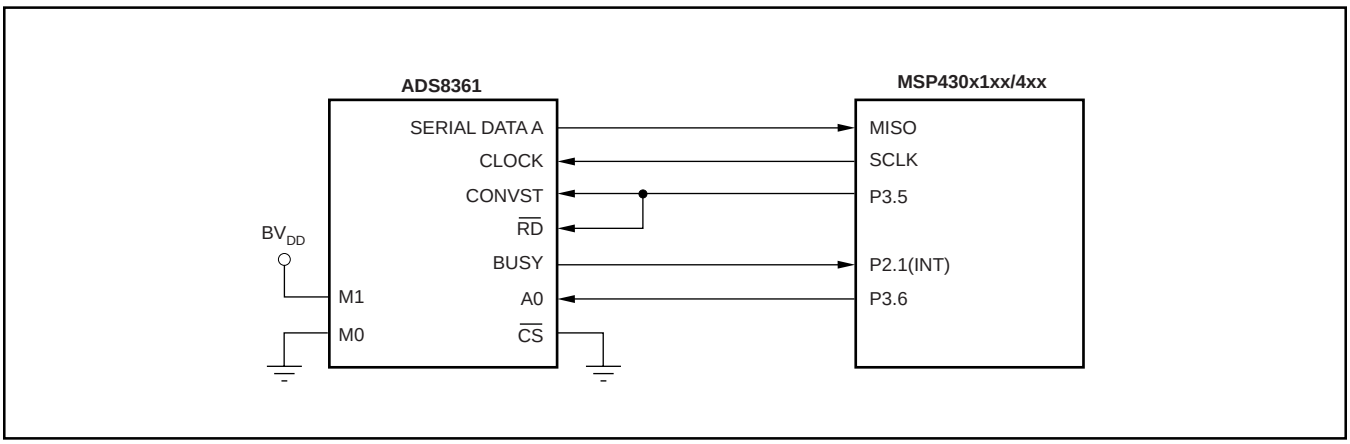


FIGURE 14. 2x2 Channel Using A Output.

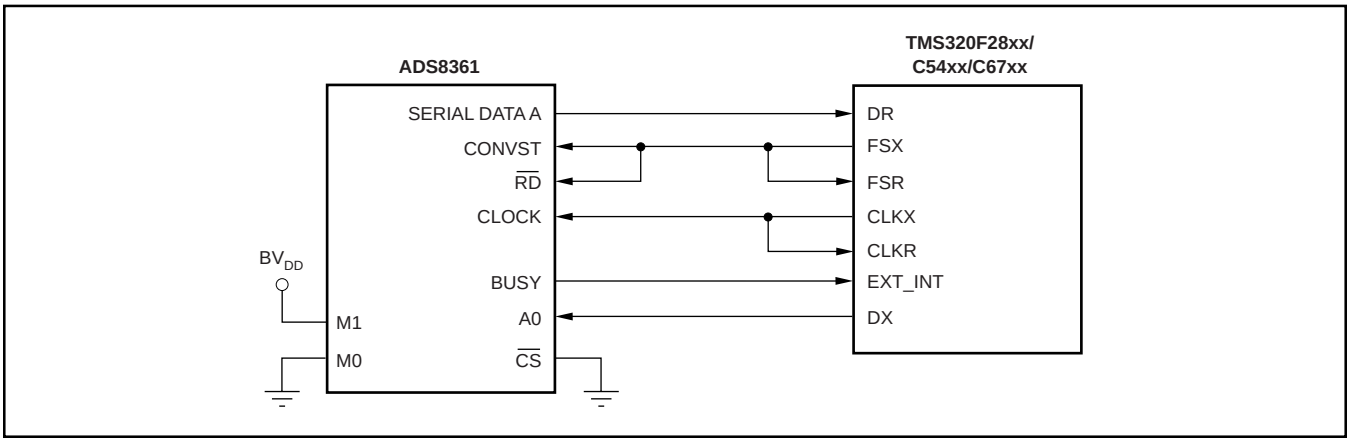


FIGURE 15. 2x2 Channel Using A Output.

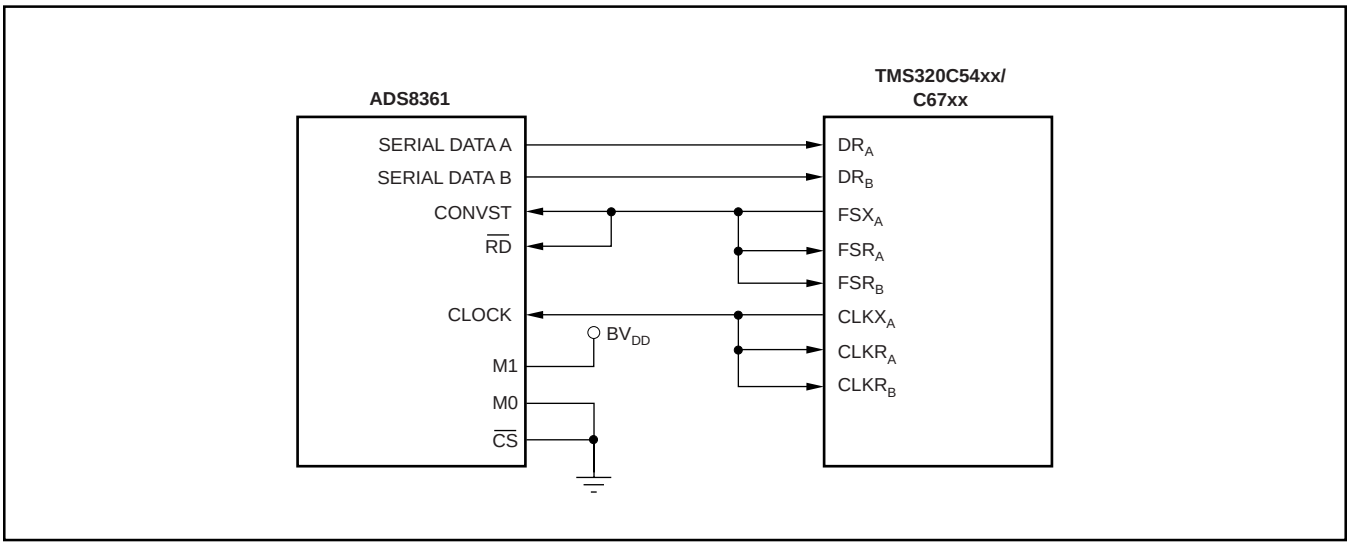


FIGURE 16. 4-Channel Sequential Mode Using A and B Outputs.

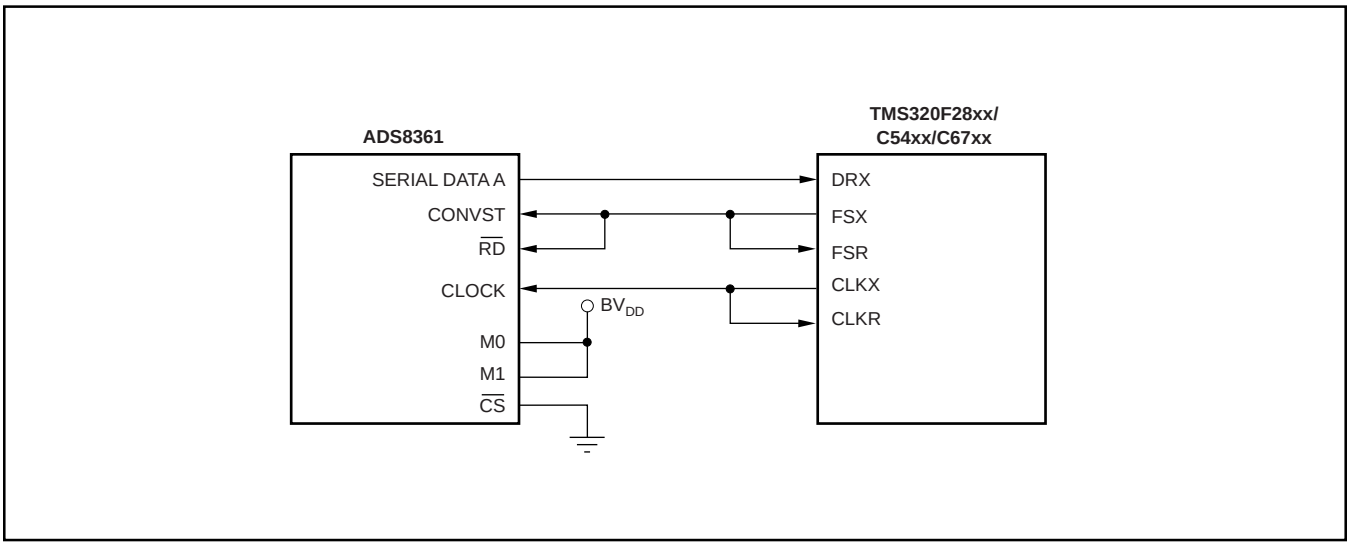
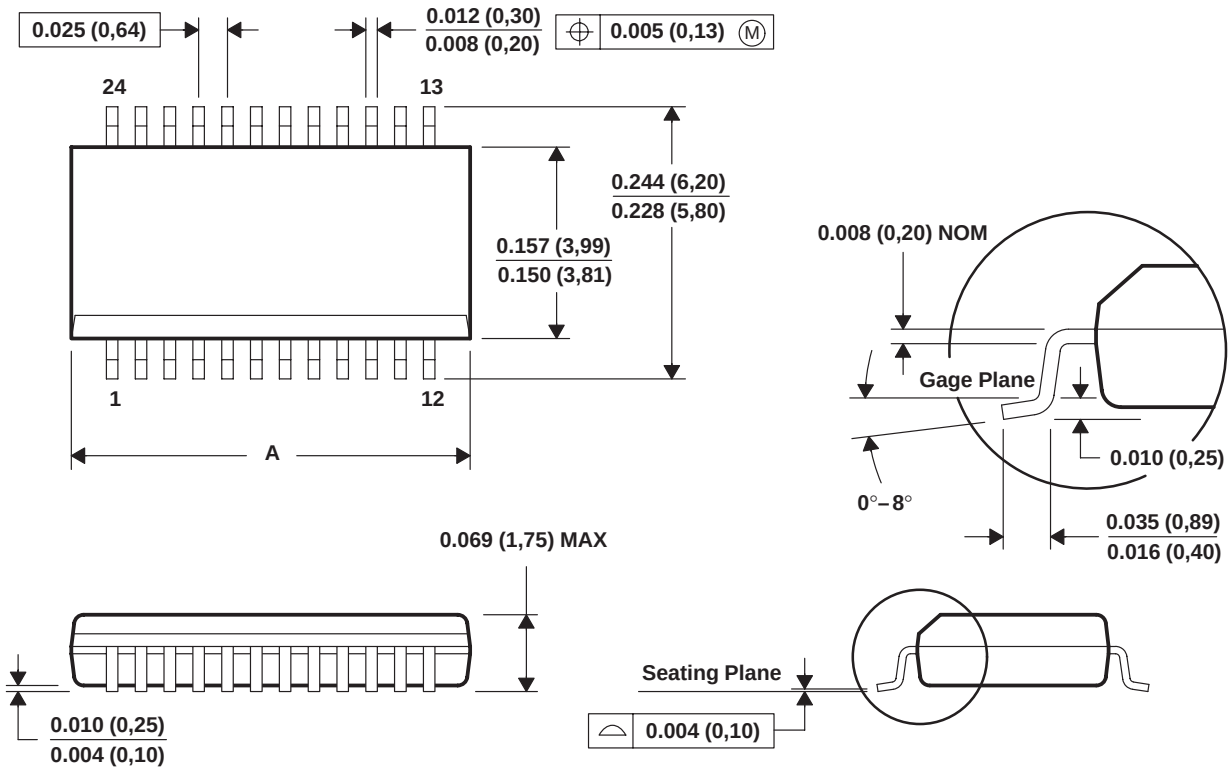


FIGURE 17. 4-Channel Sequential Mode Using A Output.

PACKAGE DRAWING

DBQ (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.188 (4,78)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)

4073301/E 10/00

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-137

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