查询ADS8371供应商 捷多邦，专业PCB打样工厂，24小时加急出货

16-BIT, 850-kHz, UNIPOLAR INPUT, MICRO POWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE

FEATURES

- 850-kHz Sample Rate
- 16-Bit NMC Ensured Over Temperature
- Zero Latency
- Low Power: 110 mW at 850 kHz
- Unipolar Input Range
- Onboard Reference Buffer
- High-Speed Parallel Interface
- Wide Digital Supply, 2.7 V to 5.25 V
- 8-/16-Bit Bus Transfer
- 48-Pin TQFP Package

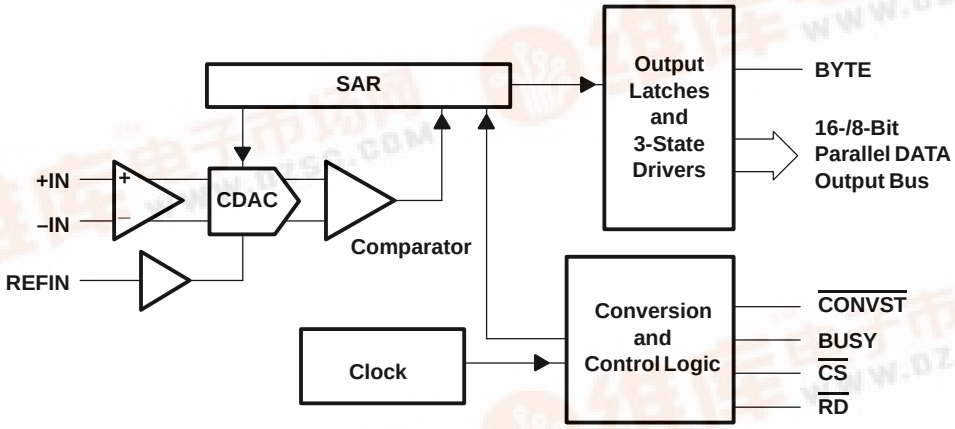
APPLICATIONS

- Medical Instruments
- Optical Networking
- Transducer Interface
- High Accuracy Data Acquisition Systems
- Magnetometers

DESCRIPTION

The ADS8371 is an 16-bit, 850 kHz A/D converter. The device includes a 16-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8371 offers a full 16-bit interface, using two read cycles, or an 8-bit bus option using three read cycles.

The ADS8371 is available in a 48-lead TQFP package and is characterized over the industrial –40°C to 85°C temperature range.



PRODUCT PREVIEW

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PRODUCT PREVIEW information concerns products in the formative or design

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS8371I	±4	–2~2	15	48 Pin TQFP	PFB	–40°C to 85°C	ADS8371IPFBT	Tape and reel 250
							ADS8371IPFBR	Tape and reel 1000
ADS8371IB	±2	–1~2	16	48 Pin TQFP	PFB	–40°C to 85°C	ADS8371IBPFBT	Tape and reel 250
							ADS8371IBPFBR	Tape and reel 1000

NOTE: For the most current specifications and package information, refer to our website at www.ti.com.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNIT
Voltage	+IN to AGND		–0.4 V to +VA + 0.1 V
	–IN to AGND		–0.4 V to 0.5 V
Voltage range	+VA to AGND		–0.3 V to 7 V
	+VBD to BDGND		–0.3 V to 7 V
	+VA to +VBD		–0.3 V to 2.55 V
Digital input voltage to BDGND			–0.3 V to +VBD + 0.3 V
Digital output voltage to BDGND			–0.3 V to +VBD + 0.3 V
Operating free-air temperature range, T_A			–40°C to 85°C
Storage temperature range, T_{stg}			–65°C to 150°C
Junction temperature (T_J max)			150°C
TQFP package	Power dissipation		$(T_J Max – T_A)/\theta_{JA}$
	θ_{JA} thermal impedance		86°C/W
Lead temperature, soldering		Vapor phase (60 sec)	215°C
		Infrared (15 sec)	220°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

T_A = –40°C to 85°C, +VA = 5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 850 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input						
Full-scale input voltage (1)		+IN – –IN	0		V_{ref}	V
Absolute input voltage		+IN	–0.2		V_{ref} + 0.2	V
		–IN	–0.2		0.2	
Input capacitance				45		pF
Input leakage current				1		nA
System Performance						
Resolution				18		Bits
No missing codes	ADS8371I		15			Bits
	ADS8371IB		16			
Integral linearity (2) (3)	ADS8371I		–4	±1.5	4	LSB
	ADS8371IB		–2	±1.5	2	
Differential linearity	ADS8371I		–2	±1	2	LSB
	ADS8371IB		–1	±1	2	
Offset error (4)	ADS8371I		–1	±0.5	1	mV
	ADS8371IB		–0.75	±0.25	0.75	
Gain error (4)	ADS8371I	V_{ref} = 4.096 V	–0.1		0.1	%FS
	ADS8371IB	V_{ref} = 4.096 V	–0.06		0.06	%FS
Noise				60		µV RMS
Power supply rejection ratio		At FFFFh output code		75		dB
Sampling Dynamics						
Conversion time					0.9	µs
Acquisition time			0.25			µs
Throughput rate					850	kHz
Aperture delay				4		ns
Aperture jitter				15		ps
Step response				150		ns
Over voltage recovery				150		ns

(1) Ideal input span, does not include gain or offset error.
(2) LSB means least significant bit
(3) This is endpoint INL, not best fit.
(4) Measured relative to an ideal full-scale input (+IN – –IN) of 4.096 V

PRODUCT PREVIEW

TEXAS INSTRUMENTS
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SPECIFICATIONS (CONTINUED)

T_A = –40°C to 85°C, +VA = +5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 850 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DynamicCharacteristics						
Total harmonic distortion (THD) (1)	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				dB
	ADS8371IB					
	ADS8371I	V_{IN} = 4 V_{pp} at 10 kHz		–96		
	ADS8371IB			–100		
	ADS8371I	V_{IN} = 4 V_{pp} at TBD0 kHz				
	ADS8371IB					
	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				
	ADS8371IB					
Signal to noise ratio (SNR) (1)	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				dB
	ADS8371IB					
	ADS8371I	V_{IN} = 4 V_{pp} at 10 kHz		84		
	ADS8371IB			86		
	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				
	ADS8371IB					
	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				
	ADS8371IB					
Signal to noise + distortion (SINAD) (1)	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				dB
	ADS8371IB					
	ADS8371I	V_{IN} = 4 V_{pp} at 10 kHz		83		
	ADS8371IB			85		
	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				
	ADS8371IB					
	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				
	ADS8371IB					
Spurious free dynamic range (SFDR) (1)	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				dB
	ADS8371IB					
	ADS8371I	V_{IN} = 4 V_{pp} at 10 kHz		96		
	ADS8371IB			100		
	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				
	ADS8371IB					
	ADS8371I	V_{IN} = 4 V_{pp} at TBD kHz				
	ADS8371IB					
–3 dB Small signal bandwidth				3		MHz
Voltage Reference Input						
Reference voltage at REFIN, V_{ref}			2.5	4.096	4.2	V
Reference resistance (2)				500		kΩ
Reference current drain		f_S = 580 kHz			1	mA

(1) Calculated on the first nine harmonics of the input frequency
(2) Can vary ±20%

PRODUCT PREVIEW

SPECIFICATIONS (CONTINUED)

T_A = –40°C to 85°C, +VA = +5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 850 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input/Output						
Logic family				CMOS		
Logic level	V_{IH}	I_{IH} = 5 µA	+VBD–1		$+V_{BD}$ + 0.3	V
	V_{IL}	I_{IL} = 5 µA	–0.3		0.8	
	V_{OH}	I_{OH} = 2 TTL loads	$+V_{BD}$ – 0.6			
	V_{OL}	I_{OL} = 2 TTL loads			0.4	
Data format				Straight Binary		
Power Supply Requirements						
Power supply voltage	+VBD		2.7	3.3	5.25	V
	+VA		4.75	5	5.25	V
Supply current, 500-kHz sample rate (1)				22	26	mA
Power dissipation, 500-kHz sample rate (1)				110	130	mW
Temperature Range						
Operating free-air			–40		85	°C

(1) This includes only +VA current. +VBD current is typical 1 mA with 5 pF load capacitance on all output pins.

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TIMING CHARACTERISTICS

All specifications typical at –40°C to 85°C, +VA = +VBD = 5 V (1) (2) (3)

	PARAMETER	MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time			0.92	µs
t_{ACQ}	Acquisition time	0.25			µs
t_{HOLD}	Sampling capacitor hold time			25	ns
t_{pd1}	$\overline{CONVST}$ low to conversion started (BUSY high)			45	ns
t_{pd2}	Propagation delay time, End of conversion to BUSY low			20	ns
t_{pd3}	Propagation delay time, from start of conversion (internal state) to rising edge of BUSY			20	ns
t_{w1}	Pulse duration, $\overline{CONVST}$ low	40			ns
t_{su1}	Setup time, $\overline{CS}$ low to $\overline{CONVST}$ low	20			ns
t_{w2}	Pulse duration, $\overline{CONVST}$ high	20			ns
	$\overline{CONVST}$ falling edge jitter			10	ps
t_{w3}	Pulse duration, BUSY signal low	Min(t_{ACQ})		1	µs
t_{w4}	Pulse duration, BUSY signal high			0.92	µs
t_{h1}	Hold time, First data bus data transition ($\overline{RD}$ low, or $\overline{CS}$ low for read cycle, or BYTE or BUS18/$\overline{16}$ input changes) after $\overline{CONVST}$ low	40			ns
t_{d1}	Delay time, $\overline{CS}$ low to $\overline{RD}$ low	0			ns
t_{su2}	Setup time, $\overline{RD}$ high to $\overline{CS}$ high	0			ns
t_{w5}	Pulse duration, $\overline{RD}$ low time	50			ns
t_{en}	Enable time, $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid			20	ns
t_{d2}	Delay time, data hold from $\overline{RD}$ high	5			ns
t_{d3}	Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid	10		20	ns
t_{w6}	Pulse duration, $\overline{RD}$ high	20			ns
t_{w7}	Pulse duration, $\overline{CS}$ high time	20			ns
t_{h2}	Hold time, last $\overline{RD}$ (or $\overline{CS}$ for read cycle) rising edge to $\overline{CONVST}$ falling edge	125			ns
t_{pd4}	Propagation delay time, BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge	Max(t_{d5})			ns
t_{d4}	Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew	0			ns
t_{su3}	Setup time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge	10			ns
t_{h3}	Hold time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge	10			ns
t_{dis}	Disable time, $\overline{RD}$ High ($\overline{CS}$ high for read cycle) to 3-stated data bus			20	ns
t_{d5}	Delay time, BUSY low to MSB data valid			30	ns
t_{su4}	Setup time, BYTE or BUS18/$\overline{16}$ change before BUSY falling edge	10		20	ns
t_{su5}	Setup time, BYTE transition to next BYTE transition, or BUS18/$\overline{16}$ transition to next BUS18/$\overline{16}$ transition	50			ns
$t_{su(AB)}$	Setup time, from the falling edge of $\overline{CONVST}$ (used to start the valid conversion) to the next falling edge of $\overline{CONVST}$ (when $\overline{CS}$ = 0 and $\overline{CONVST}$ used to abort) or to the next falling edge of $\overline{CS}$ (when $\overline{CS}$ is used to abort).	65		700	ns

(1) All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +VBD) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) See timing diagrams.
(3) All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

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TIMING CHARACTERISTICS

All specifications typical at –40°C to 85°C, +VA = 5 V, +VBD = 3 V (1)(2) (3)

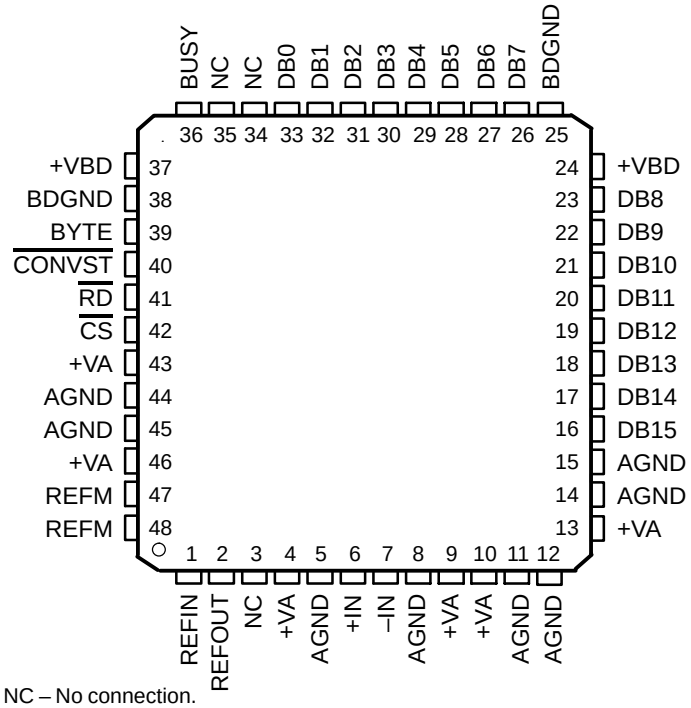
PARAMETER		MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time			0.92	µs
t_{ACQ}	Acquisition time	0.25			µs
t_{HOLD}	Sampling capacitor hold time			25	ns
t_{pd1}	$\overline{CONVST}$ low to conversion started (BUSY high)	10		50	ns
t_{pd2}	Propagation delay time, end of conversion to BUSY low	10		25	ns
t_{pd3}	Propagation delay time, from start of conversion (internal state) to rising edge of BUSY			25	ns
t_{w1}	Pulse duration, $\overline{CONVST}$ low	40			ns
t_{su1}	Setup time, $\overline{CS}$ low to $\overline{CONVST}$ low	20			ns
t_{w2}	Pulse duration, $\overline{CONVST}$ high	20			ns
	$\overline{CONVST}$ falling edge jitter			10	ps
t_{w3}	Pulse duration, BUSY signal low	Min(t_{ACQ})		1	µs
t_{w4}	Pulse duration, BUSY signal high			0.92	µs
t_{h1}	Hold time, first data bus transition ($\overline{RD}$ low, or $\overline{CS}$ low for read cycle, or BYTE or BUS 18/$\overline{16}$ input changes) after $\overline{CONVST}$ low	40			ns
t_{d1}	Delay time, $\overline{CS}$ low to $\overline{RD}$ low	0			ns
t_{su2}	Setup time, $\overline{RD}$ high to $\overline{CS}$ high	0			ns
t_{w5}	Pulse duration, $\overline{RD}$ low	50			ns
t_{en}	Enable time, $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid			30	ns
t_{d2}	Delay time, data hold from $\overline{RD}$ high	10			ns
t_{d3}	Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid	10		30	ns
t_{w6}	Pulse duration, $\overline{RD}$ high time	20			ns
t_{w7}	Pulse duration, $\overline{CS}$ high time	20			ns
t_{h2}	Hold time, last $\overline{RD}$ (or $\overline{CS}$ for read cycle) rising edge to $\overline{CONVST}$ falling edge	125			ns
t_{pd4}	Propagation delay time, BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge	Max(td5)			ns
t_{d4}	Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew	0			ns
t_{su3}	Setup time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge	10			ns
t_{h3}	Hold time, BYTE or BUS18/$\overline{16}$ transition to $\overline{RD}$ falling edge	10			ns
t_{dis}	Disable time, $\overline{RD}$ High ($\overline{CS}$ high for read cycle) to 3-stated data bus			30	ns
t_{d5}	Delay time, BUSY low to MSB data valid delay time			40	ns
t_{su4}	Setup time, BYTE or BUS18/$\overline{16}$ change before BUSY falling edge	10		30	ns
t_{su5}	Setup time, BYTE transition to next BYTE transition, or BUS18/$\overline{16}$ transition to next BUS18/$\overline{16}$ transition	50			ns
$t_{su(AB)}$	Setup time, from the falling edge of $\overline{CONVST}$ (used to start the valid conversion) to the next falling edge of $\overline{CONVST}$ (when $\overline{CS}$ = 0 and $\overline{CONVST}$ used to abort) or to the next falling edge of $\overline{CS}$ (when $\overline{CS}$ is used to abort).	70		700	ns

(1) All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +VBD) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) See timing diagrams.
(3) All timing are measured with 10 pF equivalent loads on all data bits and BUSY pins.

PRODUCT PREVIEW

PIN ASSIGNMENTS

PFB PACKAGE
(TOP VIEW)



NC – No connection.

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TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION		
AGND	5, 8, 11, 12, 14, 15, 44, 45	–	Analog ground		
BDGND	25, 38	–	Digital ground for bus interface digital supply		
BUSY	36	O	Status output. High when a conversion is in progress.		
BYTE	39	I	Byte select input. Used for 8-bit bus reading. 0: No fold back 1: Low byte D[7:0] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[15:8].		
$\overline{\text{CONVST}}$	40	I	Convert start. The falling edge of this input ends the acquisition period and starts the hold period.		
$\overline{\text{CS}}$	42	I	Chip select. The falling edge of this input starts the acquisition period.		
Data Bus			8-Bit Bus		16-Bit Bus
			BYTE = 0	BYTE = 1	BYTE = 0
DB15	16	O	D15 (MSB)	D7	D15 (MSB)
DB14	17	O	D14	D6	D14
DB13	18	O	D13	D5	D13
DB12	19	O	D12	D4	D12
DB11	20	O	D11	D3	D11
DB10	21	O	D10	D2	D10
DB9	22	O	D9	D1	D9
DB8	23	O	D8	D0 (LSB)	D8
DB7	26	O	D7	All ones	D7
DB6	27	O	D6	All ones	D6
DB5	28	O	D5	All ones	D5
DB4	29	O	D4	All ones	D4
DB3	30	O	D3	All ones	D3
DB2	31	O	D2	All ones	D2
DB1	32	O	D1	All ones	D1
DB0	33	O	D0 (LSB)	All ones	D0 (LSB)
–IN	7	I	Inverting input channel		
+IN	6	I	Non inverting input channel		
NC	2, 3, 34, 35	–	No connection		
REFIN	1	I	Reference input		
REFM	47, 48	I	Reference ground		
$\overline{\text{RD}}$	41	I	Synchronization pulse for the parallel output. When $\overline{\text{CS}}$ is low, this serves as the output enable and puts the previous conversion result on the bus.		
+VA	4, 9, 10, 13, 43, 46	–	Analog power supplies, 5-V dc		
+VBD	24, 37	–	Digital power supply for bus		

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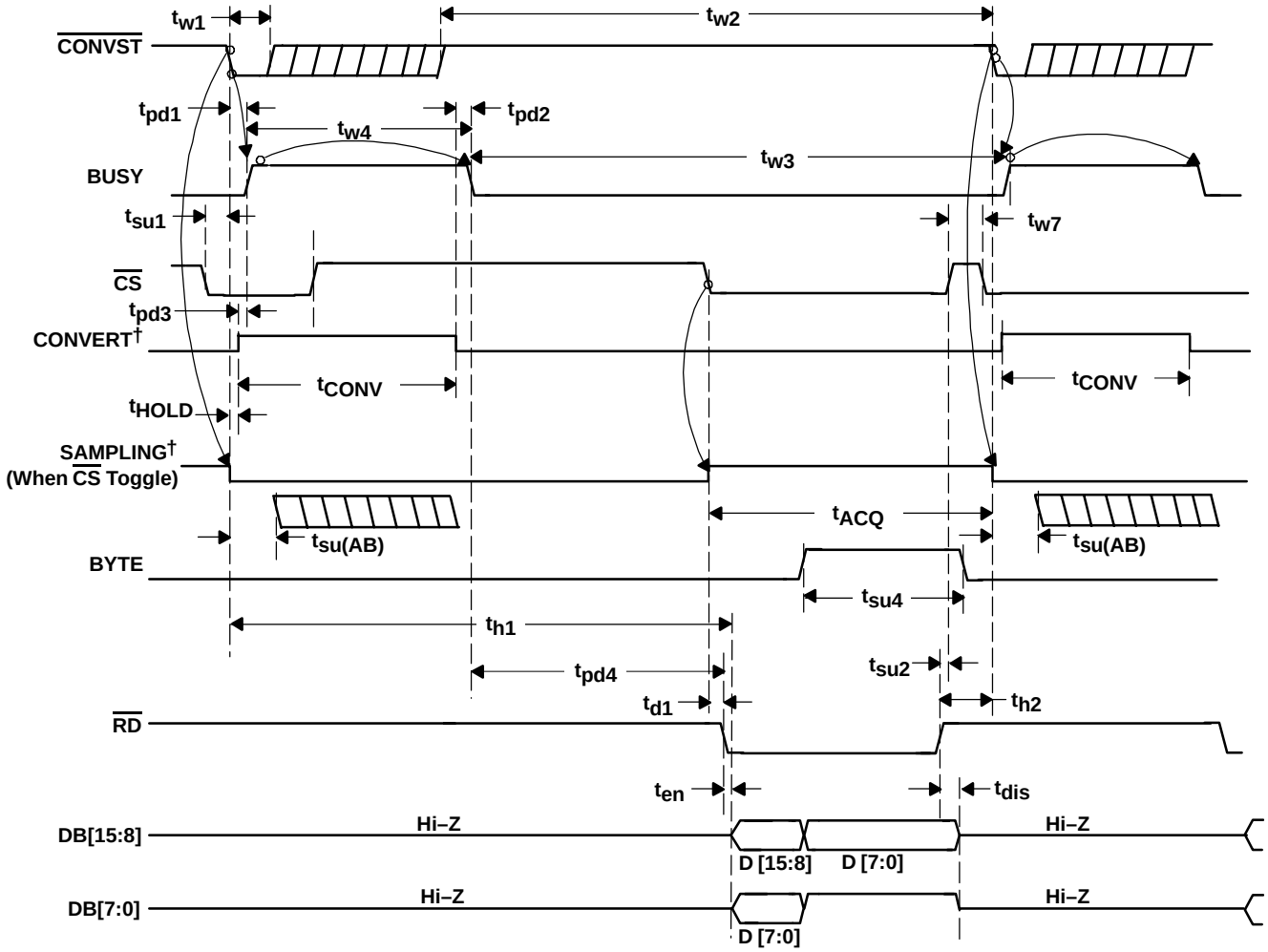
TIMING DIAGRAMS



†Signal internal to device

Figure 1. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ and $\overline{RD}$ Toggling

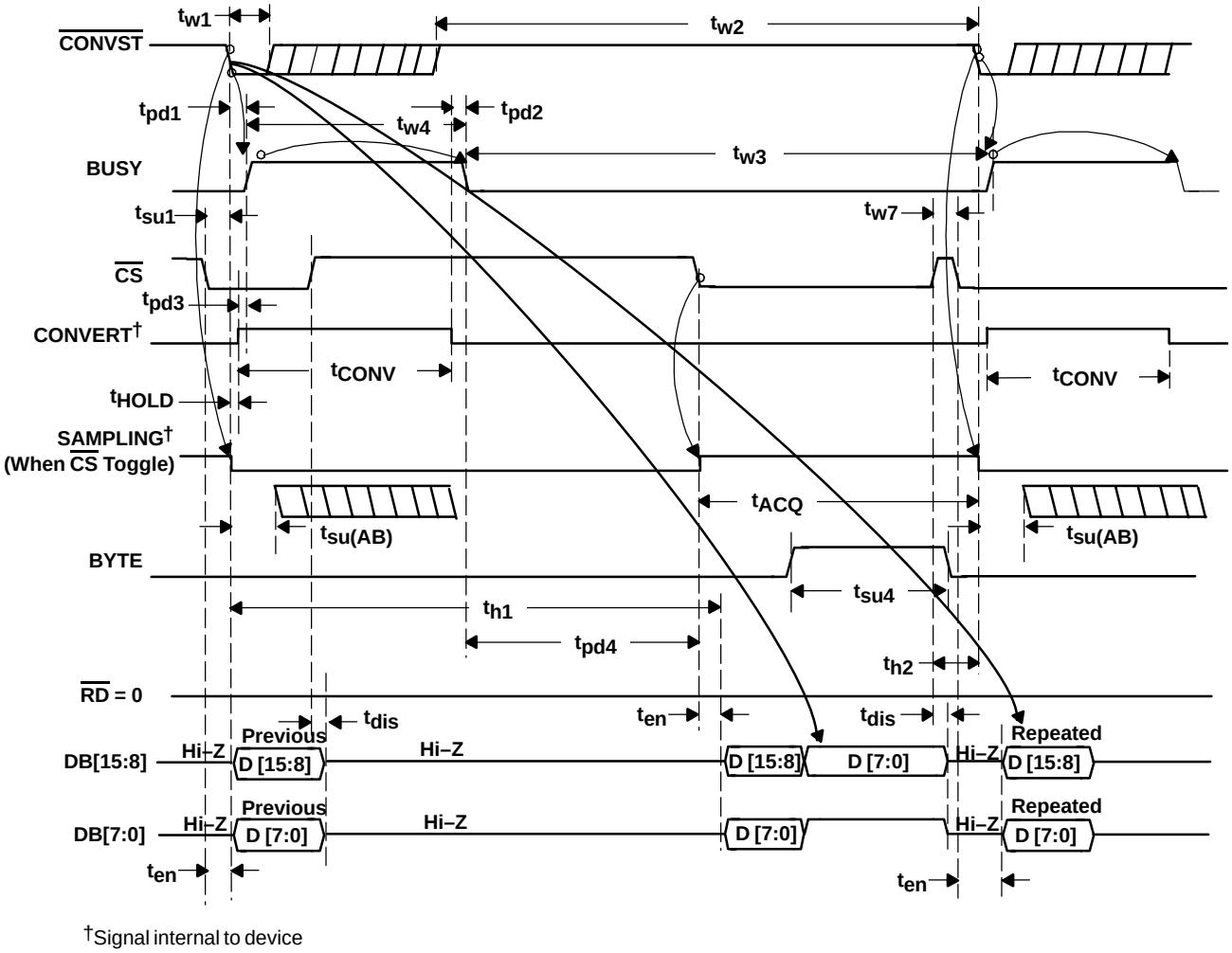


Figure 2. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ Toggling, $\overline{RD}$ Tied to BDGND

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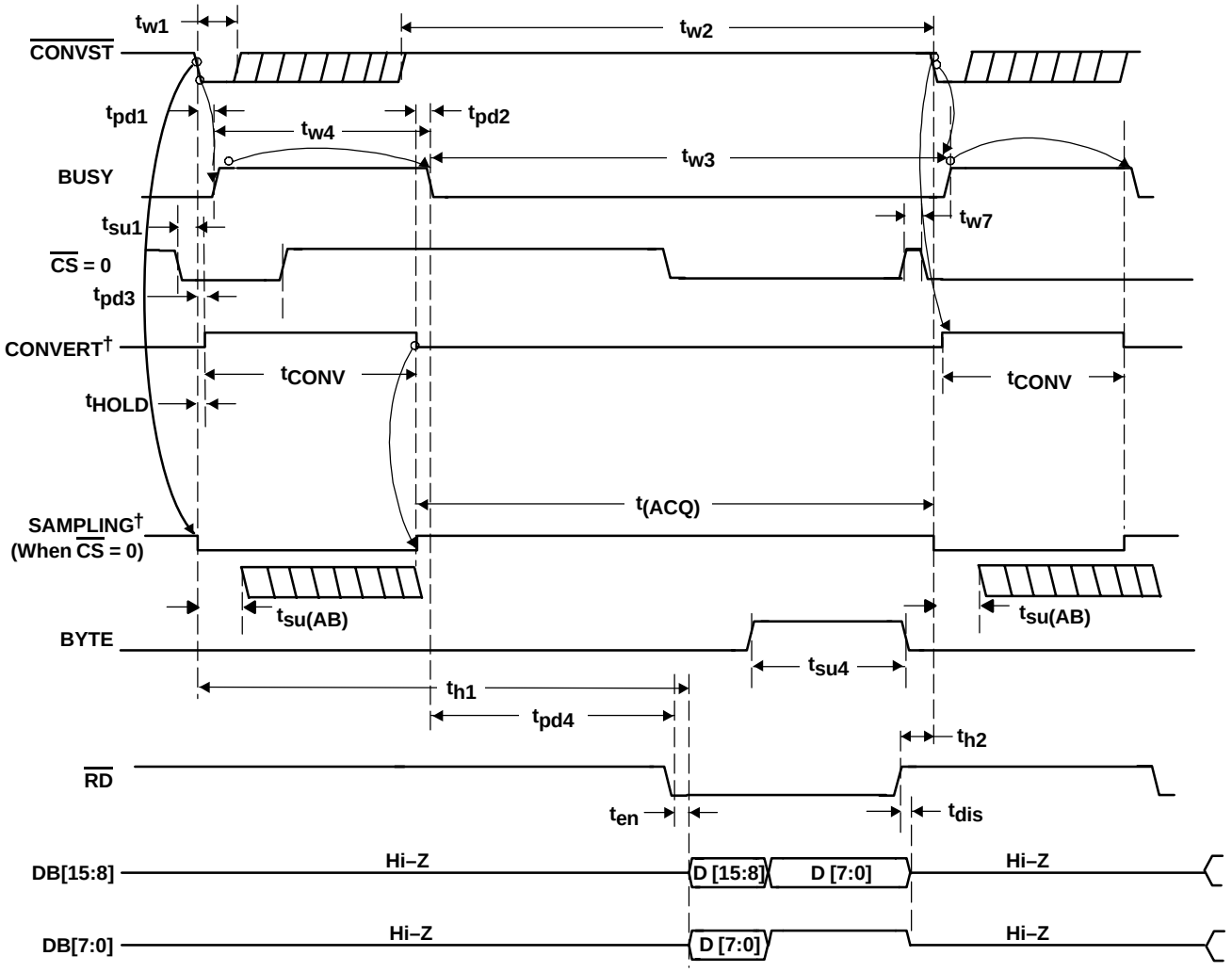
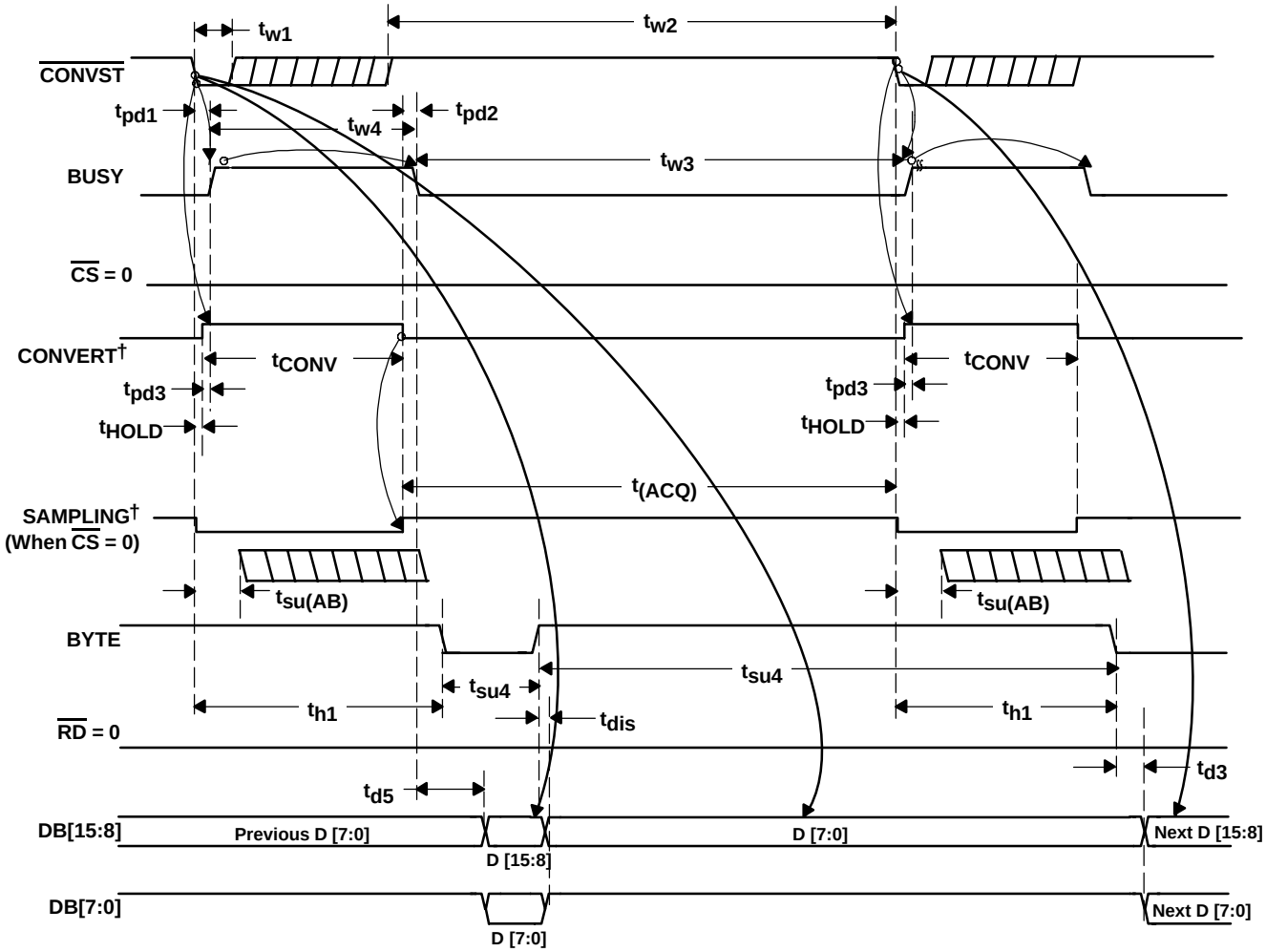


†Signal internal to device

Figure 3. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ Tied to BDGND, $\overline{RD}$ Toggling



†Signal internal to device

Figure 4. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ and $\overline{RD}$ Tied to BDGND—Auto Read

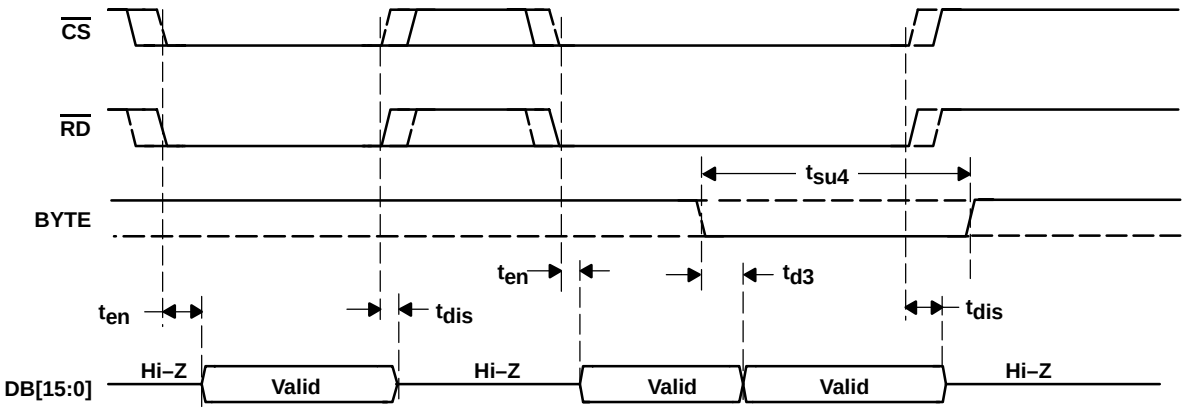


Figure 5. Detailed Timing for Read Cycles

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APPLICATION INFORMATION

MICROCONTROLLER INTERFACING

ADS8371 to 8-Bit Microcontroller Interface

Figure 6 shows a parallel interface between the ADS8371 and a typical microcontroller using the 8-bit data bus. The BUSY signal is used as a falling-edge interrupt to the microcontroller.

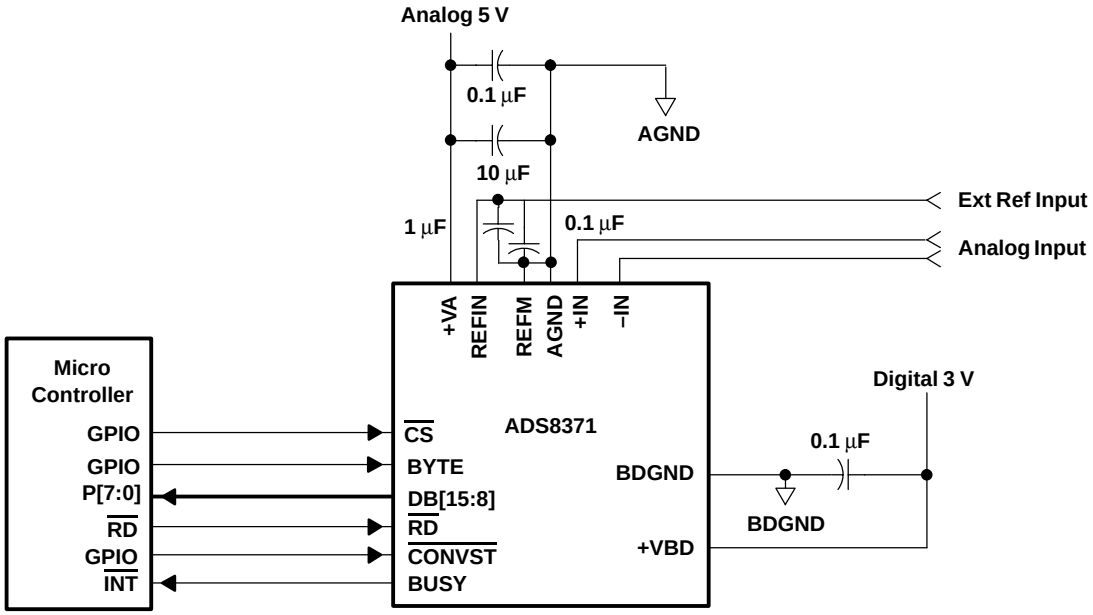

Figure 6. ADS8371 Application Circuitry

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

The ADS8371 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 6 for the application circuit for the ADS8371.

The conversion clock is generated internally. The conversion time of 0.92 μs is capable of sustaining a 850-kHz throughput.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8371 can operate with an external reference with a range from 2.5 V to 4.2 V.

ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.2 V and 0.2 V, allowing the input to reject small signals which are common to both the +IN and –IN inputs. The +IN input has a range of –0.2 V to V_{ref} + 0.2 V. The input span (+IN – (–IN)) is limited to 0 V to V_{ref}.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8371 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45 pF) to an 18-bit settling level within the acquisition time (400 ns) of the device. When the converter goes into the hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN and –IN inputs and the span (+IN – (–IN)) should be within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used.

Care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this is not observed, the two inputs could have different setting times. This may result in offset error, gain error, and linearity error which changes with temperature and input voltage.

DIGITAL INTERFACE

Timing And Control

See the timing diagrams in the specifications section for detailed information on timing signals and their requirements.

The ADS8371 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 20 ns (after the 20 ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high), while $\overline{\text{CS}}$ is low. The ADS8371 switches from the sample to the hold mode on the falling edge of the $\overline{\text{CONVST}}$ command. A clean and low jitter falling edge of this signal is important to the performance of the converter. The BUSY output is brought high immediately following $\overline{\text{CONVST}}$ going low. BUSY stays high throughout the conversion process and returns low when the conversion has ended.

Sampling starts with the falling edge of the BUSY signal when $\overline{\text{CS}}$ is tied low or starts with the falling edge of $\overline{\text{CS}}$ when BUSY is low.

Both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ can be high during and before a conversion with one exception ($\overline{\text{CS}}$ must be low when $\overline{\text{CONVST}}$ goes low to initiate a conversion). Both the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins are brought low in order to enable the parallel output bus with the conversion.

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Reading Data

The ADS8371 outputs full parallel data in straight binary format as shown in Table 1. The parallel output is active when $\overline{CS}$ and $\overline{RD}$ are both low. There is a minimal quiet zone requirement around the falling edge of $\overline{CONVST}$. This is 125 ns prior to the falling edge of $\overline{CONVST}$ and 40 ns after the falling edge. No data read should attempted within this zone. Any other combination of $\overline{CS}$ and $\overline{RD}$ sets the parallel output to 3-state. BYTE is used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. Refer to Table 1 for ideal output codes.

Table 1. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
FULL SCALE RANGE	V_{ref}		
Least significant bit (LSB)	V_{ref}/65536	BINARY CODE	HEX CODE
Full scale	V_{ref} – 1 LSB	1111 1111 1111 1111	FFFF
Midscale	V_{ref}/2	1000 0000 0000 0000	8000
Midscale – 1 LSB	V_{ref}/2 – 1 LSB	0111 1111 1111 1111	7FFF
Zero	0 V	0000 0000 0000 0000	0000

The output data is a full 16-bit word (D15–D0) on DB15–DB0 pins (MSB–LSB) if BYTE is low.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB15–DB8. In this case two reads are necessary: the first as before, leaving BYTE low and reading the 8 most significant bits on pins DB15–DB8, then bringing BYTE high. When BYTE is high, the low bits (D7–D0) appear on pins DB15–D8.

These multiword read operations can be done with multiple active $\overline{RD}$ (toggling) or with $\overline{RD}$ tied low for simplicity.

Table 2. Conversion Data Readout

BYTE	DATA READ OUT	
	DB15–DB8 PINS	DB7–DB0 PINS
High	D7–D0	All one's
Low	D15–D8	D7–D0

PRODUCT PREVIEW

RESET

The device can be reset through the use of the combination fo $\overline{CS}$ and $\overline{CONVST}$. Since the BUSY signal is held at high during the conversion, either one of these conditions triggers an internal self-clear reset to the converter.

- Issue a $\overline{CONVST}$ when $\overline{CS}$ is low and internal CONVERT state is high. The falling edge of $\overline{CONVST}$ starts a reset.
- Issue a $\overline{CS}$ (select the device) while internal CONVERT state is high. The falling edge of $\overline{CS}$ causes a reset.

Once the device is reset, all output latches are cleared (set to zeroes) and the BUSY signal is brought low. A new sampling period is started at the falling edge of the BUSY signal immediately after the instant of the internal reset.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8371 circuitry.

As the ADS8371 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are at least n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8371 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1-μF bypass capacitor is recommended from pin 1 (REFIN) directly to pin 48 (REFM). REFM and AGND should be shorted on the same ground plane under the device.

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8371 should be clean and well bypassed. A 0.1-μF ceramic bypass capacitor should be placed as close to the device as possible. See Table 3 for the placement of the capacitor. In addition, a 1-μF to 10-μF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-μF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

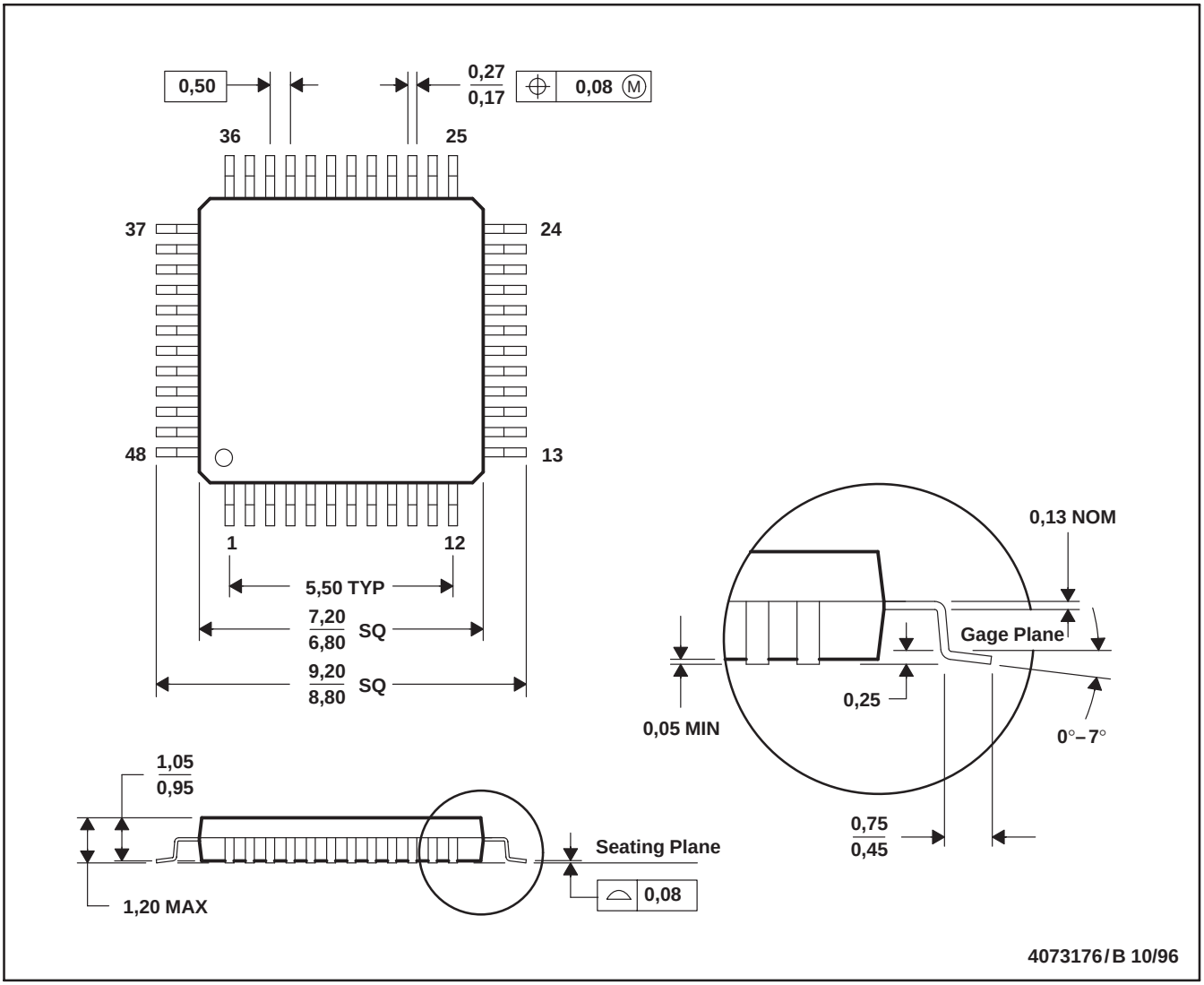
Table 3. Power Supply Decoupling Capacitor Placement

POWER SUPPLY PLANE SUPPLY PINS	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE
Pin pairs that require shortest path to decoupling capacitors	(4,5), (8,9), (10,11), (13,15), (43,44), (45,46)	(24,25)
Pins that require no decoupling	12, 14	37, 38

PRODUCT PREVIEW

MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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