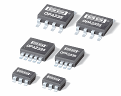
Burr-Brown Products
from Texas Instruments

OPA334
OPA2334
OPA335
OPA2335



SBOS245D – JUNE 2002 – REVISED JULY 2003

0.05μV/°C max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zerø-Drift Series

FEATURES

- LOW OFFSET VOLTAGE: 5μV (max)
- ZERO DRIFT: 0.05μV/°C (max)
- QUIESCENT CURRENT: 285μA
- SINGLE-SUPPLY OPERATION
- SINGLE AND DUAL VERSIONS
- SHUTDOWN
- *Micro*SIZE PACKAGES

APPLICATIONS

- TRANSDUCER APPLICATIONS
- TEMPERATURE MEASUREMENT
- ELECTRONIC SCALES
- MEDICAL INSTRUMENTATION
- BATTERY-POWERED INSTRUMENTS
- HANDHELD TEST EQUIPMENT

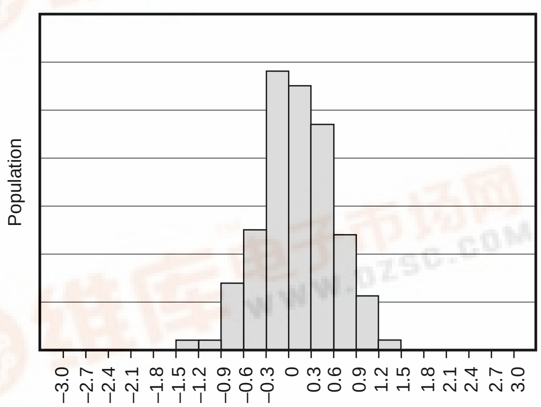
DESCRIPTION

The OPA334 and OPA335 series of CMOS operational amplifiers use auto-zeroing techniques to simultaneously provide very low offset voltage (5μV max), and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing. Single or dual supplies as low as +2.7V (±1.35V) and up to +5.5V (±2.75V) may be used. These op amps are optimized for low-voltage, single-supply operation.

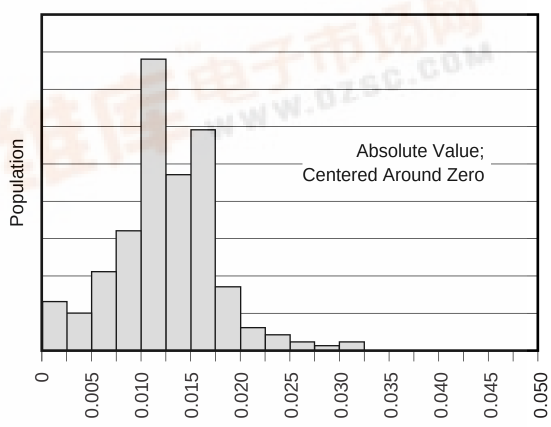
The OPA334 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current of 2μA. When the Enable pin is connected high, the amplifier is active. Connecting Enable low disables the amplifier, and places the output in a high-impedance state.

The OPA334 (single version with shutdown) comes in *Micro*SIZE SOT23-6. The OPA335 (single version without shutdown) is available in SOT23-5, and SO-8. The OPA2334 (dual version with shutdown) comes in *Micro*SIZE MSOP-10. The OPA2335 (dual version without shutdown) is offered in the MSOP-8 and SO-8 packages. All versions are specified for operation from –40°C to +125°C.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+7V
Signal Input Terminals, Voltage(2)	–0.5V to (V+) + 0.5V
Current(2)	±10mA
Output Short Circuit(3)	Continuous
Operating Temperature	–40°C to +150°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these, or any other conditions beyond those specified, is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

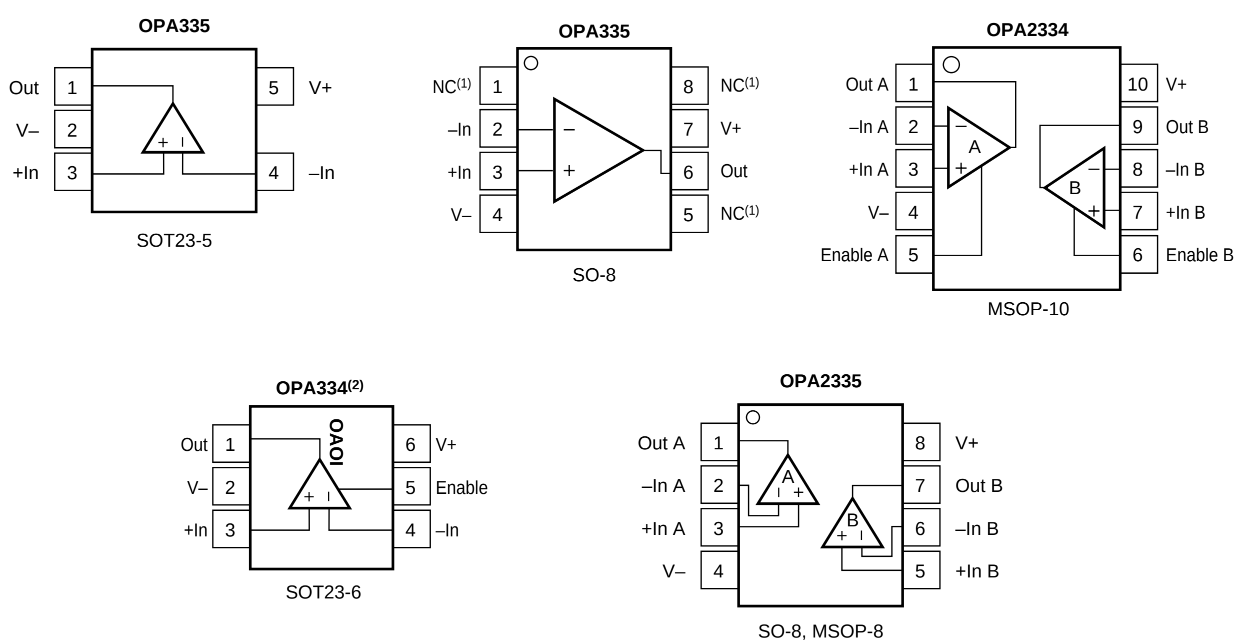
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Shutdown Version						
OPA334	SOT23-6	DBV	–40°C to +125°C	OAOI	OPA334AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA334AIDBVR	Tape and Reel, 3000
OPA2334	MSOP-10	DGS	–40°C to +125°C	BHE	OPA2334AIDGST	Tape and Reel, 250
"	"	"	"	"	OPA2334AIDGSR	Tape and Reel, 2500
Non-Shutdown Version						
OPA335	SOT23-5	DBV	–40°C to +125°C	OAPI	OPA335AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA335AIDBVR	Tape and Reel, 3000
OPA335	SO-8	D	–40°C to +125°C	OPA335	OPA335AID	Rails, 100
"	"	"	"	"	OPA335AIDR	Tape and Reel, 2500
OPA2335	SO-8	D	–40°C to +125°C	OPA2335	OPA2335AID	Rails, 100
"	"	"	"	"	OPA2335AIDR	Tape and Reel, 2500
OPA2335	MSOP-8	DGK	–40°C to +125°C	BHF	OPA2335AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA2335AIDGKR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATIONS



NOTES: (1) NC indicates no internal connection. (2) Pin 1 of the SOT23-6 is determined by orienting the package marking as indicated in the diagram.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, T_A = –40°C to +125°C.

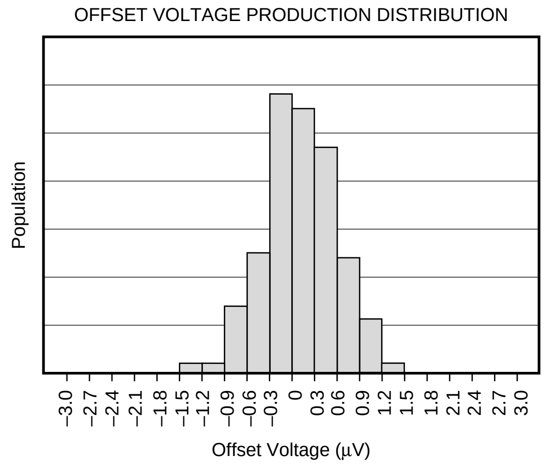
At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

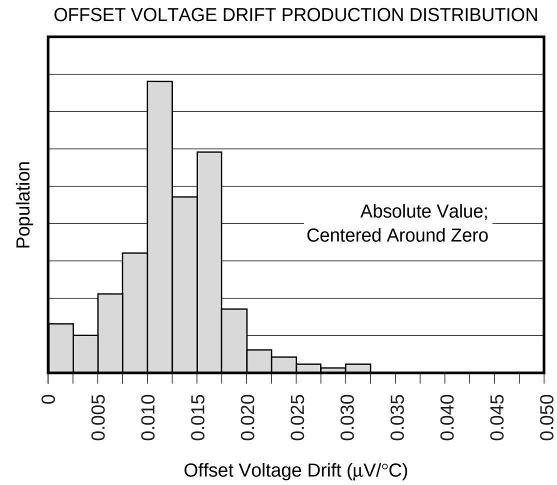
PARAMETER		CONDITION	OPA334AI, OPA335AI OPA2334AI, OPA2335AI MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_{CM} = V_S/2		1	5	μV
vs Temperature	**dV_{OS}/dT**			**±0.02**	**±0.05**	**μV/°C**
vs Power Supply	**PSRR**	**V_S = +2.7V to +5.5V, V_{CM} = 0, Over Temperature**		**±1**	**±2**	**μV/V**
Long-Term Stability(1)				See Note (1)		
Channel Separation, dc				0.1		μV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = V_S/2		±70	±200	pA
Over Temperature				**1**		**nA**
Input Offset Current	I_{OS}			±120	±400	pA
NOISE						
Input Voltage Noise, f = 0.01Hz to 10Hz	e_n			1.4		μV_{PP}
Input Current Noise Density, f = 10Hz	i_n			20		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	**V_{CM}**		**(V–) – 0.1**		**(V+) – 1.5**	**V**
Common-Mode Rejection Ratio	**CMRR**	**(V–) – 0.1V < V_{CM} < (V+) – 1.5V, Over Temperature**	**110**	**130**		**dB**
INPUT CAPACITANCE						
Differential				1		pF
Common-Mode				5		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain, Over Temperature	**A_{OL}**	**50mV < V_O < (V+) – 50mV, R_L = 100kΩ, V_{CM} = V_S/2**	**110**	**130**		**dB**
Over Temperature		**100mV < V_O < (V+) – 100mV, R_L = 10kΩ, V_{CM} = V_S/2**	**110**	**130**		**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			2		MHz
Slew Rate	SR	G = +1		1.6		V/μs
OUTPUT						
Voltage Output Swing from Rail		**R_L = 10kΩ, Over Temperature**		**15**	**100**	**mV**
Voltage Output Swing from Rail		**R_L = 100kΩ, Over Temperature**		**1**	**50**	**mV**
Short-Circuit Current	I_{SC}			±50		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			
SHUTDOWN						
t_{OFF}				1		μs
t_{ON}(2)				150		μs
V_L (shutdown)			0		+0.8	V
V_H (amplifier is active)			0.75 (V+)		5.5	V
Input Bias Current of Enable Pin				50		pA
I_{QSD}					2	μA
POWER SUPPLY						
Operating Voltage Range			2.7		5.5	V
Quiescent Current: OPA334, OPA335	I_Q	I_O = 0		285	350	μA
Over Temperature					**450**	**μA**
OPA2334, OPA2335 (total—two amplifiers)		I_O = 0		570	700	μA
Over Temperature					**900**	**μA**
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–40		+150	°C
Storage Range			–65		+150	°C
Thermal Resistance	θ_{JA}					°C/W
SOT23-5, SOT23-6 Surface-Mount				200		°C/W
MSOP-8, MSOP-10, SO-8 Surface-Mount				150		°C/W

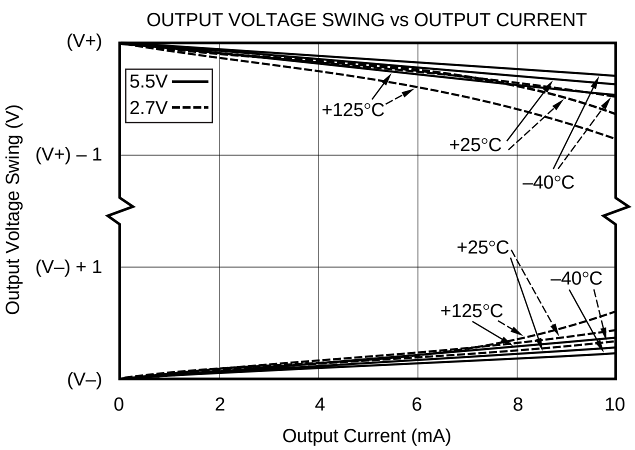
NOTES: (1) 500-hour life test at 150°C demonstrated randomly distributed variation approximately equal to measurement repeatability of 1μV. (2) Device requires one complete cycle to return to V_{OS} accuracy.

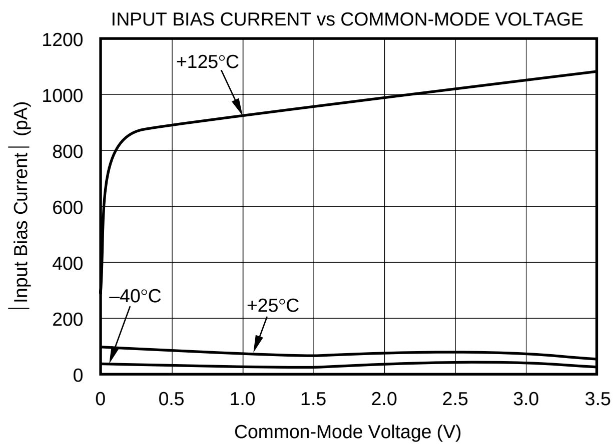
TYPICAL CHARACTERISTICS

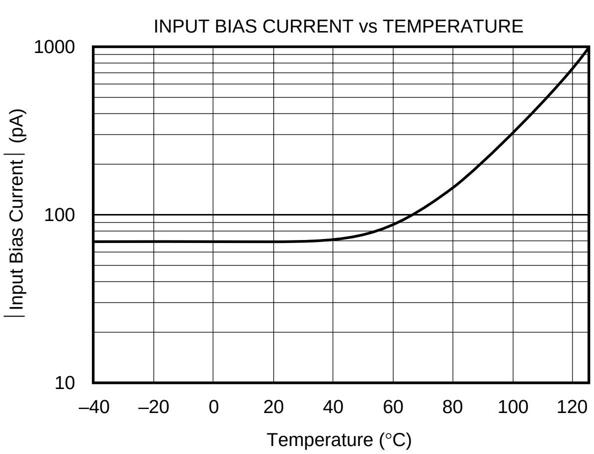
At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

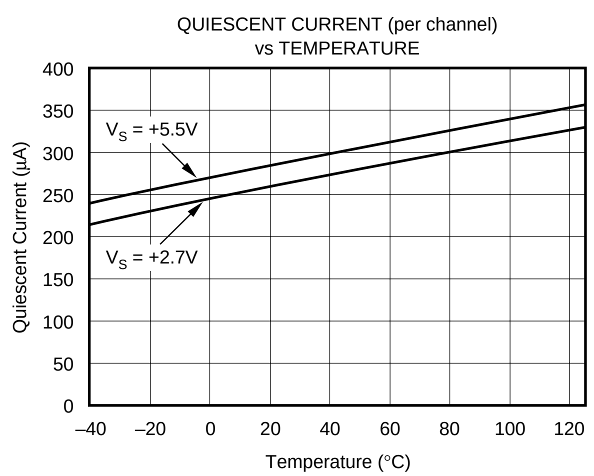








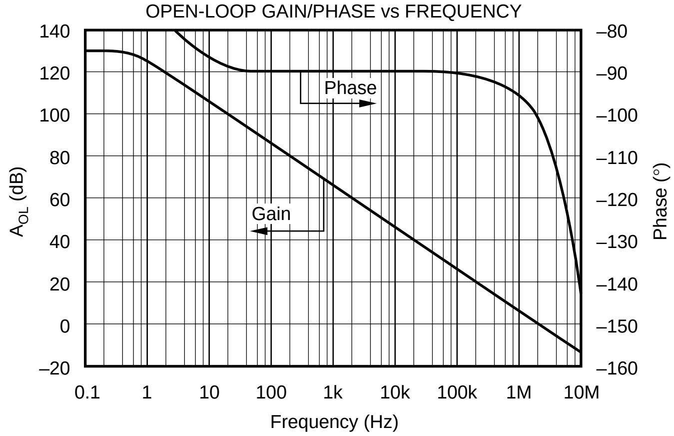




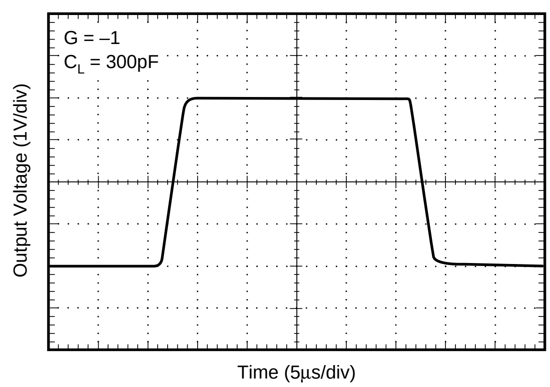
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

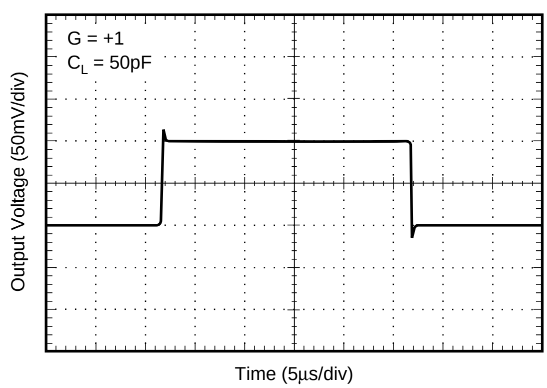
OPEN-LOOP GAIN/PHASE vs FREQUENCY



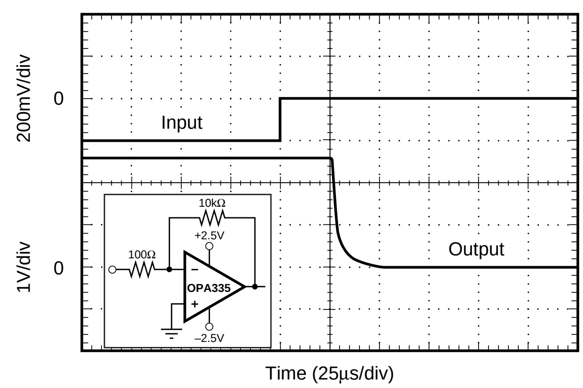
LARGE-SIGNAL RESPONSE



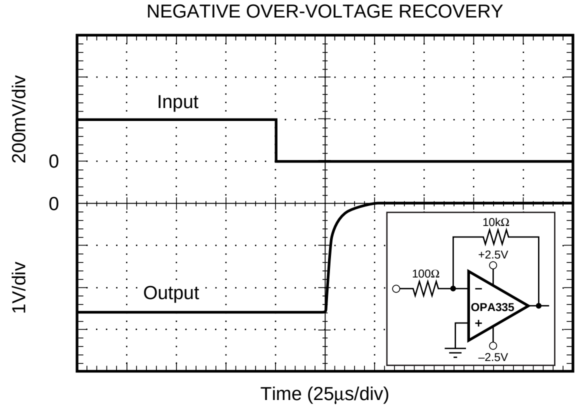
SMALL-SIGNAL RESPONSE



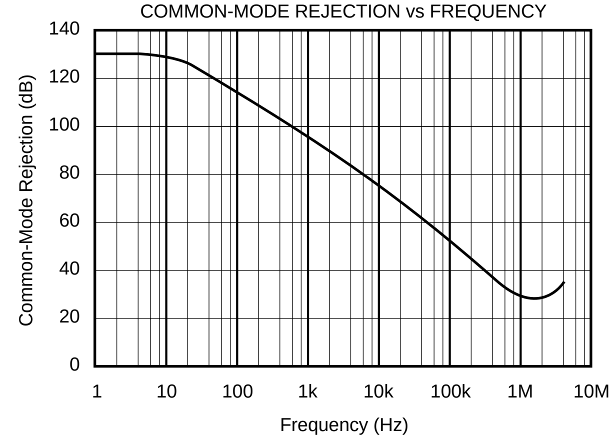
POSITIVE OVER-VOLTAGE RECOVERY



NEGATIVE OVER-VOLTAGE RECOVERY



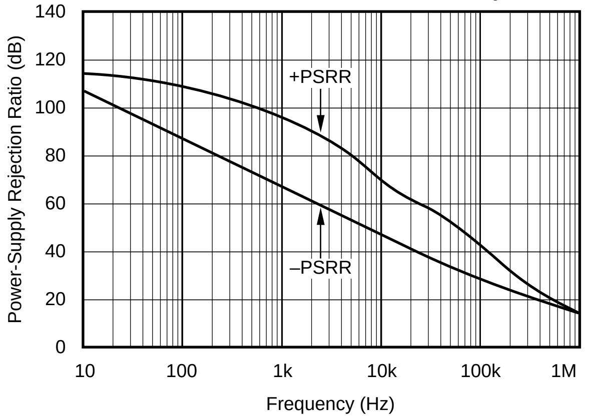
COMMON-MODE REJECTION vs FREQUENCY



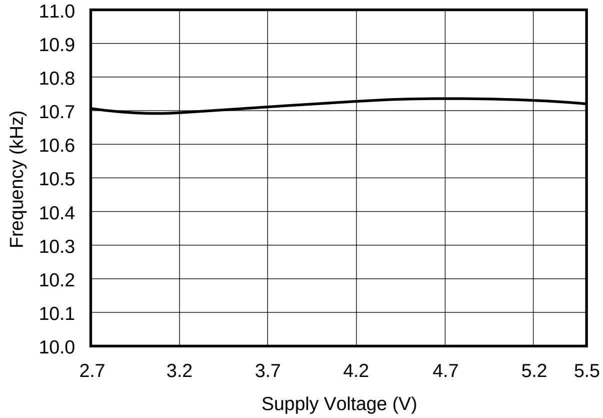
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

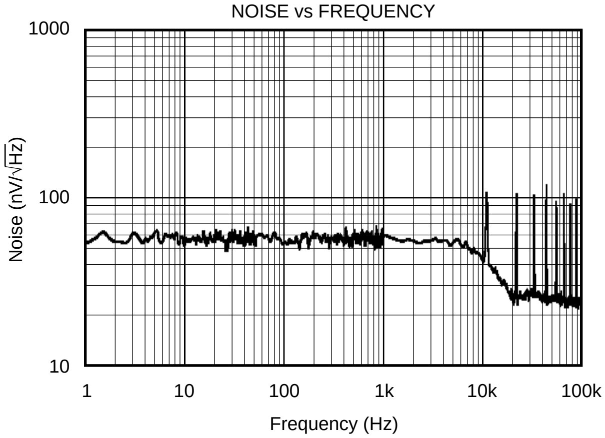
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



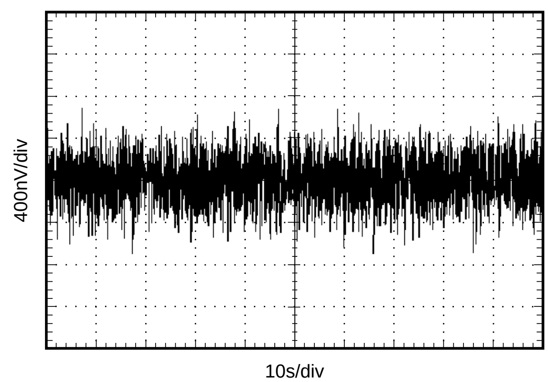
SAMPLING FREQUENCY vs SUPPLY VOLTAGE



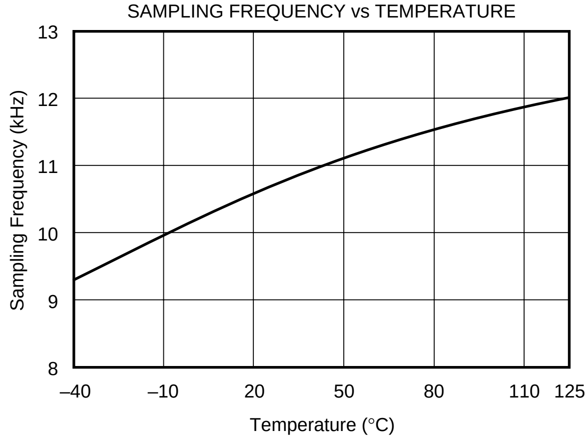
NOISE vs FREQUENCY



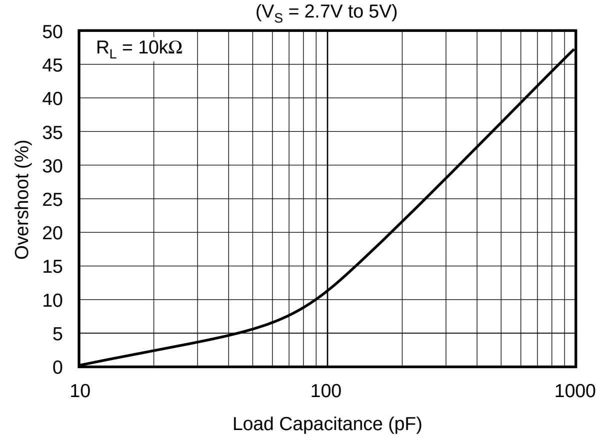
0.01Hz TO 10Hz NOISE



SAMPLING FREQUENCY vs TEMPERATURE



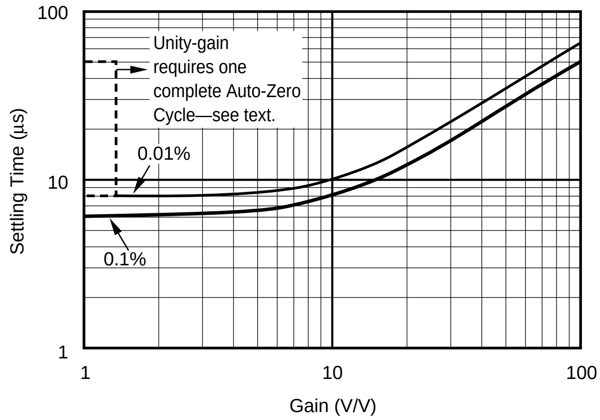
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE
(V_S = 2.7V to 5V)



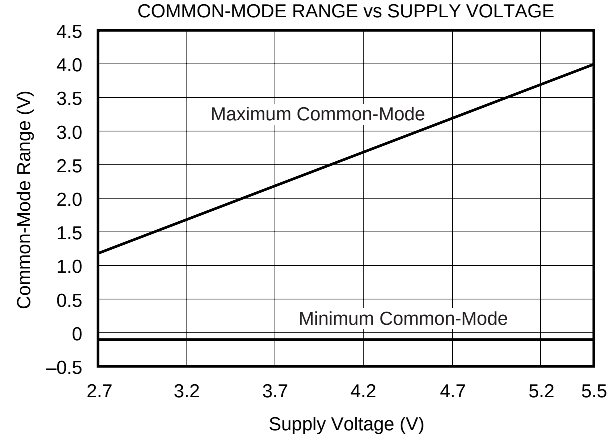
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

SETTLING TIME vs CLOSED-LOOP GAIN



COMMON-MODE RANGE vs SUPPLY VOLTAGE



APPLICATIONS INFORMATION

The OPA334 and OPA335 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a 0.1µF capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1µV/°C or higher, depending on materials used.

OPERATING VOLTAGE

The OPA334 and OPA335 series op amps operate over a power-supply range of +2.7V to +5.5V (±1.35V to ±2.75V). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

OPA334 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the V– supply voltage of the amp. A logic high enables the op amp. A valid logic high is defined as > 75% of the total supply voltage. The valid logic high signal can be up to 5.5V above the negative supply, independent of the positive supply voltage. A valid logic low is defined as < 0.8V above the V– supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin must be connected to a valid high or low voltage, or driven, not left open circuit.

The logic input is a high-impedance CMOS input, with separate logic inputs provided on the dual version. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time is 150µs, which includes one full auto-zero cycle required by the amplifier to return to V_{OS} accuracy. Prior to this time, the amplifier functions properly, but with unspecified offset voltage.

Disable time is 1µs. When disabled, the output assumes a high-impedance state. This allows the OPA334 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

INPUT VOLTAGE

The input common-mode range extends from (V–) – 0.1V to (V+) – 1.5V. For normal operation, the inputs must be limited to this range. The common-mode rejection ratio is only valid within the valid input common-mode range. A lower supply voltage results in lower input common-mode range; therefore, attention to these values must be given when selecting the input bias voltage. For example, when operating on a single 3V power supply, common-mode range is from 0.1V below ground to half the power-supply voltage.

Normally, input bias current is approximately 70pA; however, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 1.

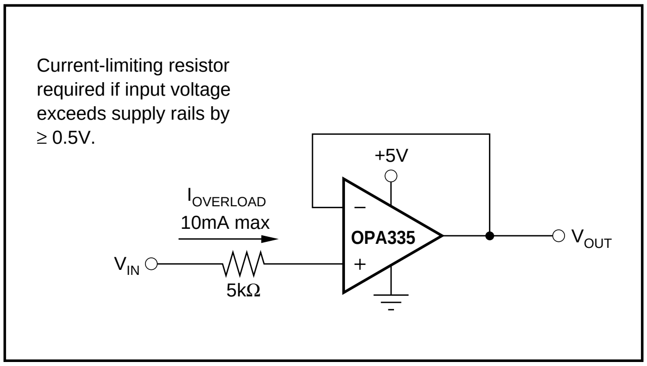


FIGURE 1. Input Current Protection.

INTERNAL OFFSET CORRECTION

The OPA334 and OPA335 series op amps use an auto-zero topology with a time-continuous 2MHz op amp in the signal path. This amplifier is zero-corrected every 100µs using a proprietary technique. Upon power-up, the amplifier requires one full auto-zero cycle of approximately 100µs to achieve specified V_{OS} accuracy. Prior to this time, the amplifier functions properly but with unspecified offset voltage.

This design has remarkably little aliasing and noise. Zero correction occurs at a 10kHz rate, but there is virtually no fundamental noise energy present at that frequency. For all practical purposes, any glitches have energy at 20MHz or higher and are easily filtered, if required. Most applications are not sensitive to such high-frequency noise, and no filtering is required.

Unity-gain operation demands that the auto-zero circuitry correct for common-mode rejection errors of the main amplifier. Because these errors can be larger than 0.01% of a full-scale input step change, one calibration cycle (100µs) can be required to achieve full accuracy. This behavior is shown in the typical characteristic section, see *Settling Time vs Closed-Loop Gain*.

ACHIEVING OUTPUT SWING TO THE OP AMP'S NEGATIVE RAIL

Some applications require output voltage swing from 0V to a positive full-scale voltage (such as +2.5V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA334 or OPA335 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires use of another resistor and an additional, more negative, power supply than the op amp's negative supply. A pull-down resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 2.

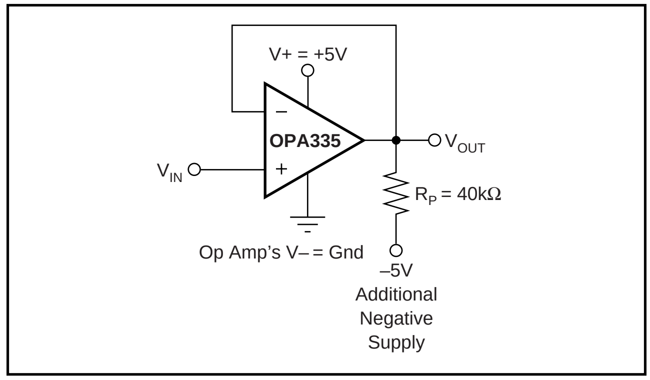


FIGURE 2. Op Amp with Pull-Down Resistor to Achieve V_{OUT} = Ground.

The OPA334 and OPA335 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below using the above technique. This technique only works with some types of output stages. The OPA334 and OPA335 have been characterized to perform well with this technique. Accuracy is excellent down to 0V and as low as –2mV. Limiting and non-linearity occurs below –2mV, but excellent accuracy returns as the output is again driven above –2mV. Lowering the resistance of the pull-down resistor will allow the op amp to swing even further below the negative rail. Resistances as low as 10kΩ can be used to achieve excellent accuracy down to –10mV.

LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1µF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility.

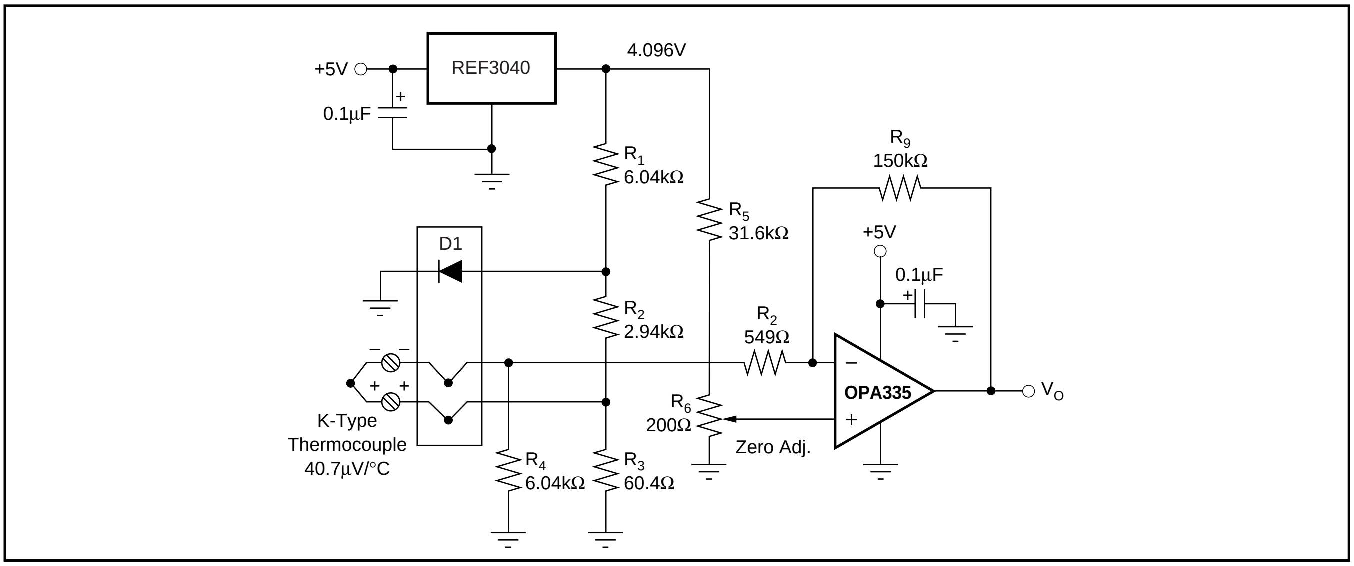


FIGURE 3. Temperature Measurement Circuit.

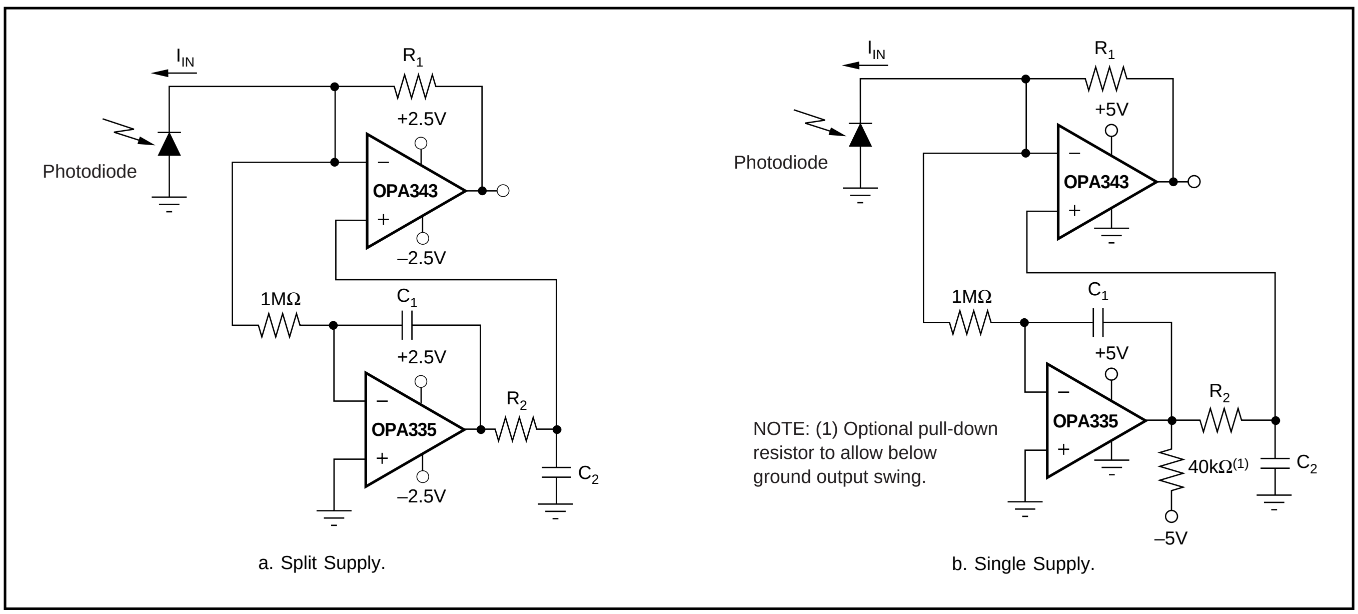


FIGURE 4. Auto-Zeroed Transimpedance Amplifier.

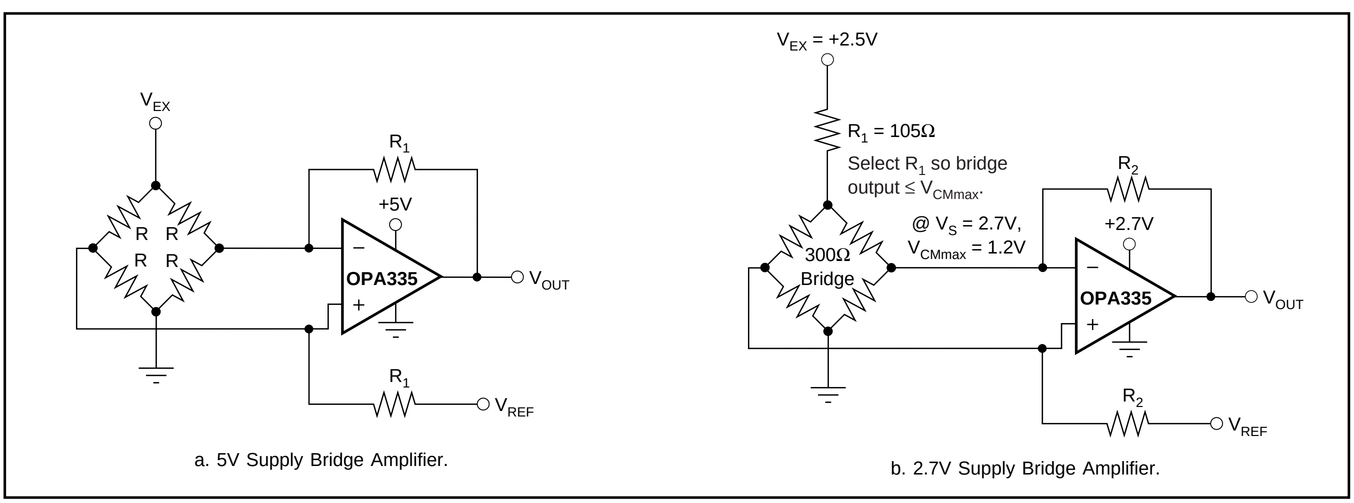


FIGURE 5. Single Op Amp Bridge Amplifier Circuits.

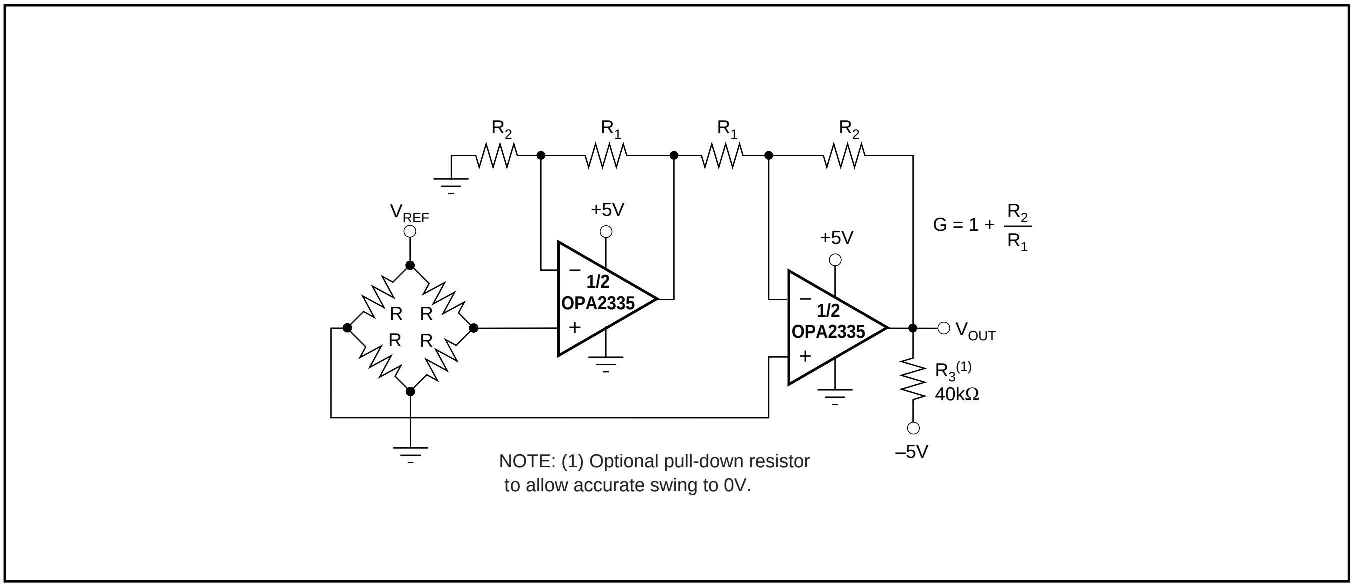


FIGURE 6. Dual Op Amp IA Bridge Amplifier.

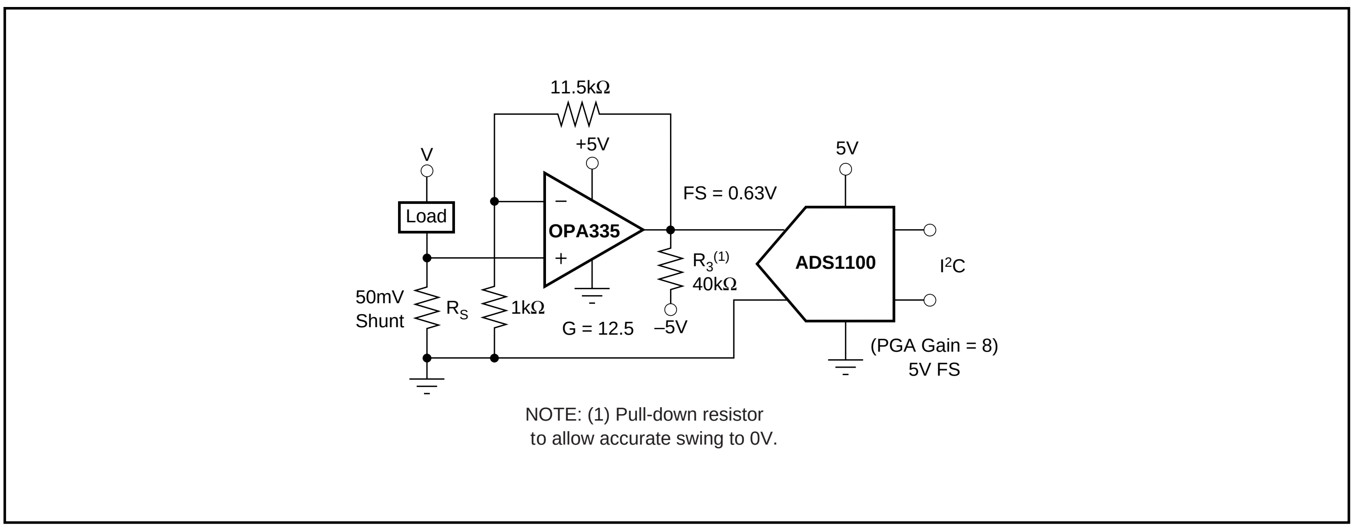


FIGURE 7. Low-Side Current Measurement.

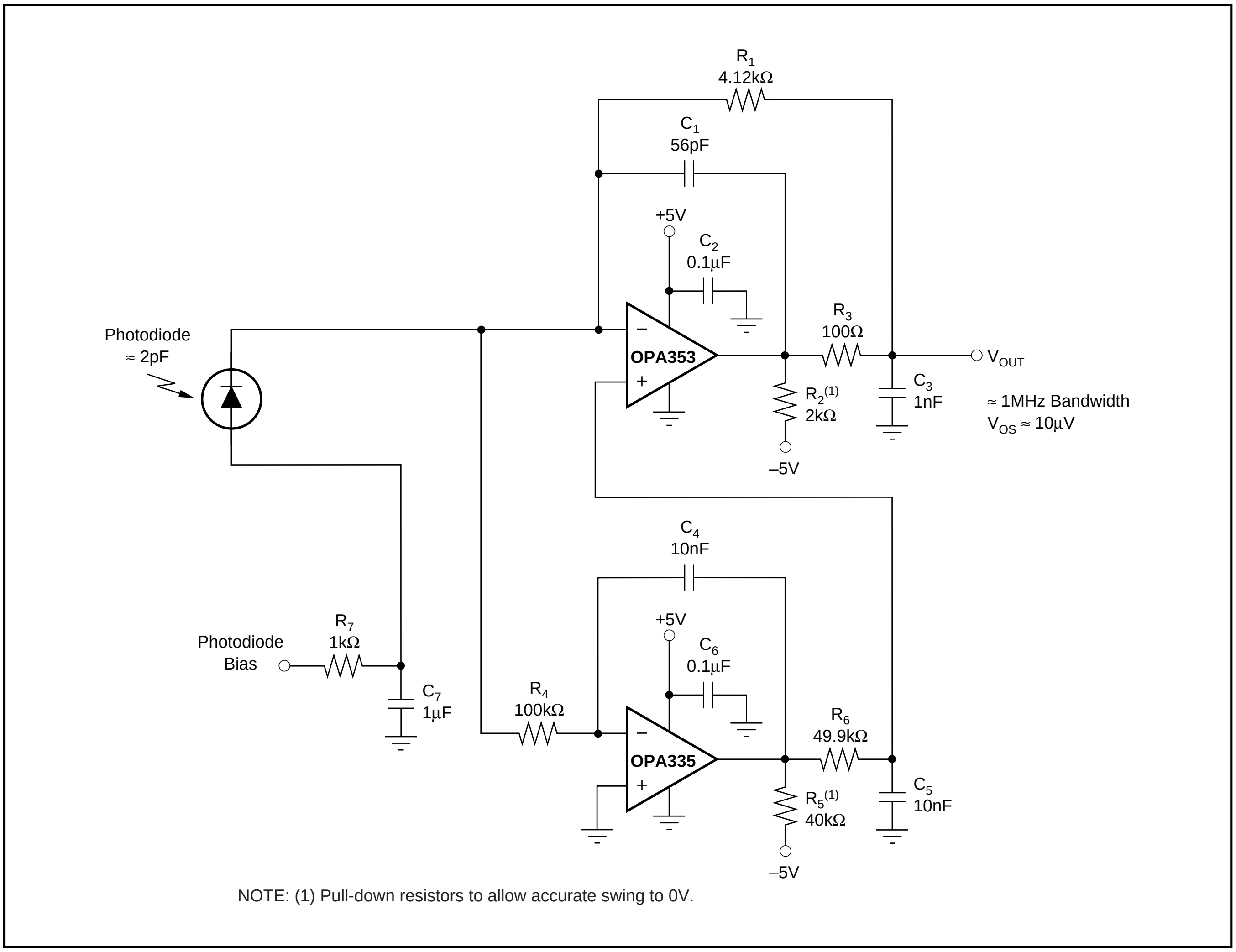
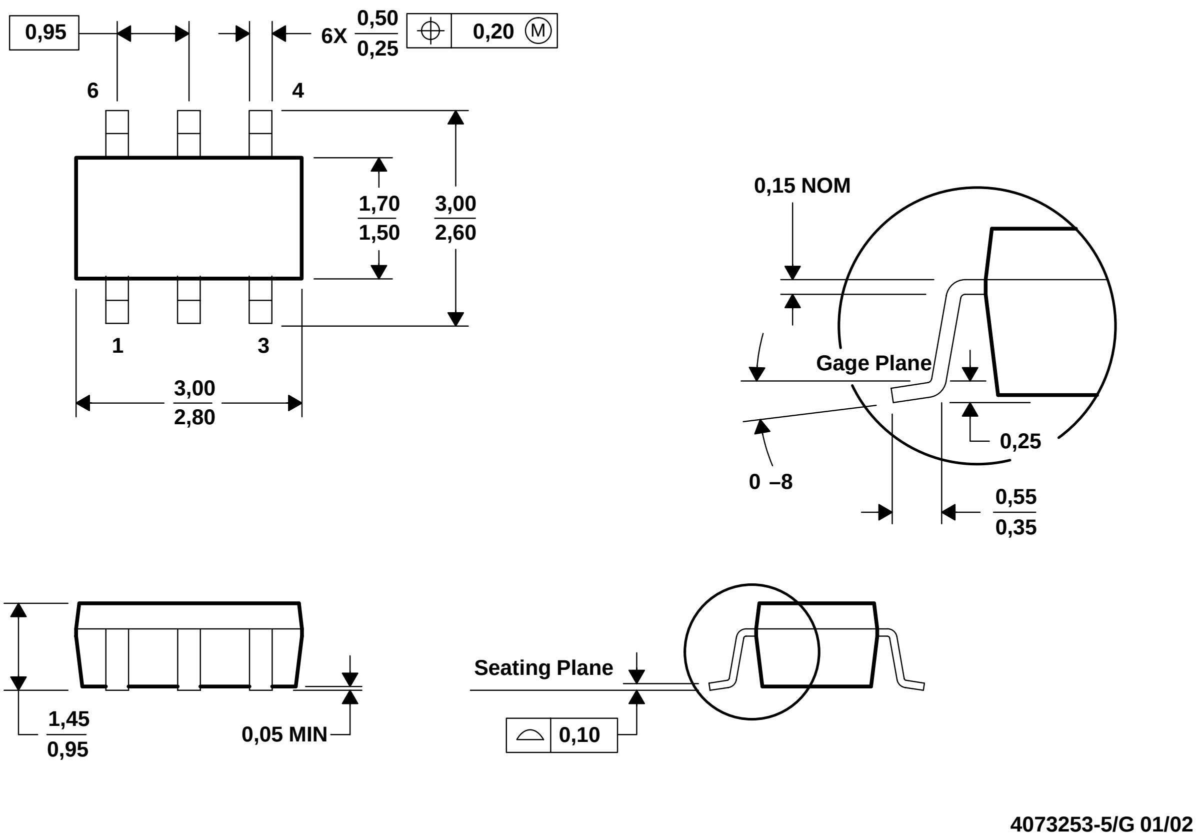


FIGURE 8. High Dynamic Range Transimpedance Amplifier.

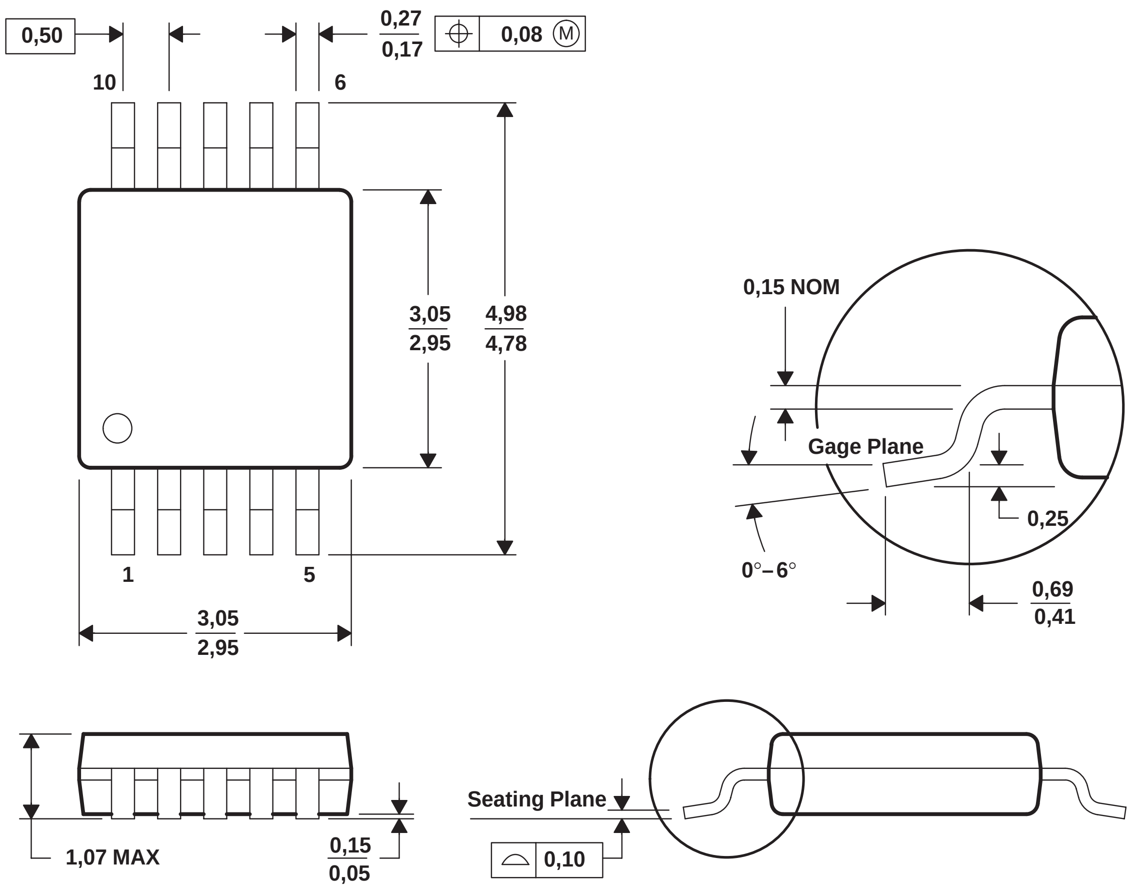
DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

PACKAGE DRAWINGS (Cont.)

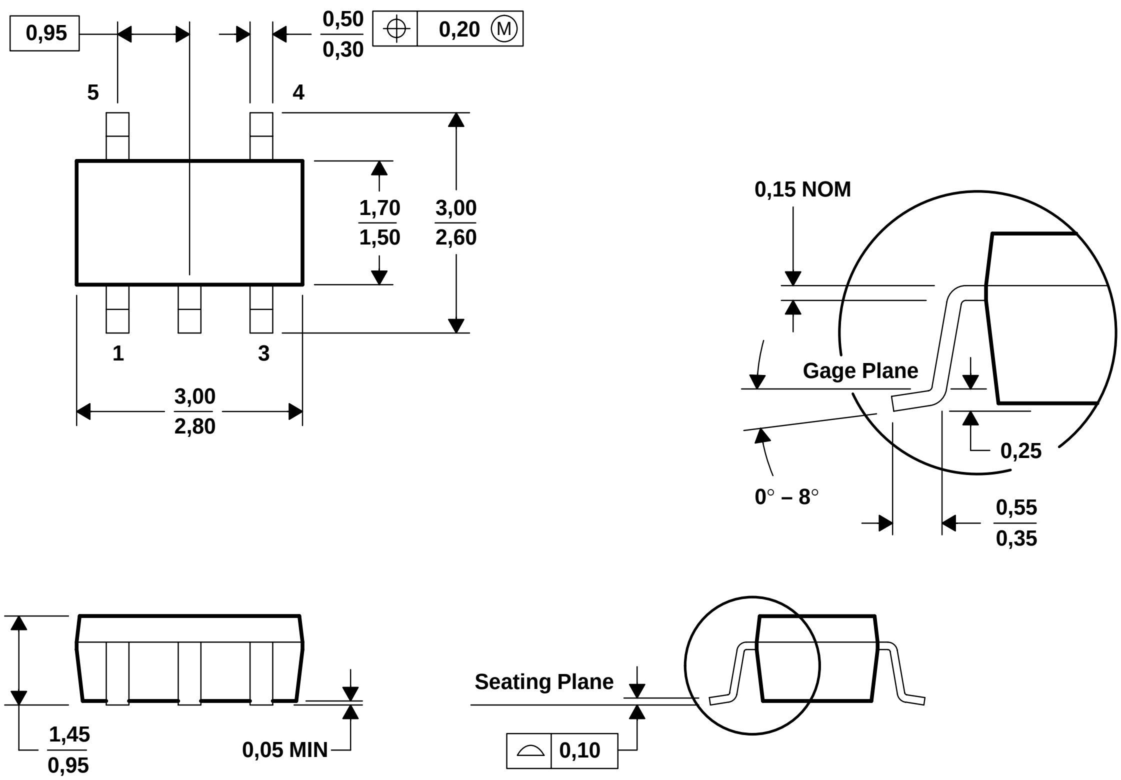
DGS (S-PDSO-G10) **PLASTIC SMALL-OUTLINE PACKAGE**



4073272/B 08/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
A. Falls within JEDEC MO-187

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**

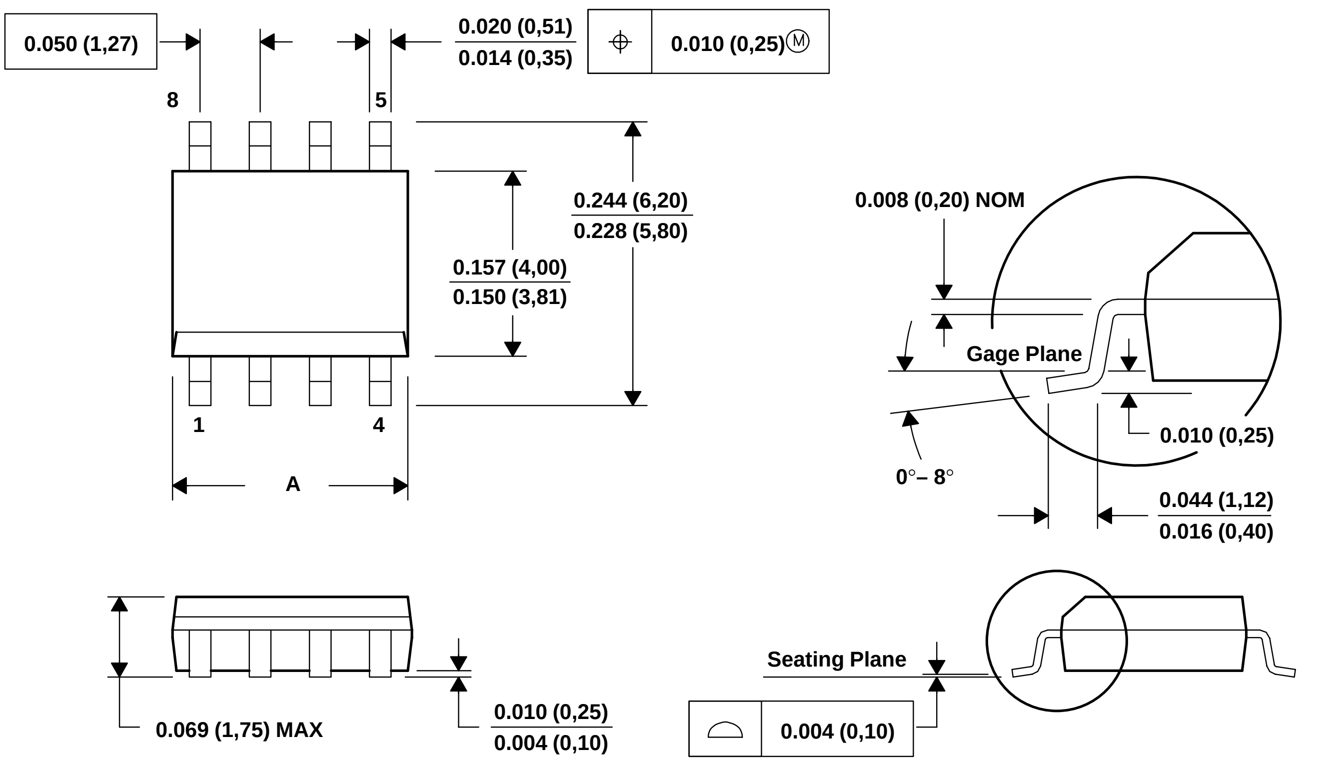


4073253-4/G 01/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

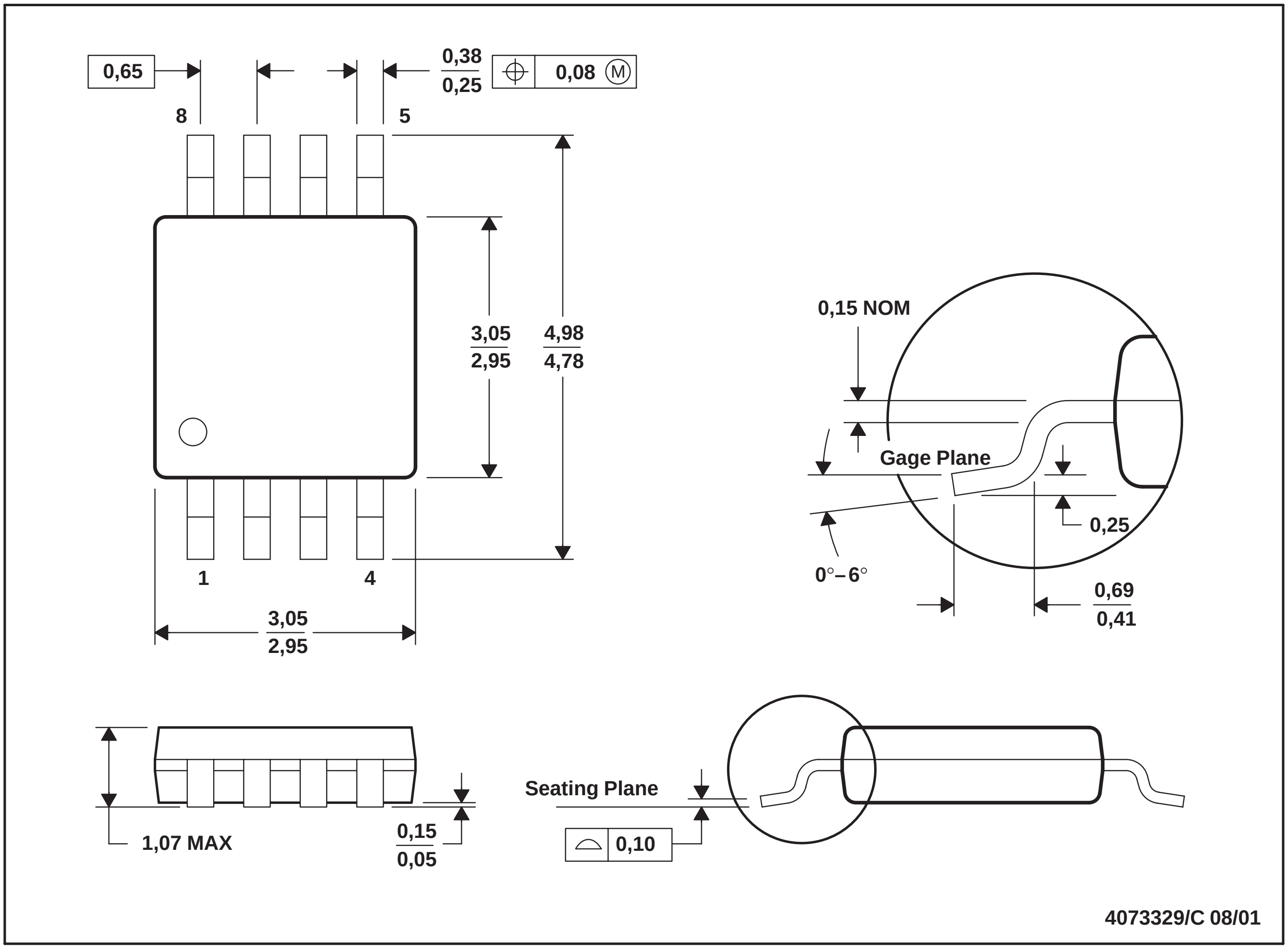


PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-187

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