

SBOS167C – NOVEMBER 2000– REVISED JUNE 2003

microPower, Rail-to-Rail Operational Amplifiers

FEATURES

- **LOW I_Q :** 20 μ A
- **microSIZE PACKAGES:** WCSP-8, SC70-5, SOT23-5, SOT23-8, and TSSOP-14
- **HIGH SPEED/POWER RATIO WITH BANDWIDTH:** 350kHz
- **RAIL-TO-RAIL INPUT AND OUTPUT**
- **SINGLE SUPPLY:** 2.3V to 5.5V

APPLICATIONS

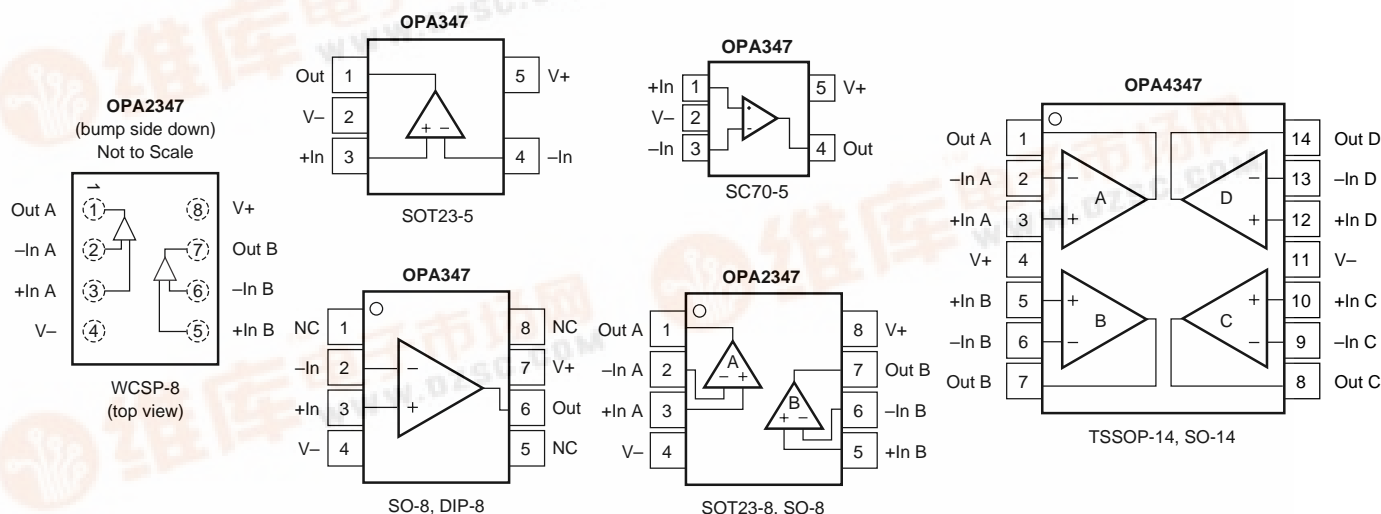
- **PORTABLE EQUIPMENT**
- **BATTERY-POWERED EQUIPMENT**
- **2-WIRE TRANSMITTERS**
- **SMOKE DETECTORS**
- **CO DETECTORS**

DESCRIPTION

The OPA347 is a *microPower*, low-cost operational amplifier available in *micropackages*. The OPA347 (single version) is available in the SC-70 and SOT23-5 packages. The OPA2347 (dual version) is available in the SOT23-8 and WCSP-8 packages. Both are also available in the SO-8. The OPA347 is also available in the DIP-8. The OPA4347 (quad) is available in the SO-14 and the TSSOP-14.

The small size and low power consumption (34 μ A per channel maximum) of the OPA347 make it ideal for portable and battery-powered applications. The input range of the OPA347 extends 200mV beyond the rails, and the output range is within 5mV of the rails. The OPA347 also features an excellent speed/power ratio with a bandwidth of 350kHz.

The OPA347 can be operated with a single or dual power supply from 2.3V to 5.5V. All models are specified for operation from -55°C to $+125^{\circ}\text{C}$.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V-	7.5V
Signal Input Terminals, Voltage ⁽²⁾	(V-) - 0.5V to (V+) + 0.5V
Current ⁽²⁾	10mA
Output Short-Circuit ⁽³⁾	Continuous
Operating Temperature	-65°C to +150°C
Storage Temperature	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA347NA "	SOT23-5 "	DBV "	-55°C to +125°C "	A47 "	OPA347NA/250 OPA347NA/3K	Tape and Reel, 250 Tape and Reel, 3000
OPA347PA OPA347UA "	DIP-8 SO-8 "	P D "	-55°C to +125°C -55°C to +125°C "	OPA347PA OPA347UA "	OPA347PA OPA347UA OPA347UA/2K5	Rails, 50 Rails, 100 Tape and Reel, 2500
OPA347SA "	SC-70 "	DCK "	-55°C to +125°C "	S47 "	OPA347SA/250 OPA347SA/3K	Tape and Reel, 250 Tape and Reel, 3000
OPA2347EA "	SOT23-8 "	DCN "	-55°C to +125°C "	B47 "	OPA2347EA/250 OPA2347EA/3K	Tape and Reel, 250 Tape and Reel, 3000
OPA2347UA "	SO-8 "	D "	-55°C to +125°C "	OPA2347UA "	OPA2347UA OPA2347UA/2K5	Rails, 100 Tape and Reel, 2500
OPA2347YED "	WCSP-8 "	YED "	-55°C to +125°C "	YMD CCS "	OPA2347YEDT OPA2347YEDR	Tape and Reel, 250 Tape and Reel, 3000
OPA4347EA "	TSSOP-14 "	PW "	-55°C to +125°C "	OPA4347EA "	OPA4347EA/250 OPA4347EA/2K5	Tape and Reel, 250 Tape and Reel, 2500
OPA4347UA "	SO-14 "	D "	-55°C to +125°C "	OPA4347UA "	OPA4347UA OPA4347UA/2K5	Rails, 58 Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS: $V_S = 2.5V$ to $5.5V$

Boldface limits apply over the specified temperature range, $T_A = -55^{\circ}C$ to $+125^{\circ}C$.

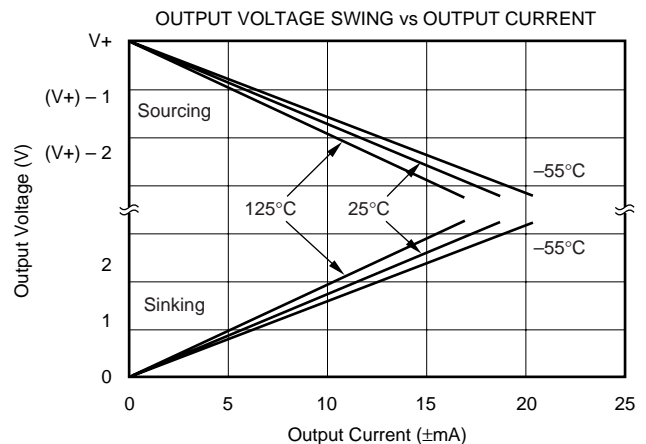
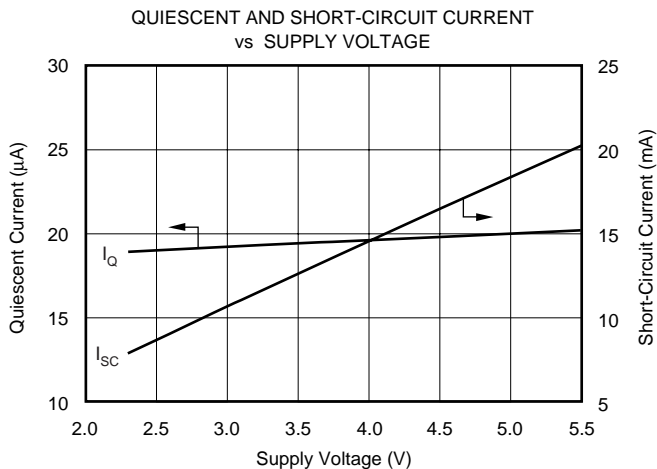
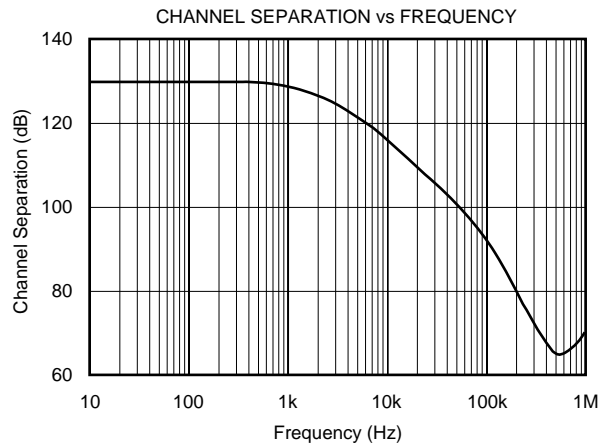
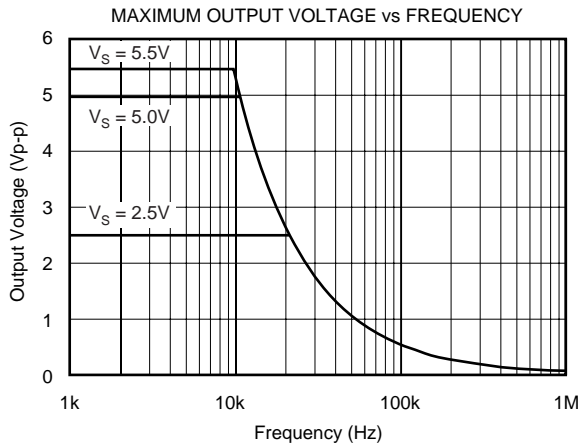
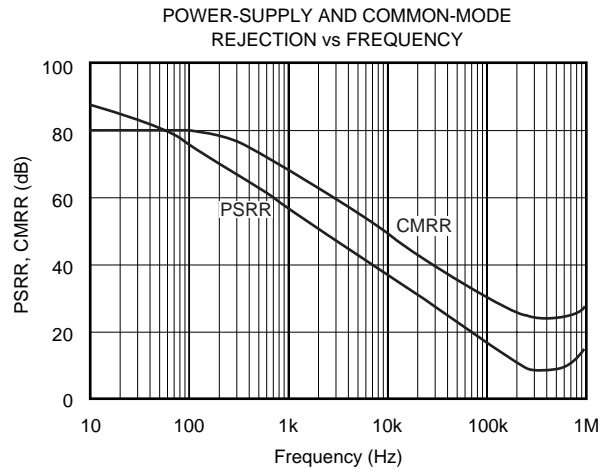
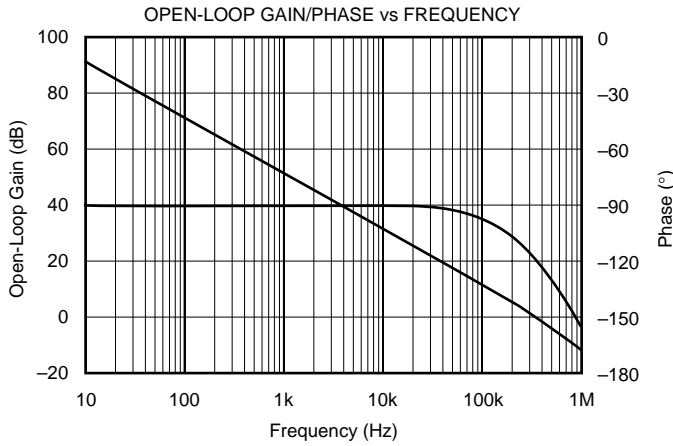
At $T_A = +25^{\circ}C$, $R_L = 100k\Omega$ connected to $V_S/2$ and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	CONDITION	OPA347NA, UA, PA, SA OPA2347EA, UA, YED OPA4347EA, UA			UNITS	
		MIN	TYP	MAX		
OFFSET VOLTAGE Input Offset Voltage over Temperature Drift vs Power Supply over Temperature Channel Separation, DC	V_{OS}	$V_S = 5.5V, V_{CM} = (V-) + 0.8V$	2	6	mV	
	dV_{OS}/dT		2	7	mV	
	PSRR	$V_S = 2.5V$ to $5.5V, V_{CM} < (V+) - 1.7V$	3	3	$\mu V/^{\circ}C$	
		$V_S = 2.5V$ to $5.5V, V_{CM} < (V+) - 1.7V$	60	175	$\mu V/V$	
	$f = 1kHz$		0.3	300	$\mu V/V$	
			128		$\mu V/V$ dB	
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio over Temperature over Temperature	V_{CM}		$(V-) - 0.2$	$(V+) + 0.2$	V	
	CMRR	$V_S = 5.5V, (V-) - 0.2V < V_{CM} < (V+) - 1.7V$	70	80	dB	
		$V_S = 5.5V, V- < V_{CM} < (V+) - 1.7V$	66		dB	
		$V_S = 5.5V, (V-) - 0.2V < V_{CM} < (V+) + 0.2V$	54	70	dB	
	$V_S = 5.5V, V- < V_{CM} < V+$	48		dB		
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Input Offset Current	I_b		± 0.5	± 10	pA	
	I_{OS}		± 0.5	± 10	pA	
INPUT IMPEDANCE Differential Common-Mode			$10^{13} \parallel 3$		$\Omega \parallel pF$	
			$10^{13} \parallel 6$		$\Omega \parallel pF$	
NOISE Input Voltage Noise, $f = 0.1Hz$ to $10Hz$ Input Voltage Noise Density, $f = 1kHz$ Input Current Noise Density, $f = 1kHz$		$V_{CM} < (V+) - 1.7V$			μV_{PP}	
	e_n		12		nV/\sqrt{Hz}	
	i_n		60		fA/\sqrt{Hz}	
			0.7			
OPEN-LOOP GAIN Open-Loop Voltage Gain over Temperature over Temperature	A_{OL}	$V_S = 5.5V, R_L = 100k\Omega, 0.015V < V_O < 5.485V$	100	115	dB	
		$V_S = 5.5V, R_L = 100k\Omega, 0.015V < V_O < 5.485V$	88		dB	
		$V_S = 5.5V, R_L = 5k\Omega, 0.125V < V_O < 5.375V$	100	115	dB	
		$V_S = 5.5V, R_L = 5k\Omega, 0.125V < V_O < 5.375V$	88		dB	
	A_{OL} (SC-70 only)	$V_S = 5.5V, R_L = 5k\Omega, 0.125V < V_O < 5.375V$	96	115	dB	
OUTPUT Voltage Output Swing from Rail over Temperature over Temperature Short-Circuit Current Capacitive Load Drive		$R_L = 100k\Omega, A_{OL} > 100dB$		5	mV	
		$R_L = 100k\Omega, A_{OL} > 88dB$		15	mV	
		$R_L = 5k\Omega, A_{OL} > 100dB$		90	mV	
		$R_L = 5k\Omega, A_{OL} > 88dB$		125	mV	
			± 17		mA	
			See Typical Characteristics			
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time, 0.1% 0.01% Overload Recovery Time	GBW	$C_L = 100pF$		350	kHz	
	SR	$G = +1$		0.17	V/ μs	
	t_s	$V_S = 5V, 2V$ Step, $G = +1$		21	μs	
		$V_S = 5V, 2V$ Step, $G = +1$		27	μs	
		$V_{IN} \times Gain = V_S$		23	μs	
POWER SUPPLY Specified Voltage Range Minimum Operating Voltage Minimum Operating Voltage (OPA347SA) Quiescent Current (per amplifier) over Temperature	V_S		2.5		V	
				2.3	V	
				2.4	V	
	I_Q	$I_Q = 0$		20	34	μA
				38	μA	
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance	θ_{JA}		-55		$^{\circ}C$	
			-65		$^{\circ}C$	
			-65		150	$^{\circ}C$
					150	$^{\circ}C$
					200	$^{\circ}C/W$
					150	$^{\circ}C/W$
					150	$^{\circ}C/W$
					150	$^{\circ}C/W$
					100	$^{\circ}C/W$
					100	$^{\circ}C/W$
					100	$^{\circ}C/W$
					250	$^{\circ}C/W$

NOTE: (1) Input bias current for the OPA2347YED package is specified in the absence of light. See the Photosensitivity section for further detail.

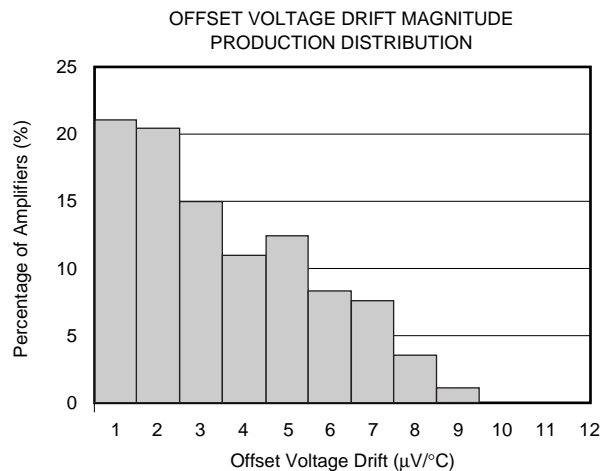
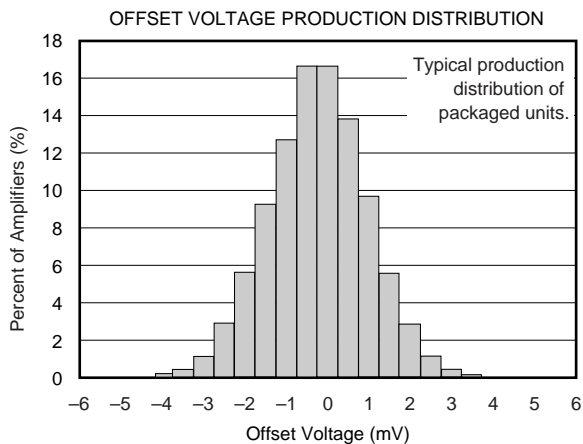
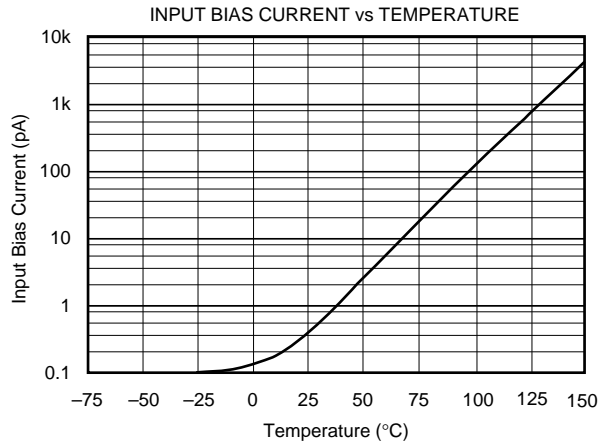
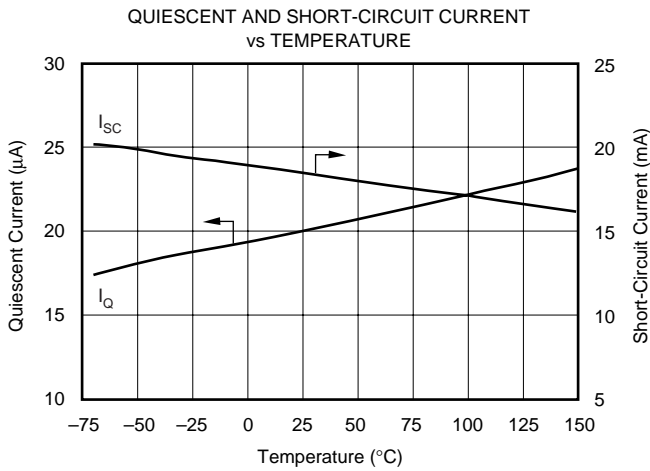
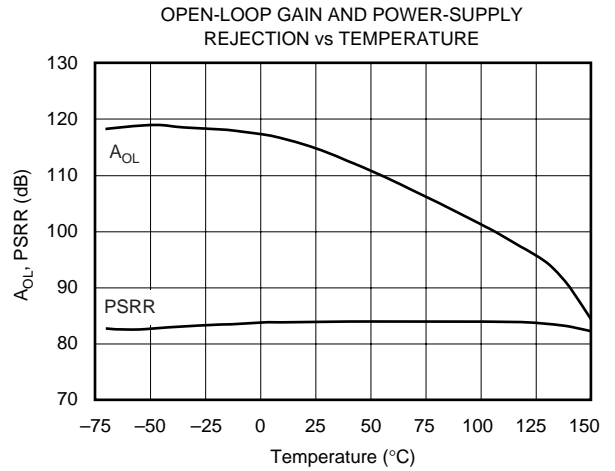
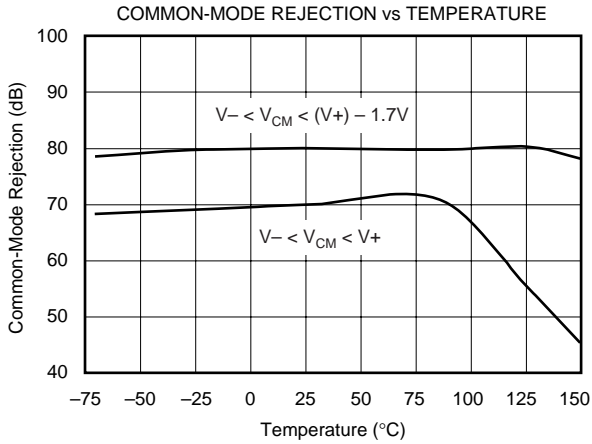
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.



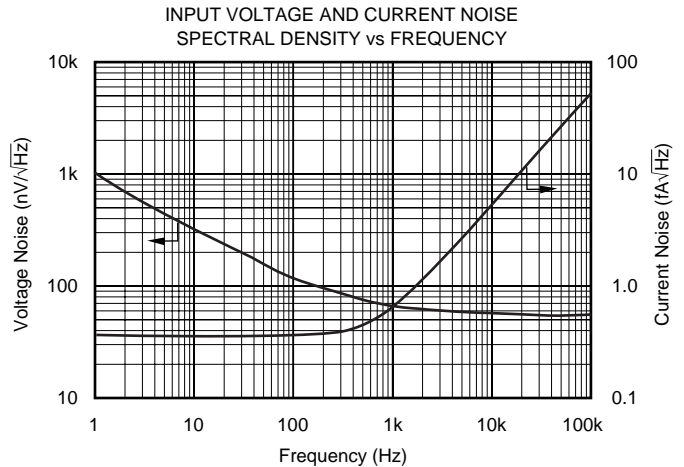
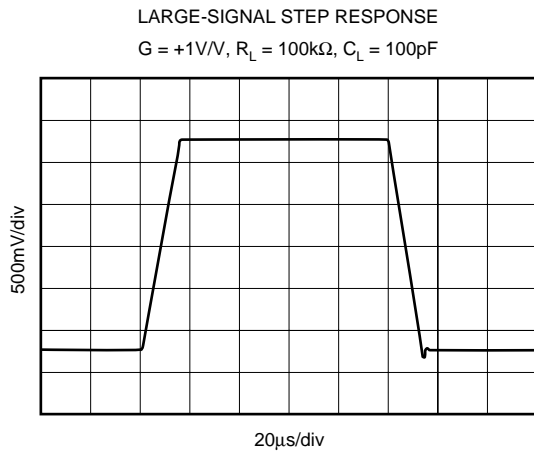
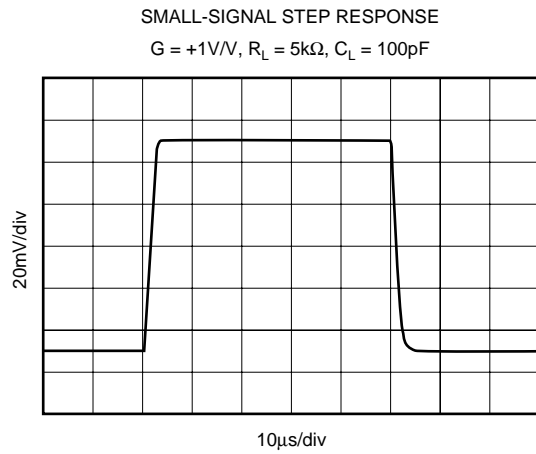
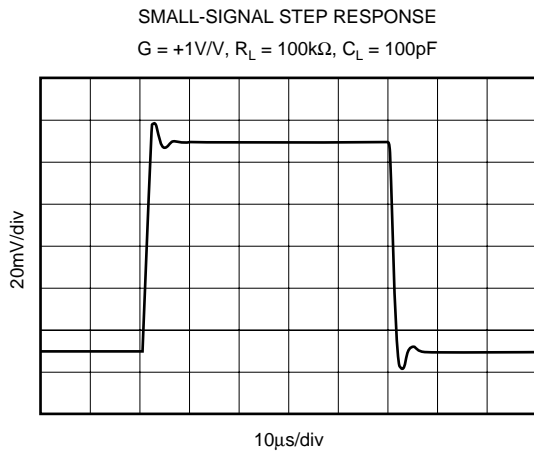
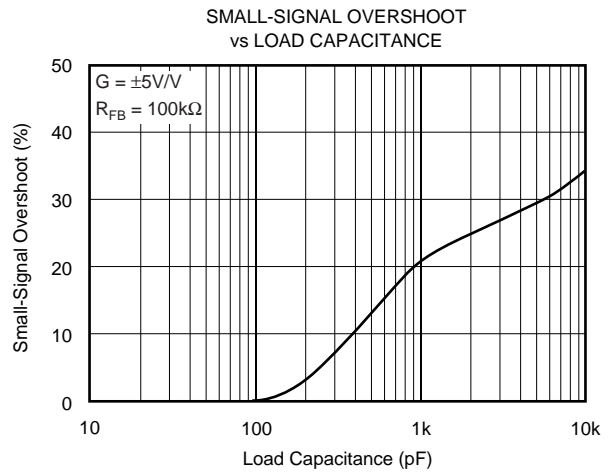
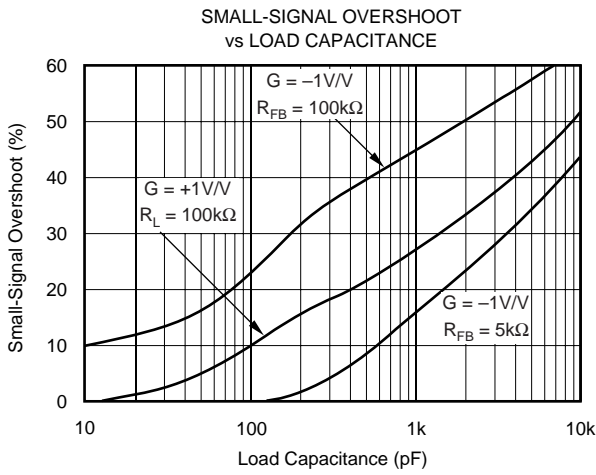
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.



APPLICATIONS INFORMATION

The OPA347 series op amps are unity-gain stable and can operate on a single supply, making them highly versatile and easy to use.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low supply applications. Figure 1 shows the input and output waveforms for the OPA347 in unity-gain configuration. Operation is from $V_S = +5V$ with a $100k\Omega$ load connected to $V_S/2$. The input is a $5V_{PP}$ sinusoid. Output voltage is approximately $4.995V_{PP}$.

Power-supply pins should be bypassed with $0.01\mu F$ ceramic capacitors.

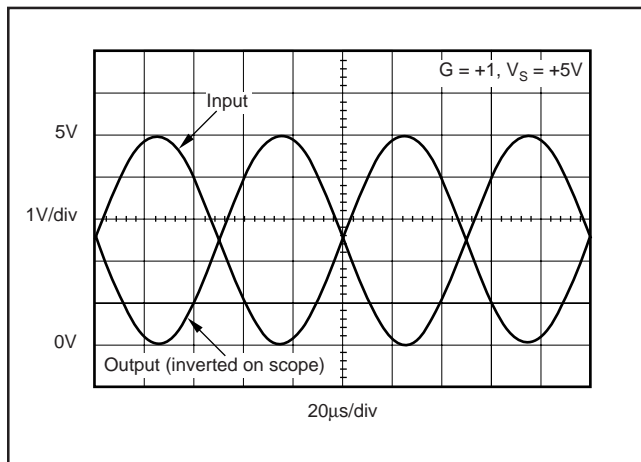


FIGURE 1. Rail-to-Rail Input and Output.

OPERATING VOLTAGE

The OPA347 series op amps are fully specified and ensured from $2.5V$ to $5.5V$. In addition, many specifications apply from $-55^{\circ}C$ to $+125^{\circ}C$. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA347 series extends $200mV$ beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 2. The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.3V$ to $200mV$ above the positive supply, while the P-channel pair is on for inputs from $200mV$ below the negative supply to approximately $(V+) - 1.3V$. There is a small transition region, typically $(V+) - 1.5V$ to $(V+) - 1.1V$, in which both pairs are on. This $400mV$ transition region can vary $300mV$ with process variation. Thus, the transition region (both stages on) can range from $(V+) - 1.65V$ to $(V+) - 1.25V$ on the low end, up to $(V+) - 1.35V$ to $(V+) - 0.95V$ on the high end. Within the $400mV$ transition region PSRR, CMRR, offset voltage, and offset drift may be degraded compared to operation outside this region. For more information on designing with rail-to-rail input op amps, see Figure 3, *Design Optimization with Rail-to-Rail Input Op Amps*.

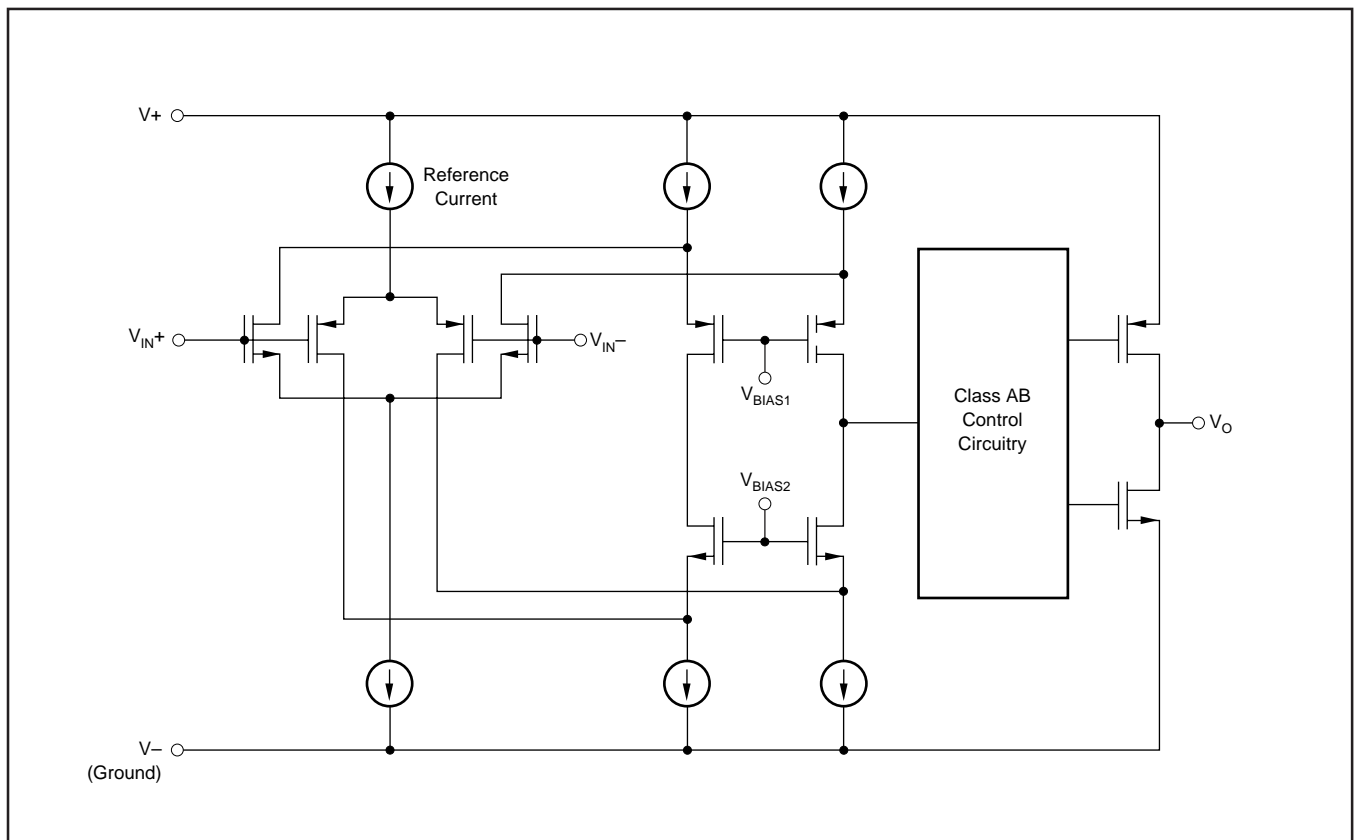


FIGURE 2. Simplified Schematic.

DESIGN OPTIMIZATION WITH RAIL-TO-RAIL INPUT OP AMPS

Rail-to-rail op amps can be used in virtually any op amp configuration. To achieve optimum performance, however, applications using these special double-input-stage op amps may benefit from consideration of their special behavior.

In many applications, operation remains within the common-mode range of only one differential input pair. However, some applications exercise the amplifier through the transition region of both differential input stages. A small discontinuity may occur in this transition. Careful selection of the circuit configuration, signal levels, and biasing can often avoid this transition region.

With a unity-gain buffer, for example, signals will traverse this transition at approximately 1.3V below the $V+$ supply and may exhibit a small discontinuity at this point.

The common-mode voltage of the noninverting amplifier is equal to the input voltage. If the input signal always remains less than the transition voltage, no discontinuity will be created. The closed-loop gain of this configuration can still produce a rail-to-rail output.

Inverting amplifiers have a constant common-mode voltage equal to V_B . If this bias voltage is constant, no discontinuity will be created. The bias voltage can generally be chosen to avoid the transition region.

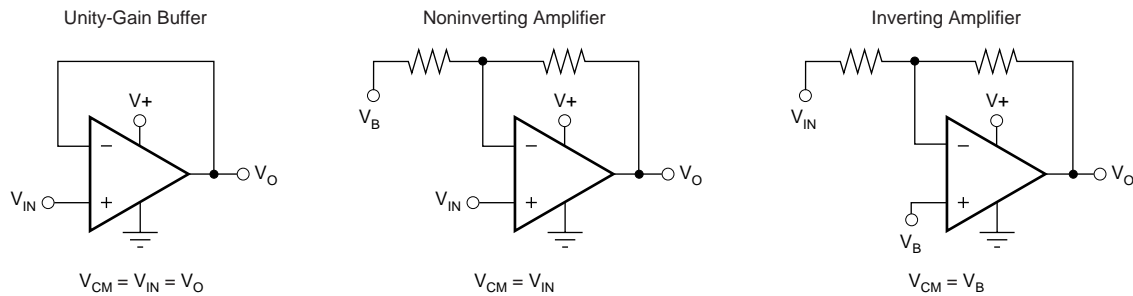


FIGURE 3. Design Optimization with Rail-to-Rail Input Op Amps.

COMMON-MODE REJECTION

The CMRR for the OPA347 is specified in several ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region ($V_{CM} < (V+) - 1.7V$) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at $V_S = 5.5V$ over the entire common-mode range is specified.

INPUT VOLTAGE

The input common-mode range extends from $(V-) - 0.2V$ to $(V+) + 0.2V$. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 500mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, will not cause any damage to the op amp. Furthermore, if input current is limited the inputs may go beyond the power supplies without phase inversion, as shown in Figure 4, unlike some other op amps.

Normally, input currents are 0.4pA. However, large inputs (greater than 500mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, as well as keeping the input voltage below the maximum rating, it is also important to limit the input current to less than 10mA. This is easily accomplished with an input resistor, as shown in Figure 5.

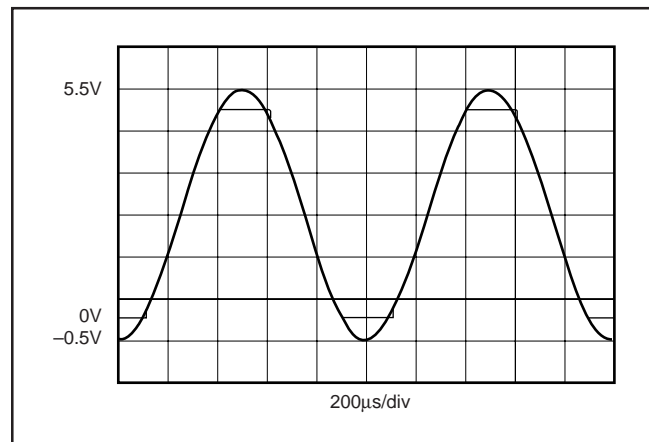


FIGURE 4. OPA347—No Phase Inversion with Inputs Greater than the Power-Supply Voltage.

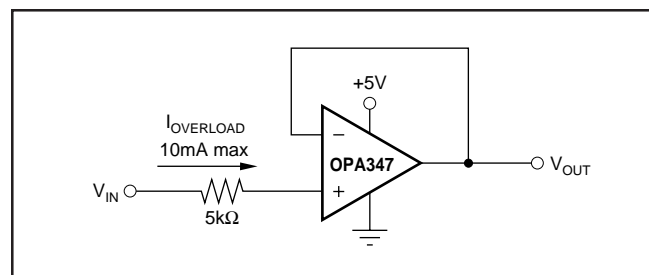


FIGURE 5. Input Current Protection for Voltages Exceeding the Supply Voltage.

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving $5\text{k}\Omega$ loads connected to any potential between $V+$ and ground. For light resistive loads ($> 100\text{k}\Omega$), the output voltage can typically swing to within 5mV from supply rail. With moderate resistive loads ($10\text{k}\Omega$ to $50\text{k}\Omega$), the output can swing to within a few tens of millivolts from the supply rails while maintaining high open-loop gain (see the typical characteristic Output Voltage Swing vs Output Current).

CAPACITIVE LOAD AND STABILITY

The OPA347 in a unity-gain configuration can directly drive up to 250pF pure capacitive load. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads (see the characteristic curve Small-Signal Overshoot vs Capacitive Load). In unity-gain configurations, capacitive load drive can be improved by inserting a small (10Ω to 20Ω) resistor, R_S , in series with the output, as shown in Figure 6. This significantly reduces ringing while maintaining Direct Current (DC) performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a DC error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L , and is generally negligible.

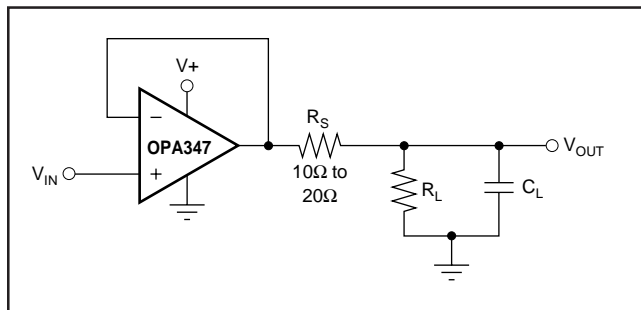


FIGURE 6. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive.

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the op amp input, and the gain setting resistors, thus degrading capacitive load drive. Best performance is achieved by using small valued resistors. For example, when driving a 500pF

load, reducing the resistor values from $100\text{k}\Omega$ to $5\text{k}\Omega$ decreases overshoot from 40% to 8% (see the characteristic curve Small-Signal Overshoot vs Load Capacitance). However, when large-valued resistors can not be avoided, a small (4pF to 6pF) capacitor, C_{FB} , can be inserted in the feedback, as shown in Figure 7. This significantly reduces overshoot by compensating the effect of capacitance, C_{IN} , which includes the amplifier input capacitance and PC board parasitic capacitance.

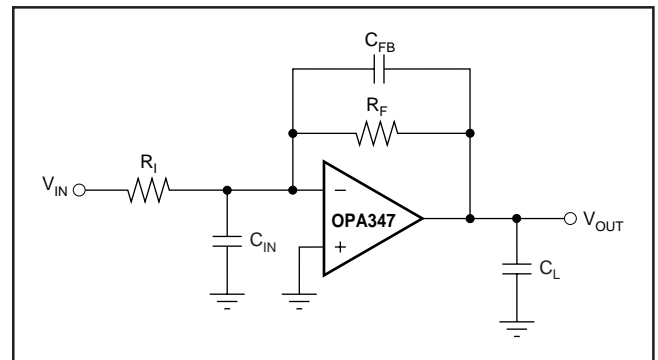


FIGURE 7. Adding a Feedback Capacitor In the Unity-Gain Inverter Configuration Improves Capacitive Load.

DRIVING ADCs

The OPA347 series op amps are optimized for driving medium-speed sampling Analog-to-Digital Converters (ADCs). The OPA347 op amps buffer the ADC's input capacitance and resulting charge injection while providing signal gain.

See Figure 8 for the OPA347 in a basic noninverting configuration driving the ADS7822. The ADS7822 is a 12-bit, *microPower* sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPA347, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC input can be used to provide for anti-aliasing filter and charge injection current.

See Figure 9 for the OPA2347 driving an ADS7822 in a speech bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit will operate with $V_S = 2.7\text{V}$ to 5V with less than $250\mu\text{A}$ typical quiescent current.

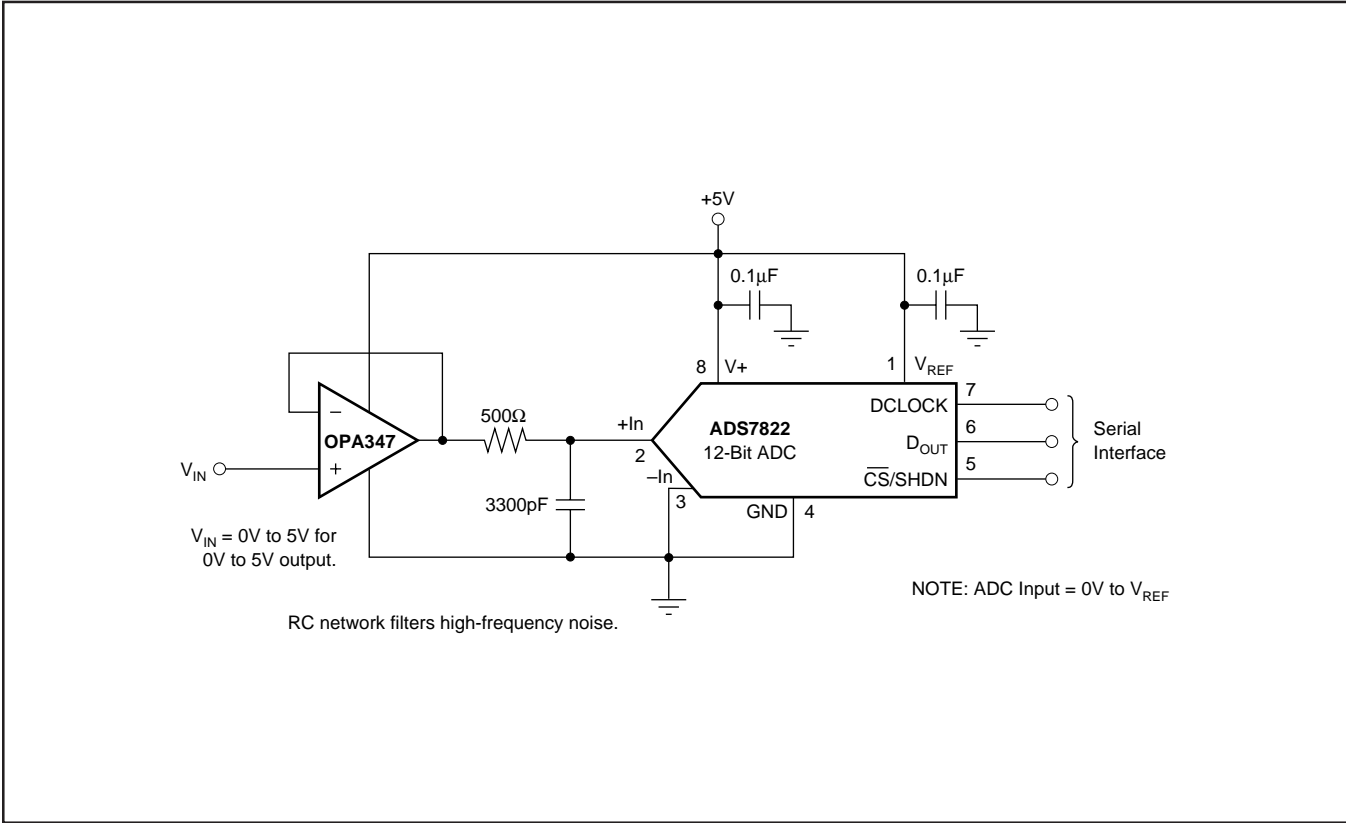


FIGURE 8. OPA347 in Noninverting Configuration Driving ADS7822.

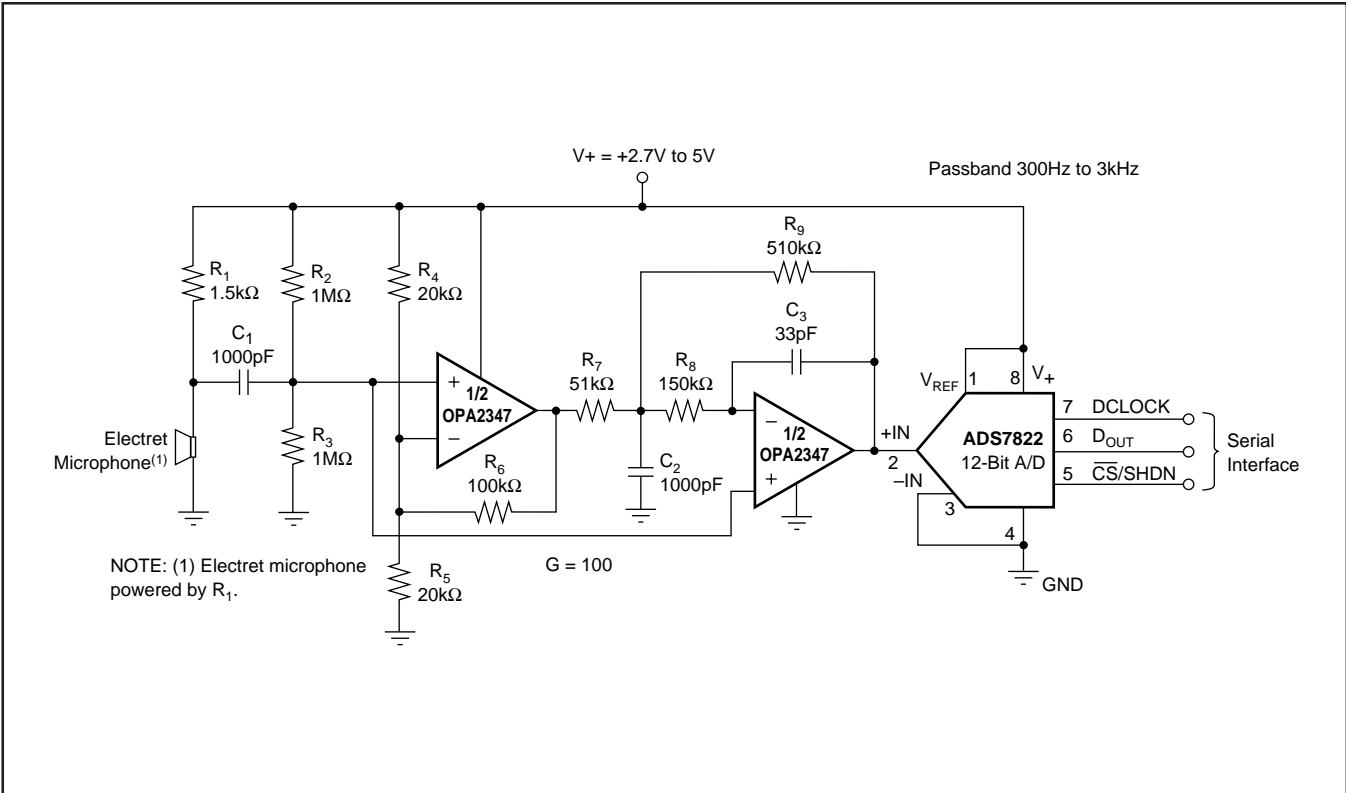


FIGURE 9. Speech Bandpass Filtered Data Acquisition System.

OPA2347 WCSP PACKAGE

The OPA2347YED is a die-level package using bump-on-pad technology. Unlike plastic packages, the OPA2347YED has no molding compound, lead frame, wire bonds, or leads. Using standard surface-mount assembly procedures, the WCSP can be mounted to a printed circuit board without additional under fill. Figures 10 and 11 detail pinout and package marking.

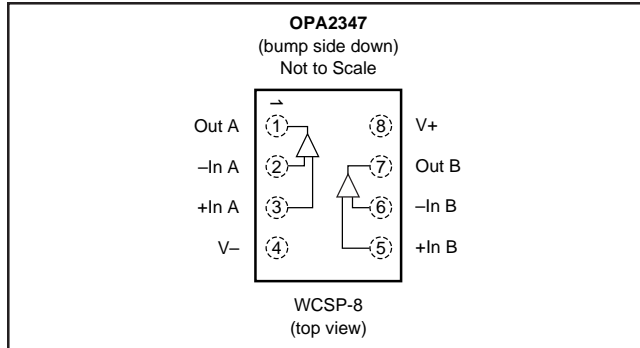


FIGURE 10. Pin Description.

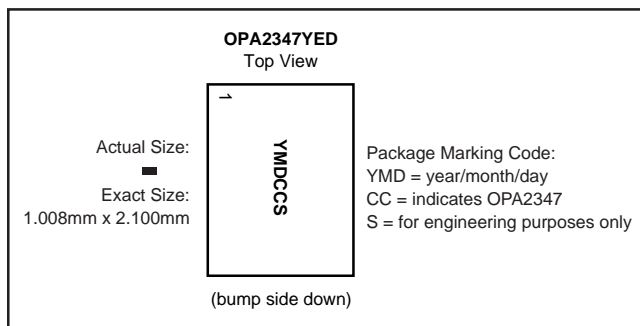


FIGURE 11. Top View Package Marking.

PHOTOSENSITIVITY

Although the OPA2347YED package has a protective backside coating that reduces the amount of light exposure on the die, unless fully shielded, ambient light will still reach the active region of the device. Input bias current for the OPA2347YED package is specified in the absence of light. Depending on the amount of light exposure in a given application, an increase in bias current, and possible increases in offset voltage should be expected. In circuit board tests under ambient light conditions, a typical increase in bias current reached 100pA. Fluorescent lighting may introduce noise or hum due to their time varying light output. Best practice should include end-product packaging that provides shielding from possible light sources during operation.

TEST	CONDITION	ACCEPT CRITERIA (ACTUAL)	SAMPLE SIZE
Temperature Cycle	-40°C to 125°C, 1 Cycle/hr, 15 Minute Ramp ⁽¹⁾ 10 Minute Dwell	500 (1600) Cycles, $R < 1.2X$ from R_0	36
Drop	50cm	10 (129) Drops, $R < 1.2X$ from R_0	8
Key Push	100 Cycles/min, 1300 μe , Displacement = 2.7mm Max	5K (6.23K) Cycles, $R < 1.2X$ from R_0	8
3 Point Bend	Strain Rate 5 mm/min, 85 mm Span	$R < 1.2X$ from R_0	8

NOTE: (1) Per IPC9701.

TABLE II. Reliability Test Results.

PACKAGE DIMENSIONS

The OPA2347YED is transported in tape and reel media and is described in Table I and Figure 12. Pin 1 orientation is consistent throughout the tape and reel carrier, with balls facing down in each pocket of the carrier tape. The location of Pin 1 is specified in Figure 12.

DIMENSIONS (mm)	OPA2347YED
Pocket Width, A_0	1.12 ± 0.10
Pocket Length, B_0	2.13 ± 0.10
Pocket Depth, K_0	0.61 ± 0.10
Pocket Pitch, P_1	4.00 ± 0.10
Sprocket Hole-to-Pocket Centerline, F	3.50 ± 0.05
Sprocket Hole-to-Pocket Offset, P_2	2.00 ± 0.05
Sprocket Hole Pitch, P_0	4.00 ± 0.10
Tape Width, W	8.00 ± 0.30
Reel Diameter, Max	TBD

TABLE I. Carrier Tape Dimensions.

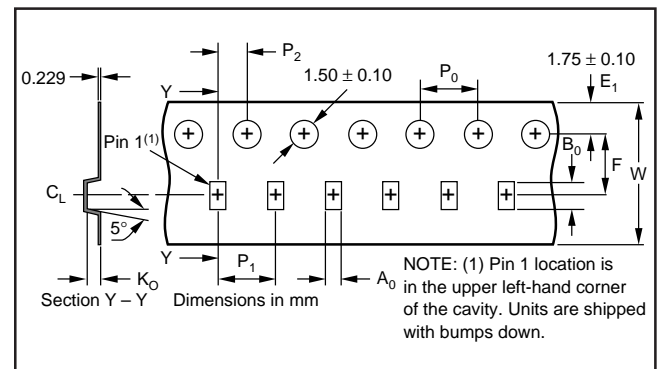


FIGURE 12. Tape and Reel Carrier Tape Diagram.

LAND PATTERNS AND ASSEMBLY

The recommended land pattern for the OPA2347YED package is detailed in Figure 13 with specifications listed in Table III. The maximum amount of force during assembly should be limited to 30 grams of force per bump.

RELIABILITY TESTING

To ensure reliability, the OPA2347YED has been verified to successfully pass a series of reliability stress tests. A summary of JEDEC standard reliability tests is shown in Table II.

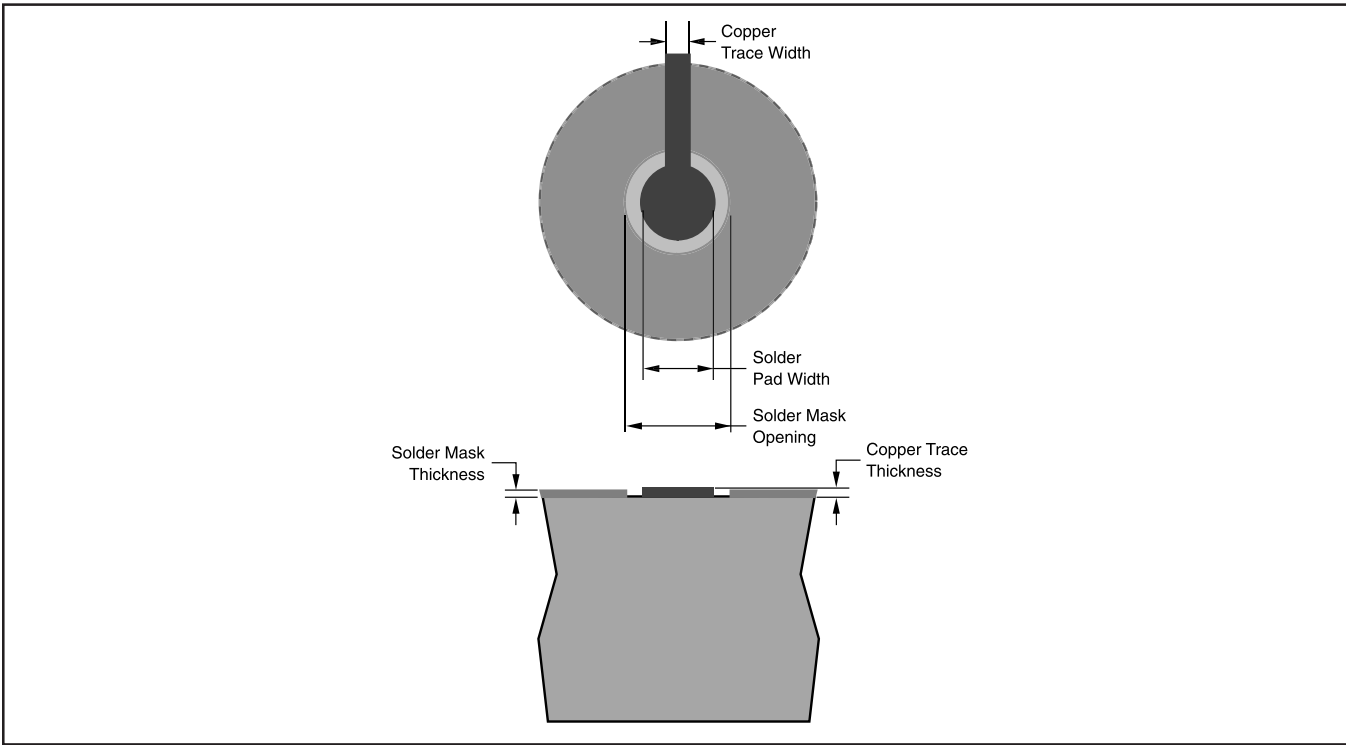


FIGURE 13. Recommended Land Area.

SOLDER PAD DEFINITION	COPPER PAD	SOLDER MASK OPENING	COPPER THICKNESS	STENCIL OPENING	STENCIL THICKNESS
Non-Solder Mask Defined (NSMD)	275 μ m (+0.0, -25 μ m)	375 μ m (+0.0, -25 μ m)	1 oz max	275 μ m X 275 μ m, sq	125 μ m Thick

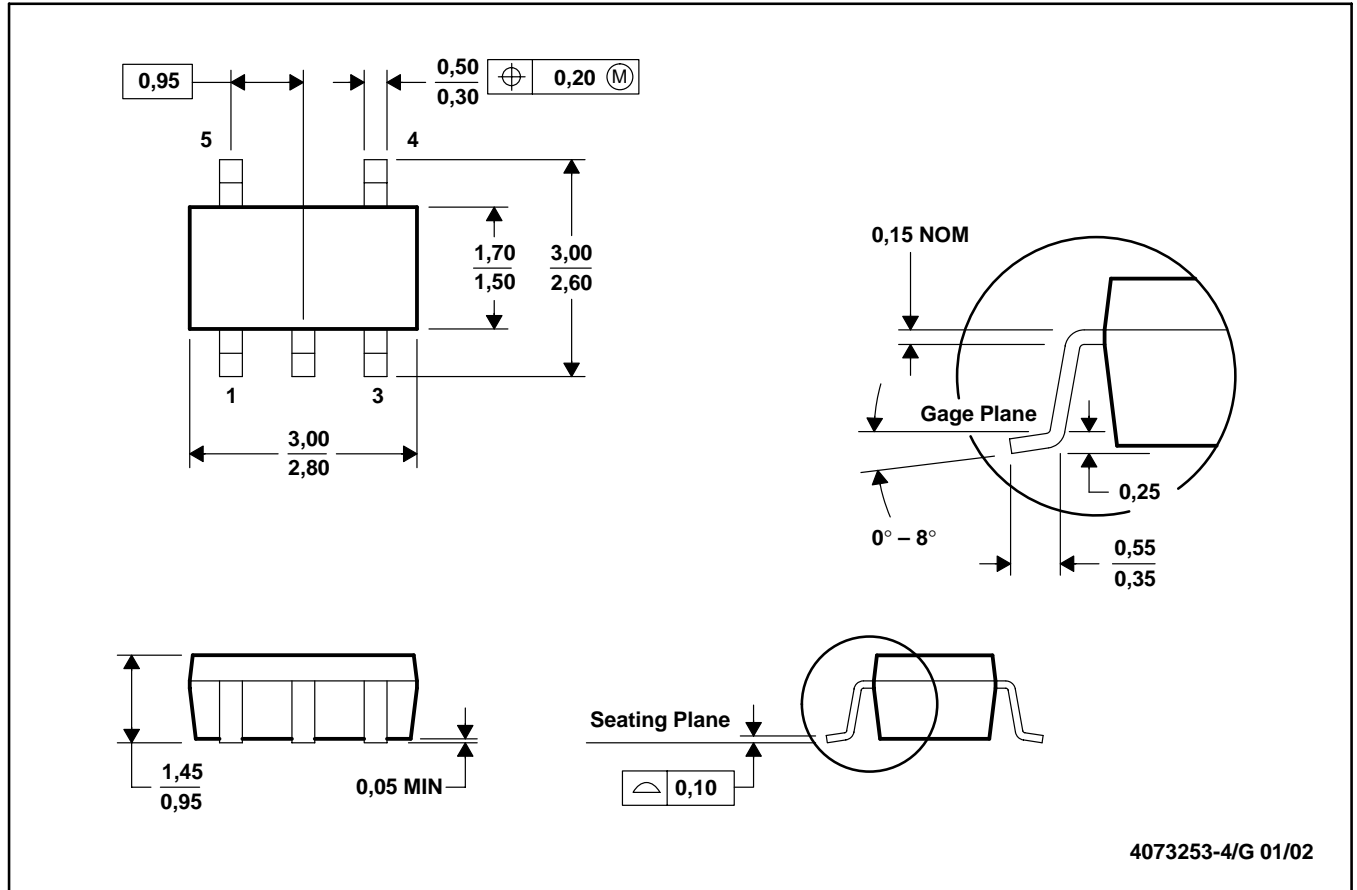
NOTES: (1) Circuit traces from NSMD-defined PWB lands should be less than 100 μ m (preferably = 75 μ m) wide in the exposed area inside the solder mask opening. Wider trace widths will reduce device stand off and impact reliability. (2) Recommended solder paste is type 3 or type 4. (3) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating range of the intended application. (4) For PWB using an Ni/Au surface finish, the gold thickness should be less than 0.5 μ m to avoid solder embrittlement and a reduction in thermal fatigue performance. (5) Solder mask thickness should be less than 20 μ m on top of the copper circuit pattern. (6) Best solder stencil performance will be achieved using laser-cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control. (7) Trace routing away from the WLCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

TABLE III. Recommended Land Pattern.

PACKAGE DRAWINGS

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE

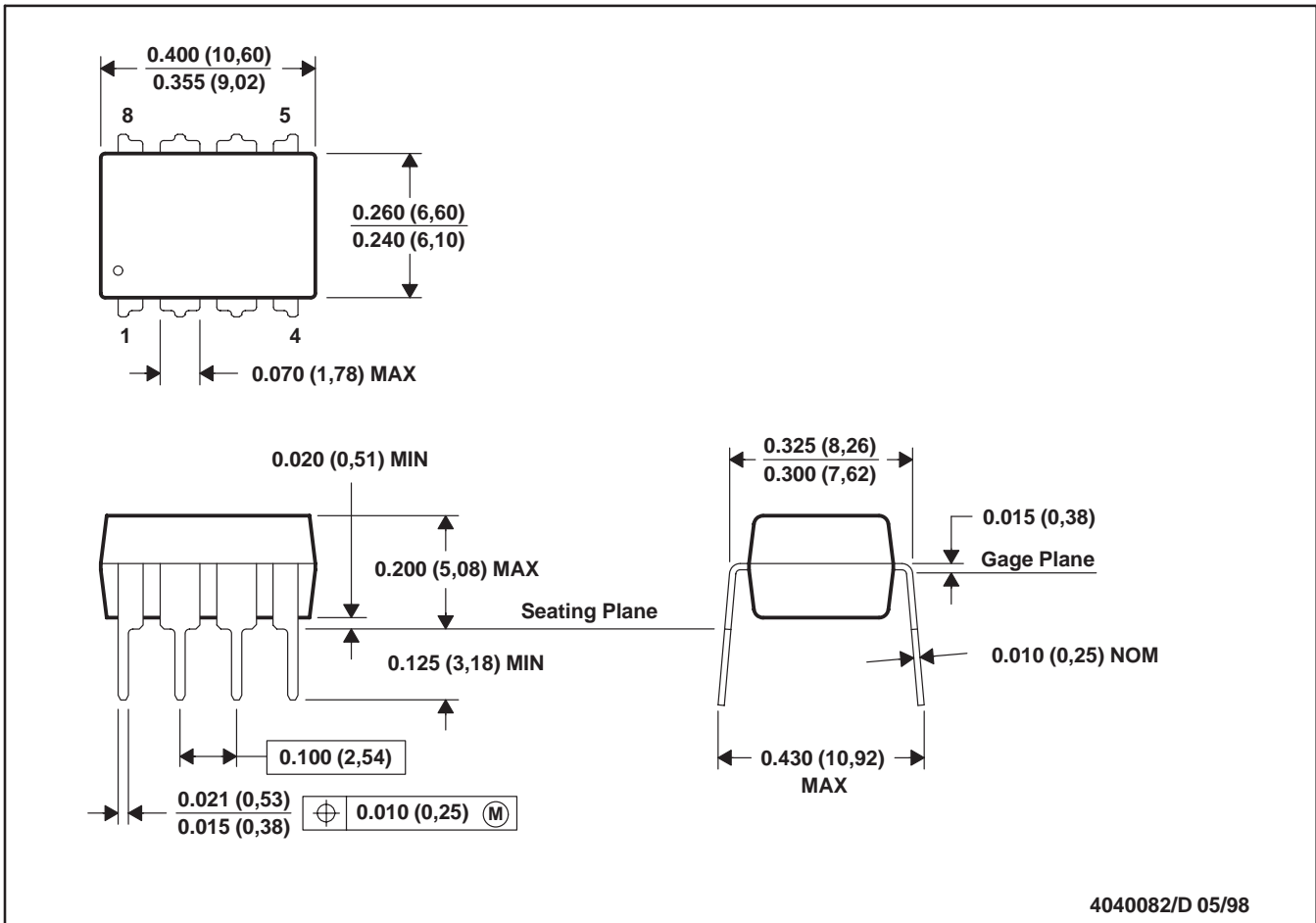


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-178

PACKAGE DRAWINGS (Cont.)

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



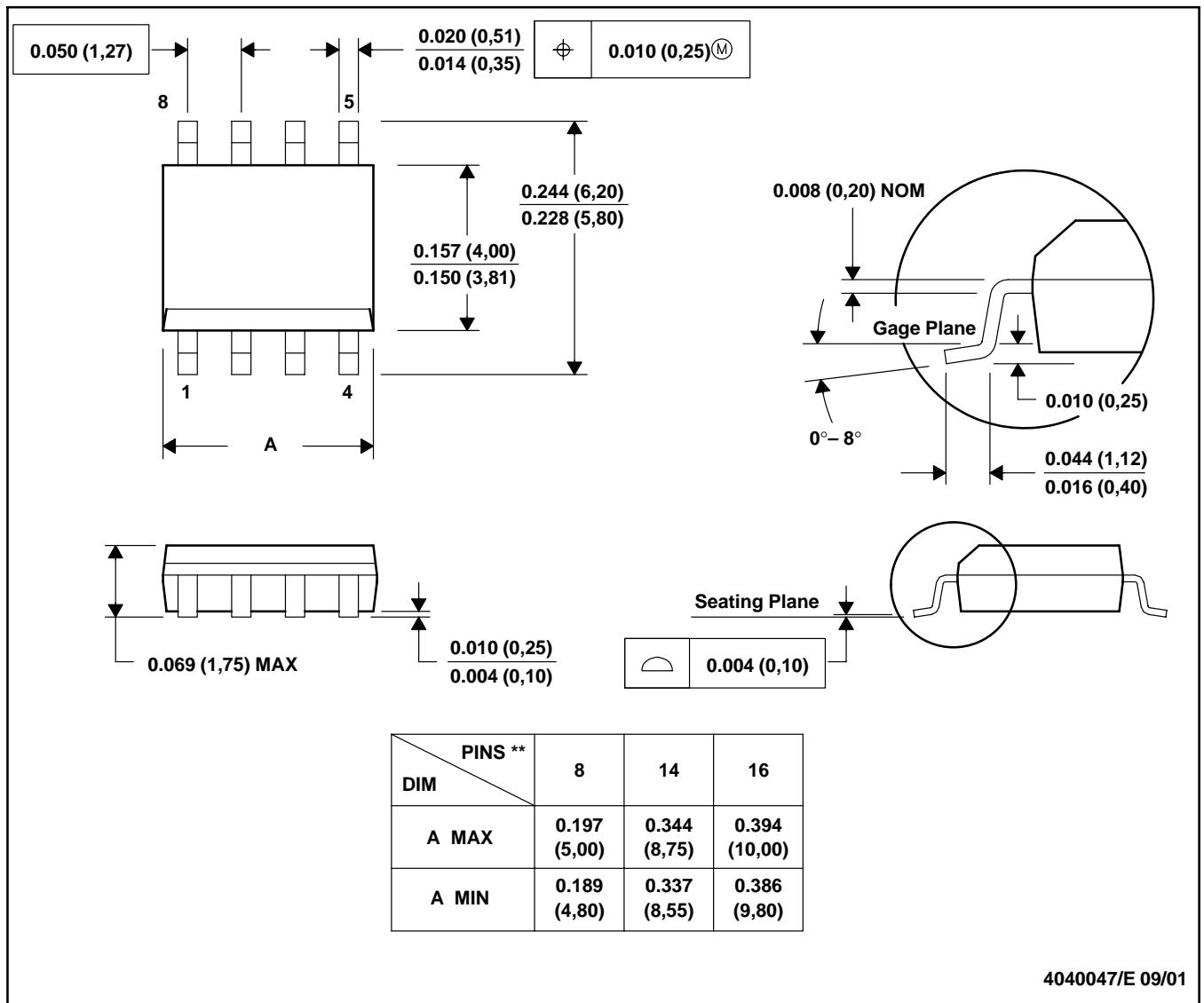
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

PACKAGE DRAWINGS (Cont.)

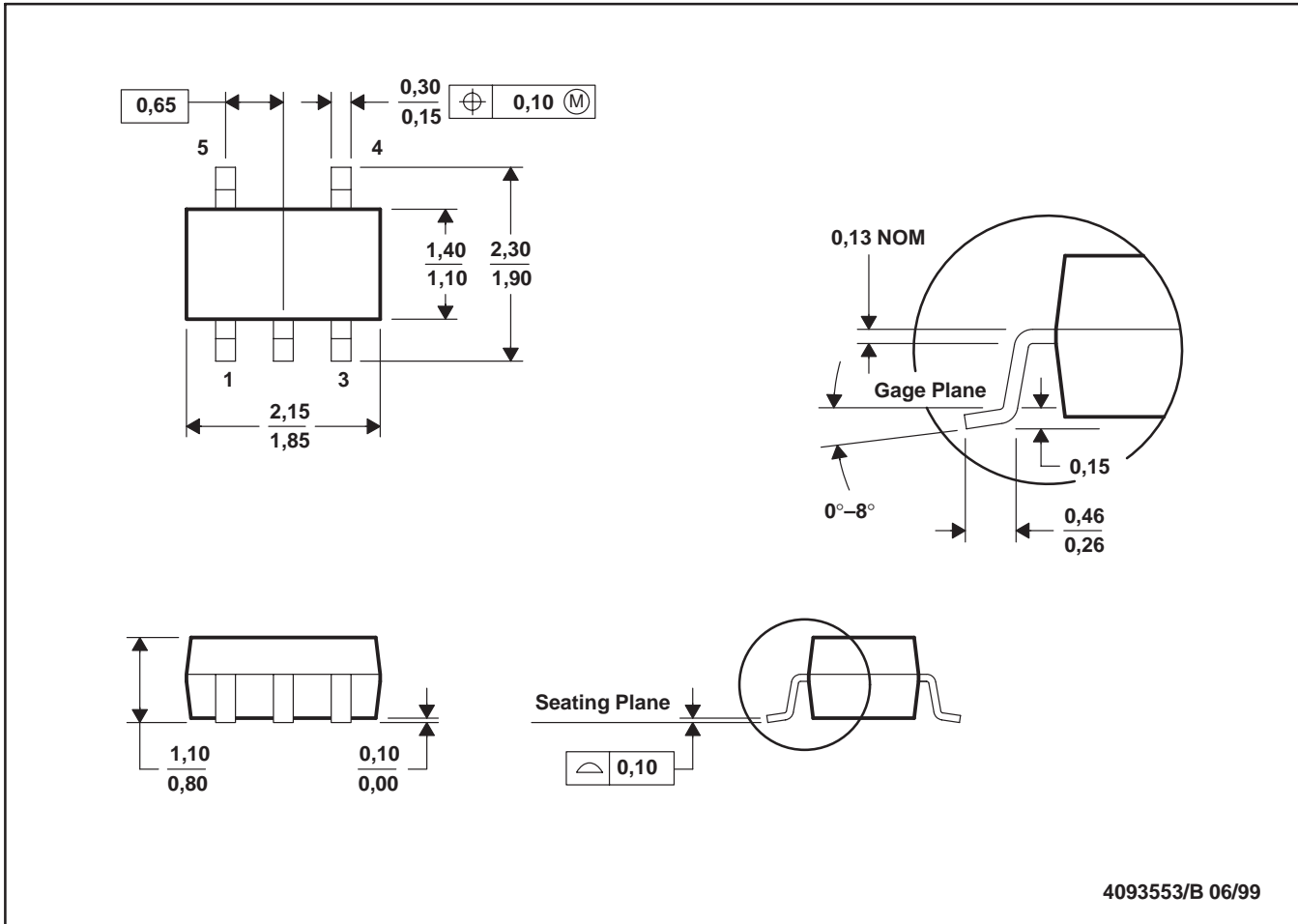
D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

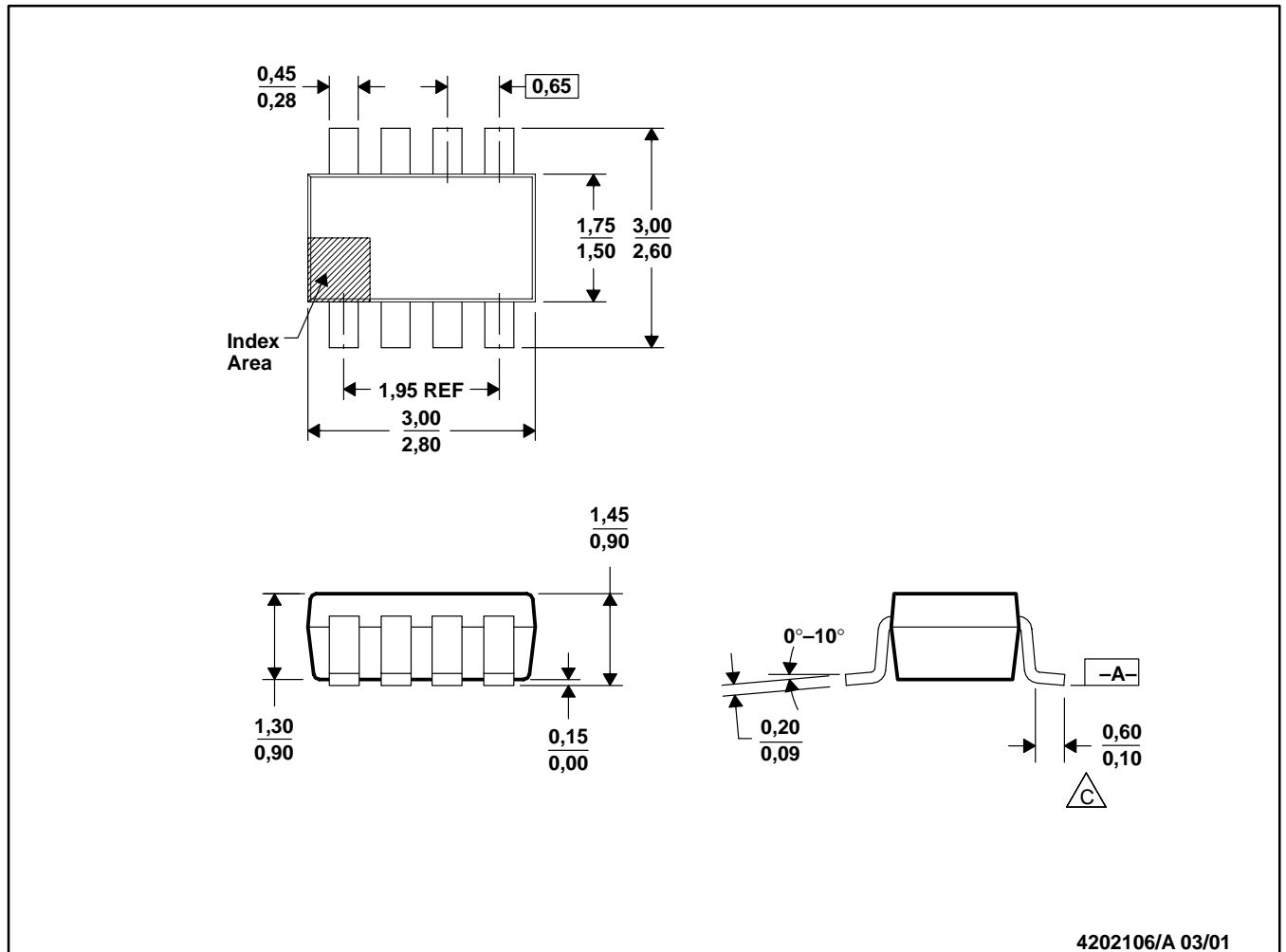
8 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-203

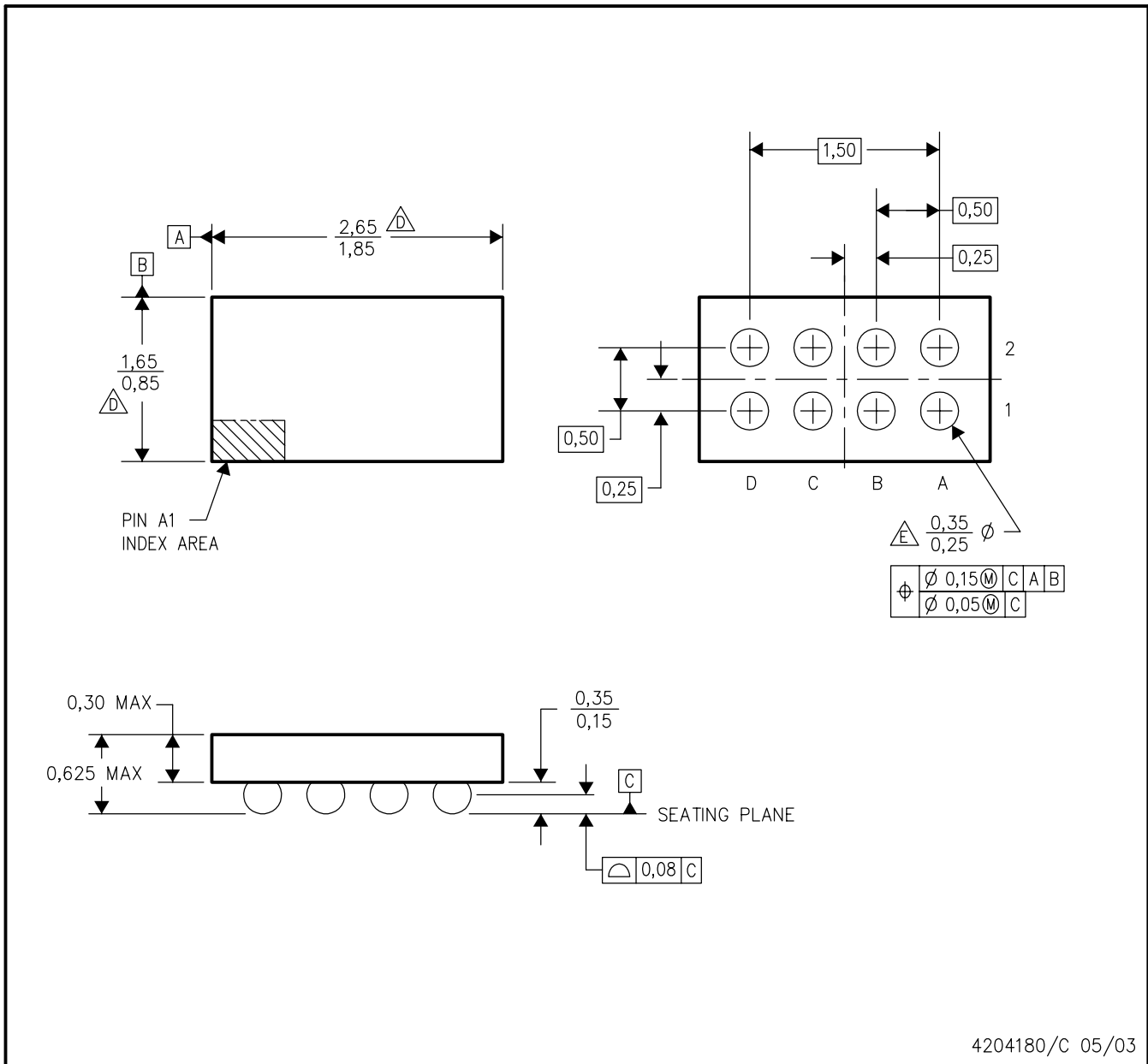


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- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Foot length measured reference to flat foot surface parallel to Datum A.
 - D. Package outline exclusive of mold flash, metal burr and dambar protrusion/intrusion.
 - E. Package outline inclusive of solder plating.
 - F. A visual index feature must be located within the cross-hatched area.

YED (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



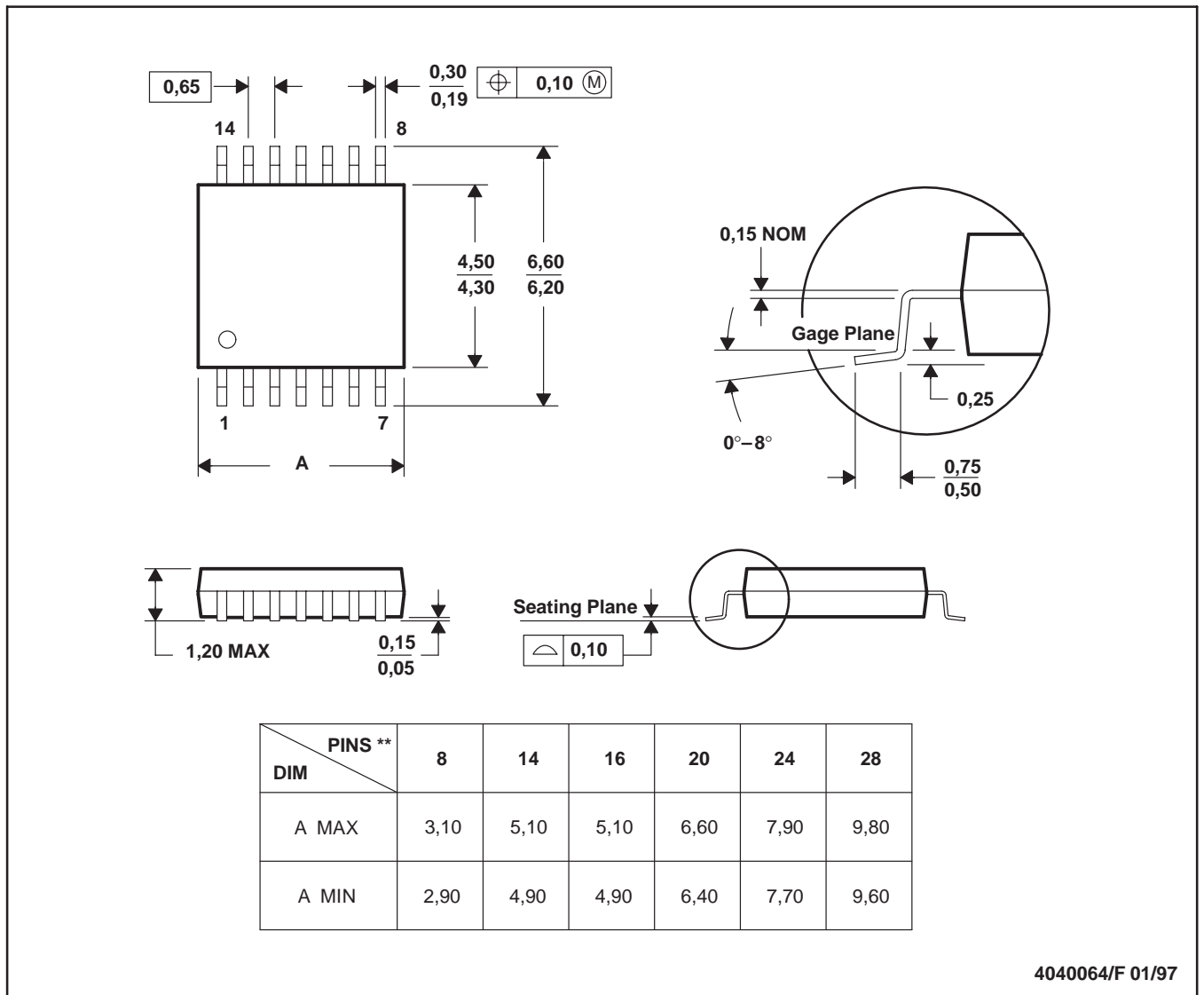
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Die size package configuration.
 - $\triangle D$ Reference Product Data Sheet for die size and orientation.
 - $\triangle E$ Reference Product Data Sheet for array population.
4 x 2 matrix pattern is shown for illustration only.
 - F. This package is Tin-Lead (SnPb).
Refer to YZD (Drawing #4205057) for Lead Free version.

PACKAGE DRAWINGS (Cont.)

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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