

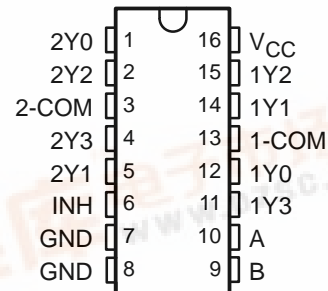
# SN74LV4052A-EP DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULPLEXER

SCLS502 – MAY 2003

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –40°C to 105°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Fast Switching**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Extremely Low Input Current**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PW PACKAGE  
(TOP VIEW)



## description

This dual 4-channel CMOS analog multiplexer/demultiplexer is designed for 2-V to 5.5-V  $V_{CC}$  operation.

The SN74LV4052A handles both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

## ORDERING INFORMATION

$T_A$	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV4052ATPWREP	L4052EP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE

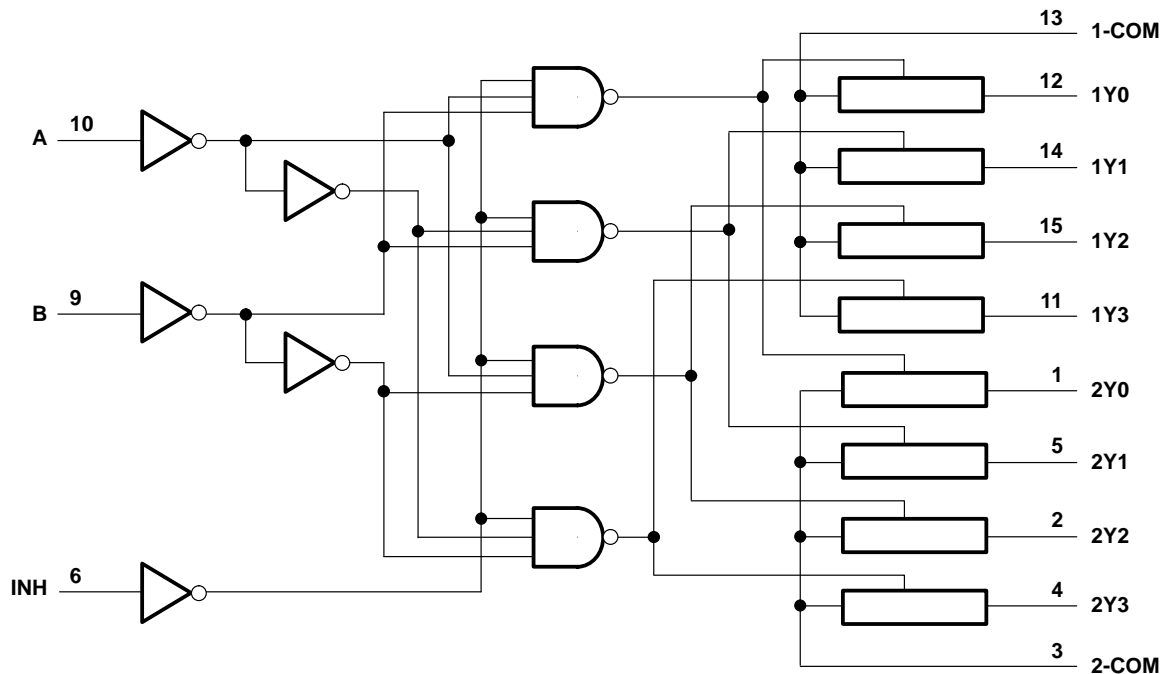
INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7.0 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7.0 V
Switch I/O voltage range, $V_{IO}$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
I/O diode current, $I_{IOK}$ ( $V_{IO} < 0$ or $V_{IO} > V_{CC}$ )	±50 mA
Switch through current, $I_T$ ( $V_{IO} = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3)	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. This value is limited to 5.5 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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## DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

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### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2 <sup>†</sup>	5.5	V
V <sub>IH</sub>	High-level input voltage, control inputs	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage, control inputs	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V		V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Control input voltage		0	5.5	V
V <sub>IO</sub>	Input/output voltage		0	V <sub>CC</sub>	V
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V		200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V		100	
		V <sub>CC</sub> = 4.5 V to 5.5 V		20	
T <sub>A</sub>	Operating free-air temperature		–40	105	°C

<sup>†</sup> With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	MAX	UNIT
r <sub>on</sub>	On-state switch resistance I <sub>T</sub> = 2 mA, V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub> , (see Figure 1)	2.3 V		225	Ω
		3 V		190	
		4.5 V		100	
r <sub>on(p)</sub>	Peak on-state resistance I <sub>T</sub> = 2 mA, V <sub>I</sub> = V <sub>CC</sub> to GND, V <sub>INH</sub> = V <sub>IL</sub>	2.3 V		600	Ω
		3 V		225	
		4.5 V		125	
Δr <sub>on</sub>	Difference in on-state resistance between switches I <sub>T</sub> = 2 mA, V <sub>I</sub> = V <sub>CC</sub> to GND, V <sub>INH</sub> = V <sub>IL</sub>	2.3 V		40	Ω
		3 V		30	
		4.5 V		20	
I <sub>I</sub>	Control input current V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±1	μA
I <sub>S(off)</sub>	Off-state switch leakage current V <sub>I</sub> = V <sub>CC</sub> and V <sub>O</sub> = GND, or V <sub>I</sub> = GND and V <sub>O</sub> = V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IH</sub> , (see Figure 2)	5.5 V		±1	μA
I <sub>S(on)</sub>	On-state switch leakage current V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub> , (see Figure 3)	5.5 V		±1	μA
I <sub>CC</sub>	Supply current V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		20	μA

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## DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

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**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t <sub>PLH</sub> t <sub>PHL</sub> Propagation delay time	COM or Y	Y or COM	C <sub>L</sub> = 50 pF, (see Figure 4)		12	ns
t <sub>PZH</sub> t <sub>PZL</sub> Enable delay time	INH	COM or Y	C <sub>L</sub> = 50 pF, (see Figure 5)		25	ns
t <sub>PHZ</sub> t <sub>PLZ</sub> Disable delay time	INH	COM or Y	C <sub>L</sub> = 50 pF, (see Figure 5)		25	ns

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t <sub>PLH</sub> t <sub>PHL</sub> Propagation delay time	COM or Y	Y or COM	C <sub>L</sub> = 50 pF, (see Figure 4)		8	ns
t <sub>PZH</sub> t <sub>PZL</sub> Enable delay time	INH	COM or Y	C <sub>L</sub> = 50 pF, (see Figure 5)		18	ns
t <sub>PHZ</sub> t <sub>PLZ</sub> Disable delay time	INH	COM or Y	C <sub>L</sub> = 50 pF, (see Figure 5)		18	ns

**analog switch characteristics over recommended operating free-air temperature range (unless  
otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	COM or Y	Y or COM	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 600 Ω, f <sub>in</sub> = 1 MHz (sine wave) (see Note 5 and Figure 6)	2.3 V		30		MHz
				3 V		35		
				4.5 V		50		
Crosstalk (between any switches)	COM or Y	Y or COM	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 600 Ω, f <sub>in</sub> = 1 MHz (sine wave) (see Note 6 and Figure 7)	2.3 V		–45		dB
				3 V		–45		
				4.5 V		–45		
Crosstalk (control input to signal output)	INH	COM or Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 600 Ω, f <sub>in</sub> = 1 MHz (square wave) (see Figure 8)	2.3 V		20		mV
				3 V		35		
				4.5 V		65		
Feed-through attenuation (switch off)	COM or Y	Y or COM	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 600 Ω, f <sub>in</sub> = 1 MHz (sine wave) (see Note 6 and Figure 9)	2.3 V		–45		dB
				3 V		–45		
				4.5 V		–45		
Sine-wave distortion	COM or Y	Y or COM	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 10 kΩ, f <sub>in</sub> = 1 kHz (sine wave) (see Figure 10)	V <sub>I</sub> = 2 V <sub>p-p</sub>	2.3 V		0.1	%
				V <sub>I</sub> = 2.5 V <sub>p-p</sub>	3 V		0.1	
				V <sub>I</sub> = 4 V <sub>p-p</sub>	4.5 V		0.1	

NOTES: 5. Adjust f<sub>in</sub> voltage to obtain 0 dBm at output. Increase f<sub>in</sub> frequency until dB meter reads –3 dB.

6. Adjust f<sub>in</sub> voltage to obtain 0 dBm at input.

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operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50 pF,    f = 10 MHz	11.8	pF

PARAMETER MEASUREMENT INFORMATION

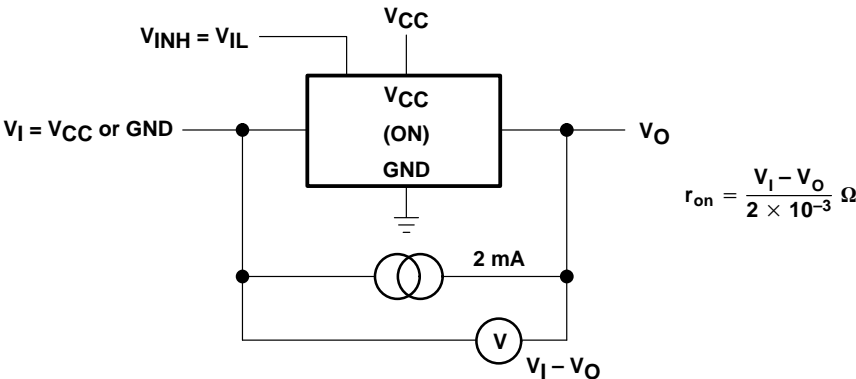


Figure 1. On-State Resistance Test Circuit

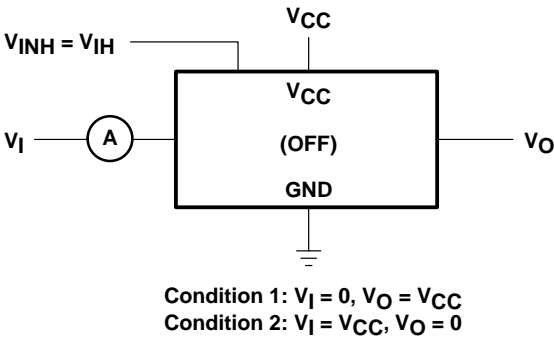


Figure 2. Off-State Switch Leakage-Current Test Circuit

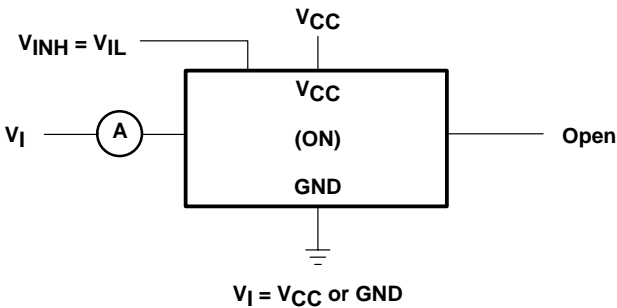


Figure 3. On-State Switch Leakage-Current Test Circuit

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## PARAMETER MEASUREMENT INFORMATION

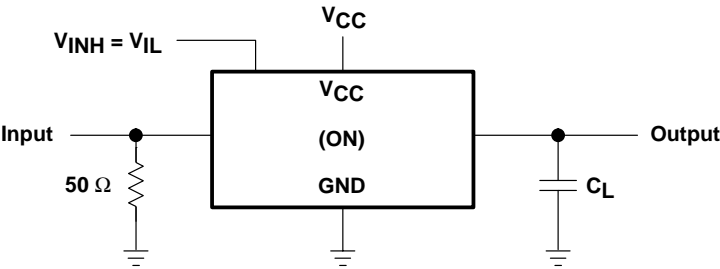


Figure 4. Propagation Delay Time, Signal Input to Signal Output

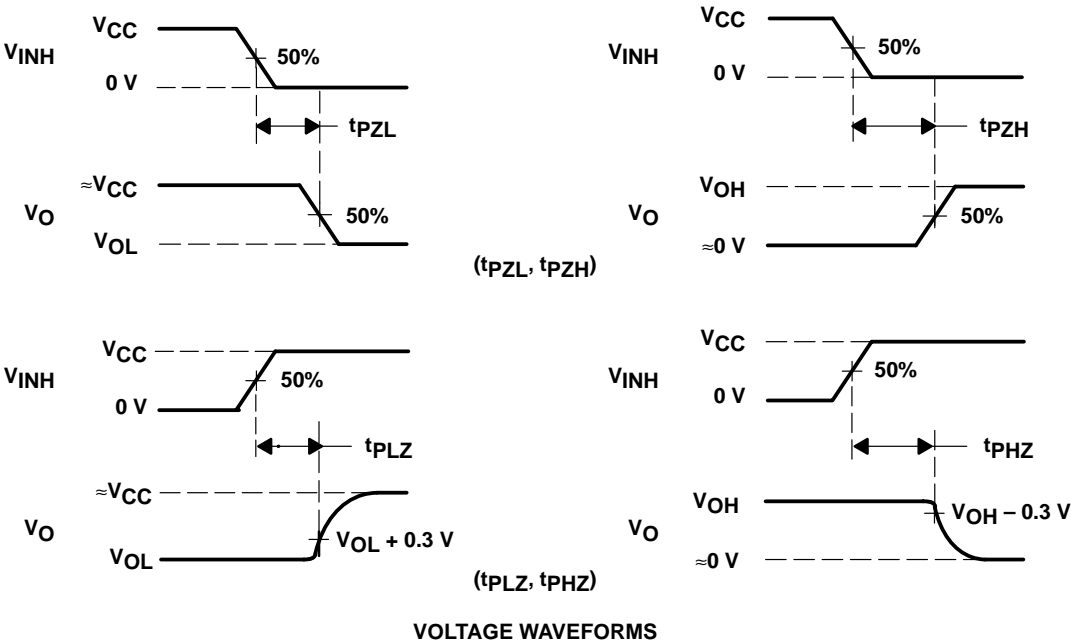
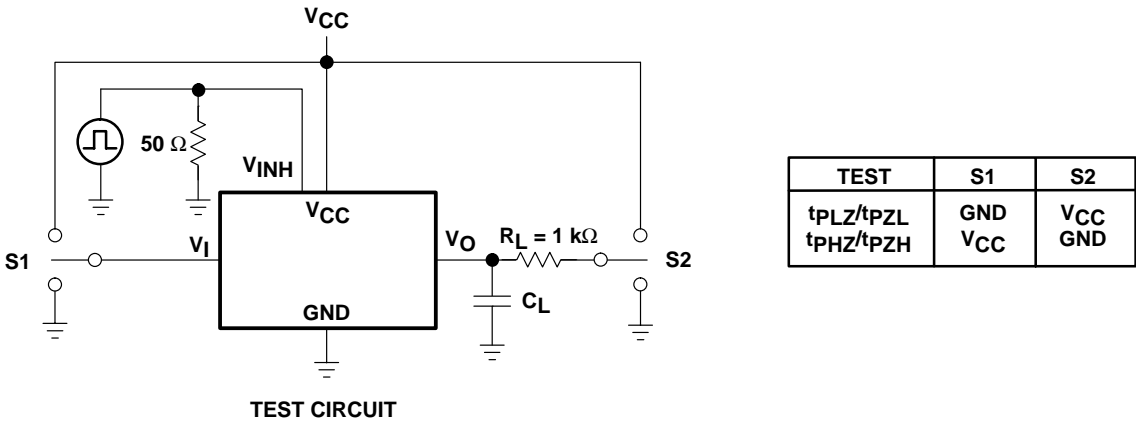


Figure 5. Switching Time (tPZL, tPLZ, tPZH, tPHZ), Control to Signal Output

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## PARAMETER MEASUREMENT INFORMATION

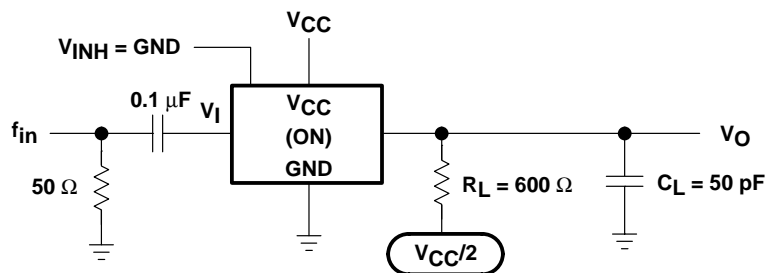


Figure 6. Frequency Response (Switch On)

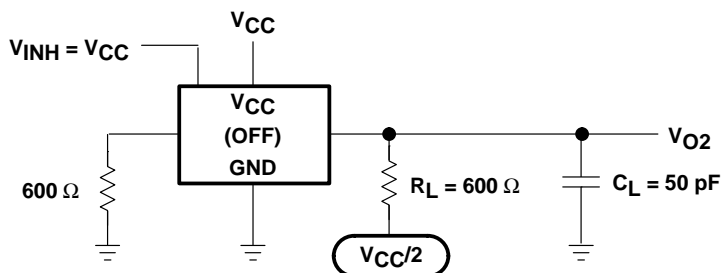
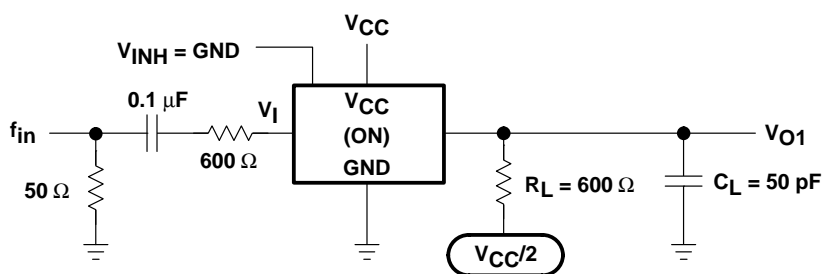


Figure 7. Crosstalk Between Any Two Switches

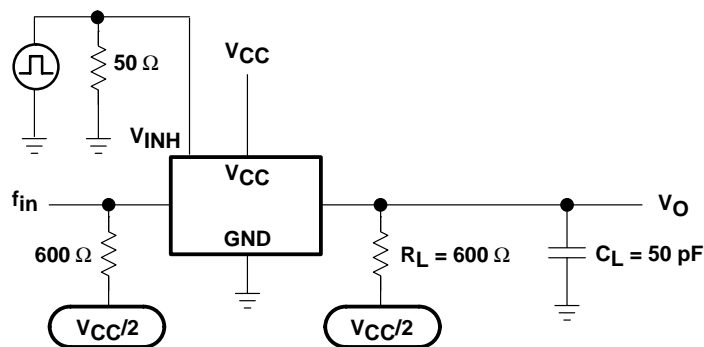


Figure 8. Crosstalk Between Control Input and Switch Output

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### PARAMETER MEASUREMENT INFORMATION

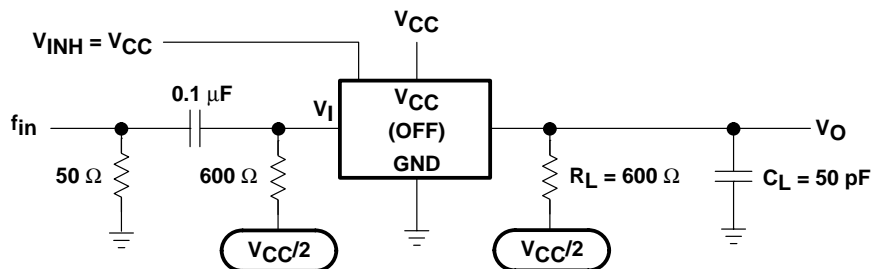


Figure 9. Feed-Through Attenuation (Switch Off)

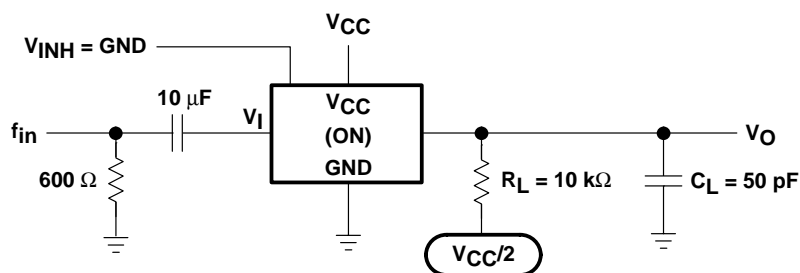


Figure 10. Sine-Wave Distortion

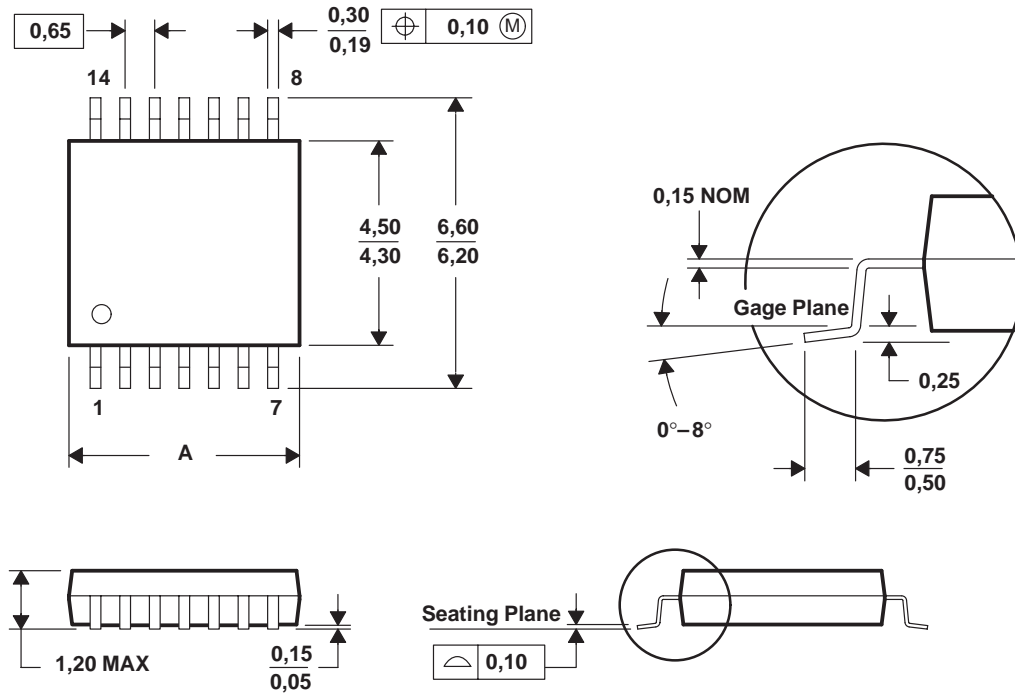
# MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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