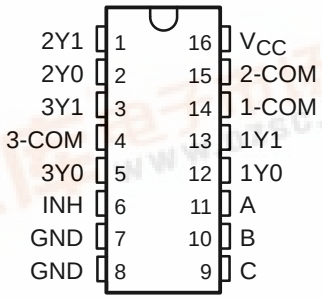
SN74LV4053A-EP
TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

SCLS503 – MAY 2003

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –40°C to 105°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **2-V to 5.5-V V_{CC} Operation**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PW PACKAGE
(TOP VIEW)



description/ordering information

This triple 2-channel CMOS analog multiplexer/demultiplexer is designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV4053A handles both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

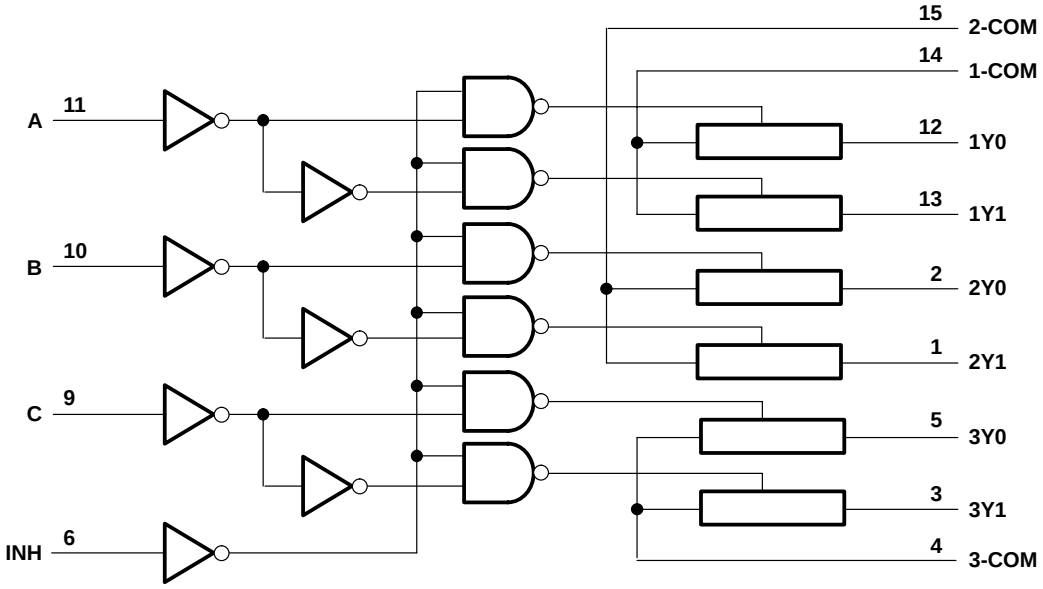
T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV4053ATPWREP	L4053EP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				ON CHANNELS
INH	C	B	A	
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	None

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7.0 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7.0 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$) . . . . . ±50 mA
Switch through current, I_T (V_{IO} = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 108°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2‡	5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	V
V_{IO}	Input/output voltage		0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	105	°C

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN74LV4053A-EP		UNIT
				MIN	TYP	MAX	MIN	MAX	
r_{on}	On-state switch resistance	I_T = 2 mA, V_I = V_{CC} or GND, V_{INH} = V_{IL}, (see Figure 1)	2.3 V		41	180		225	Ω
			3 V		30	150		190	
			4.5 V		23	75		100	
$r_{on(p)}$	Peak on-state resistance	I_T = 2 mA, V_I = V_{CC} to GND, V_{INH} = V_{IL}	2.3 V		139	500		600	Ω
			3 V		63	180		225	
			4.5 V		35	100		125	
Δr_{on}	Difference in on-state resistance between switches	I_T = 2 mA, V_I = V_{CC} to GND, V_{INH} = V_{IL}	2.3 V		2	30		40	Ω
			3 V		1.6	20		30	
			4.5 V		1.3	15		20	
I_I	Control input current	V_I = 5.5 V or GND	0 to 5.5 V			±0.1		±1	μA
$I_{S(off)}$	Off-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_{INH} = V_{IH}, (see Figure 2)	5.5 V			±0.1		±1	μA
$I_{S(on)}$	On-state switch leakage current	V_I = V_{CC} or GND, V_{INH} = V_{IH} (see Figure 3)	5.5 V			±0.1		±1	μA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5 V					20	μA
C_{IC}	Control input capacitance				2				pF
C_{IS}	Common terminal capacitance				8.2				pF
C_{OS}	Switch terminal capacitance				5.6				pF
C_F	Feed-through capacitance				0.5				pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN74LV4053A-EP		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		2.5	10		16	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		7.6	18		23	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		7.7	18		23	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 4)		4.4	12		18	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		8.8	28		35	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		11.7	28		35	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN74LV4053A-EP		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		1.6	6		10	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		5.3	12		15	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		6.1	12		15	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 4)		2.9	9		12	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		6.1	20		25	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		8.9	20		25	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN74LV4053A-EP		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF, (see Figure 4)		0.9	4		7	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		3.8	8		10	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF, (see Figure 5)		4.6	8		10	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF, (see Figure 4)		1.8	6		8	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		4.3	14		18	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF, (see Figure 5)		6.3	14		18	ns

analog switch characteristics

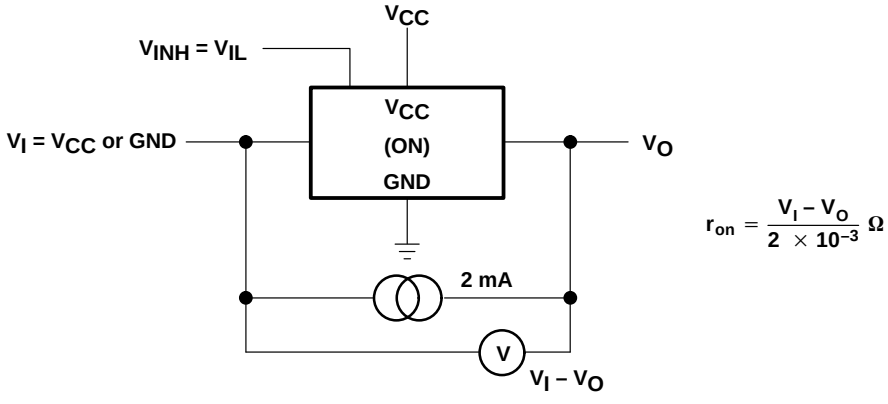
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	T_A = 25°C MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Note 5 and Figure 6)		2.3 V		30		MHz
					3 V		35		
					4.5 V		50		
Crosstalk (between any switches)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Note 6 and Figure 7)		2.3 V		–45		dB
					3 V		–45		
					4.5 V		–45		
Crosstalk (control input to signal output)	INH	COM or Yn	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)		2.3 V		20		mV
					3 V		35		
					4.5 V		65		
Feed-through attenuation (switch off)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (see Note 6 and Figure 9)		2.3 V		–45		dB
					3 V		–45		
					4.5 V		–45		
Sine-wave distortion	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	V_I = 2 V_{p-p}	2.3 V		0.1		%
				V_I = 2.5 V_{p-p}	3 V		0.1		
				V_I = 4 V_{p-p}	4.5 V		0.1		

NOTES: 5. Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads –3 dB.
6. Adjust f_{in} voltage to obtain 0-dBm input.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	5.3	pF

PARAMETER MEASUREMENT INFORMATION



$$r_{on} = \frac{V_I - V_O}{2 \times 10^{-3}}\ \Omega$$

Figure 1. On-State Resistance Test Circuit

PARAMETER MEASUREMENT INFORMATION

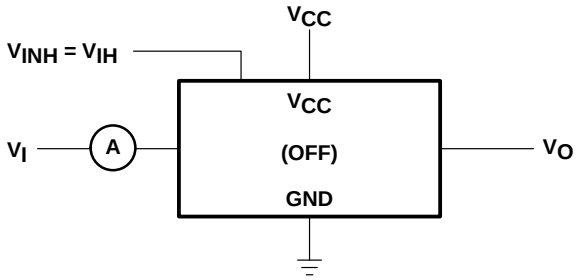


Figure 2. Off-State Switch Leakage-Current Test Circuit

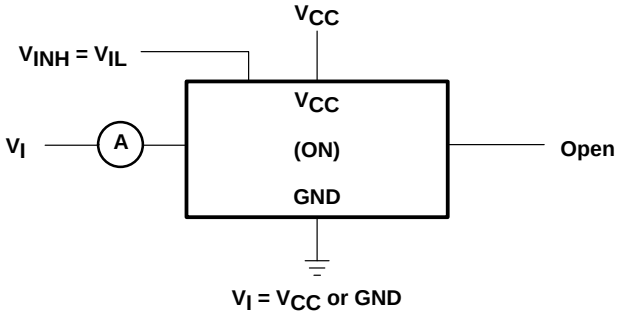


Figure 3. On-State Switch Leakage-Current Test Circuit

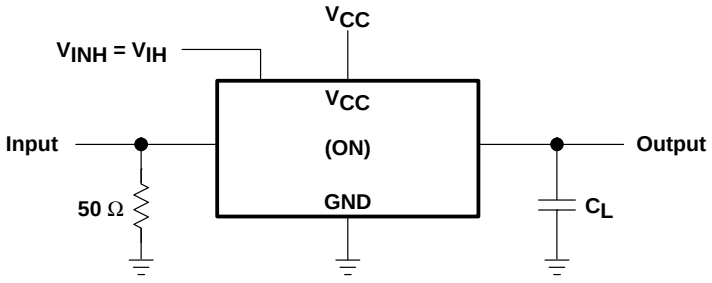
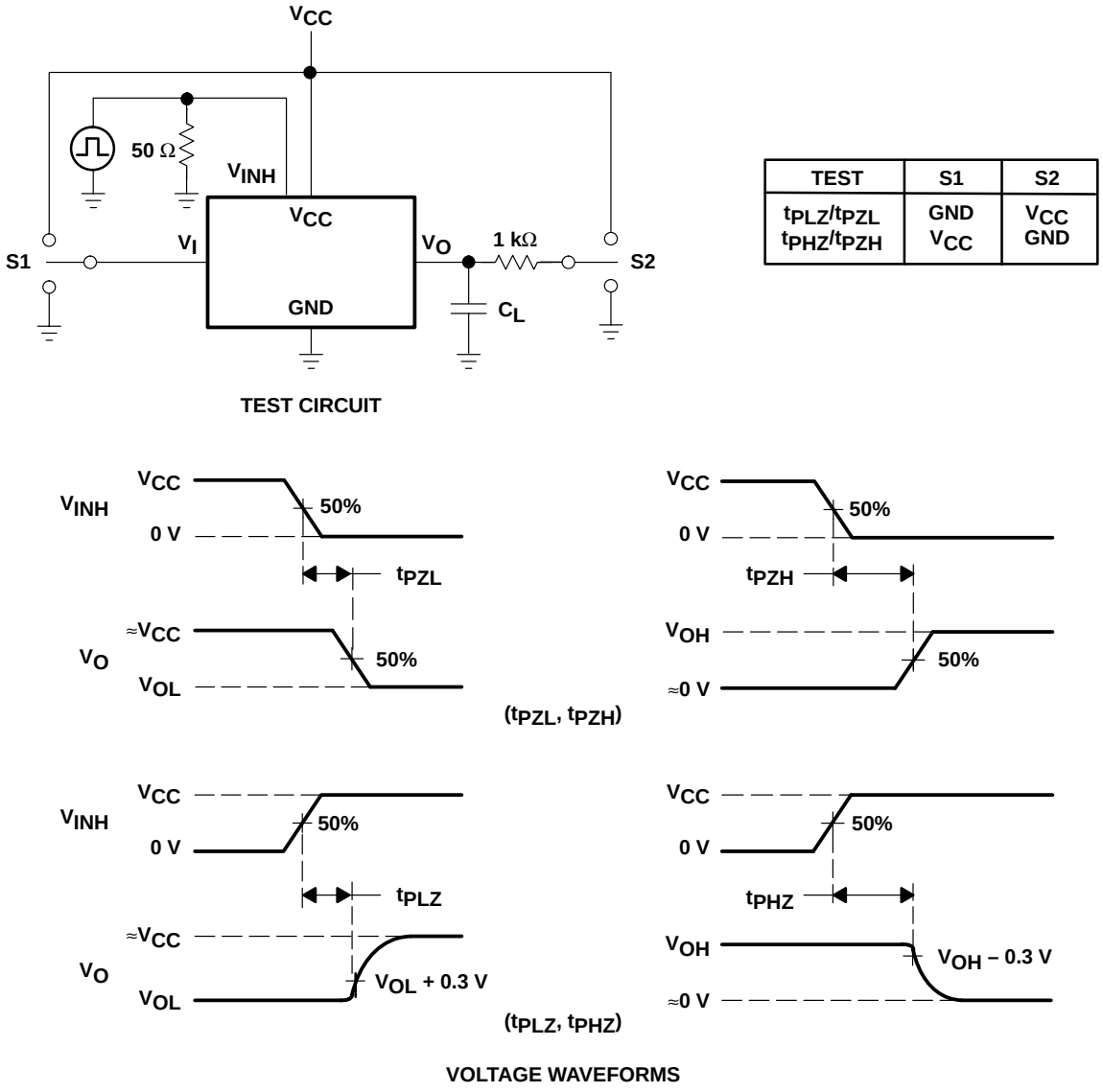


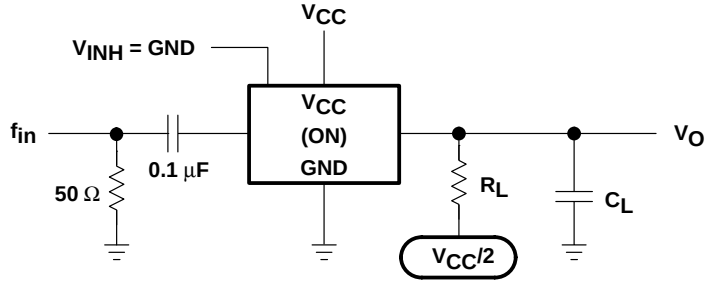
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION



TEST	S1	S2
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	GND V_{CC}	V_{CC} GND

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

PARAMETER MEASUREMENT INFORMATION

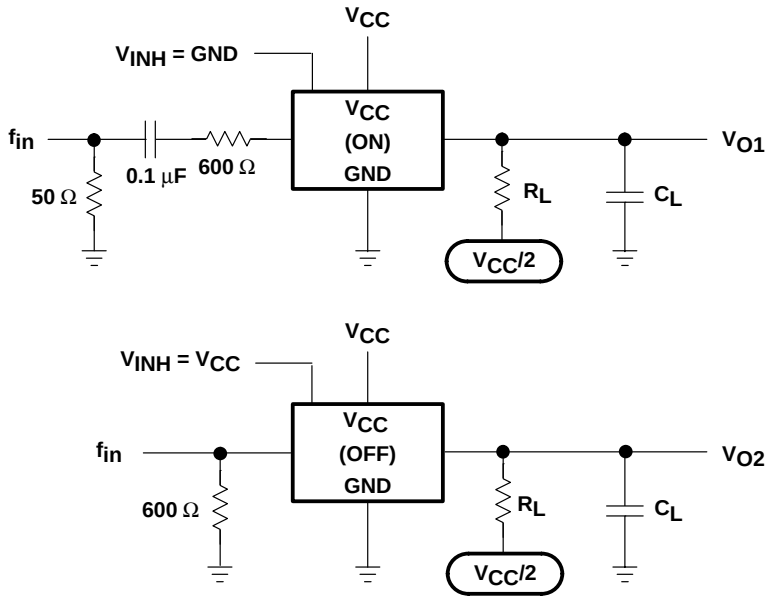


Figure 7. Crosstalk Between Any Two Switches

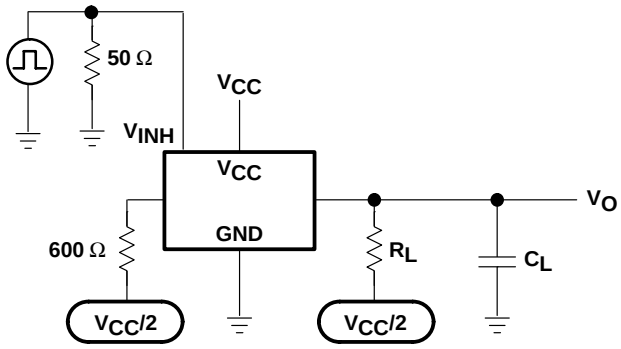


Figure 8. Crosstalk Between Control Input and Switch Output

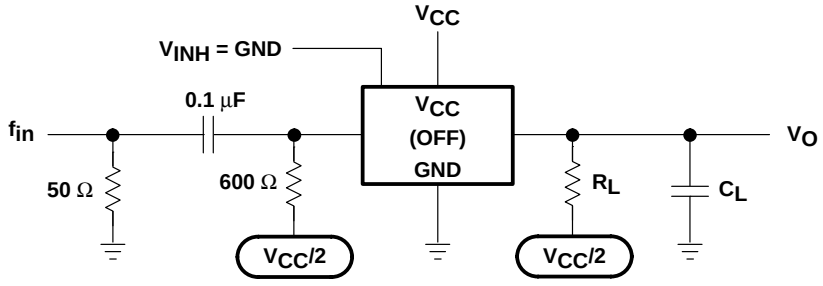


Figure 9. Feed-Through Attenuation (Switch Off)

PARAMETER MEASUREMENT INFORMATION

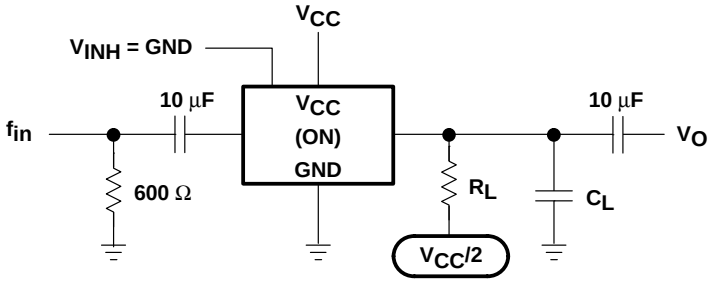
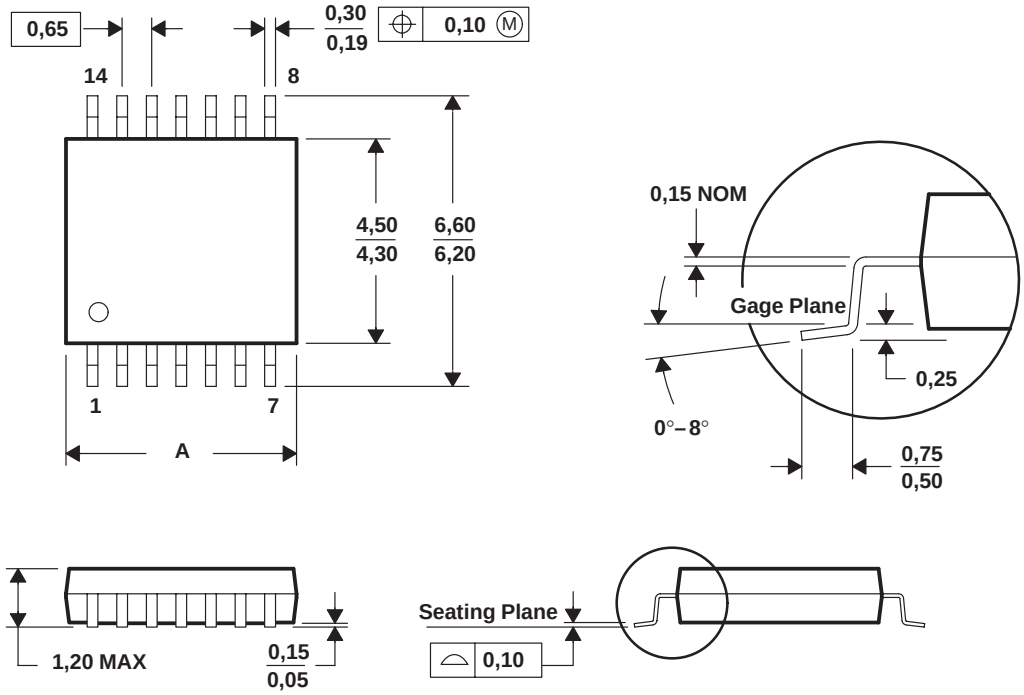


Figure 10. Sine-Wave Distortion

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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