TLK3104SA
QUAD 3.125 Gbps SERIAL TRANSCEIVER

SCAS651B— AUGUST 2000 – REVISED SEPTEMBER 2001

- **Quad 3.125 Gbps per Channel Transceiver Providing 10 Gbps Data Throughput**
- **Selectable Synchronized or Independent Channel Operation**
- **Selectable Transmitter Only, Receiver Only, or Transceiver Functions**
- **Selectable On-Chip 8-Bit/10-Bit Encoding/ Decoding (ENDEC)**
- **Supports IEEE 802.3ae Proposed XGMII Parallel Interface**
- **Supports IEEE 802.3ae Proposed XAUI Serial Interface**
- **Receiver Differential Input Thresholds 200-mV**
- **On-Chip 100-Ω Differential Receiver Termination**
- **No External Filter Capacitors Required**
- **PECL-Compatible Differential Signaling Serial Interface Using Voltage Mode Logic (VML) Driver**
- **Auto-Selects Between 1.8-V HSTL or SSTL_2 Class 1 I/O With On-Chip 50-Ω Series Termination on Outputs**
- **Able to Operate With a Single 2.5-V Power Supply**
- **On-Chip Pseudo-Random Bit Stream (PRBS) Generation and Verification for Self-Test**
- **IEEE 802.3 Management Data Input/Output (MDIO) Interface**
- **IEEE 1149.1 JTAG Test Interface**
- **Hot Plug Protection**
- **Mainstream 250 nm CMOS Technology**
- **Small Footprint 19×19 mm 289 Ball PBGA Package**

description

The TLK3104SA is a flexible four-channel serial backplane transceiver, delivering high-speed bidirectional point-to-point data transmissions to provide up to 10 Gbps of full duplex data transmission capacity. The TLK3104SA supports a broad operating range of serial data rates from 2.5 Gbps to 3.125 Gbps. The primary application of this device is to provide building blocks for developing point-to-point baseband data transmission over controlled impedance media of approximately 50 Ω. The transmission media can be printed-circuit-board traces, copper cables or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling into the lines.

The TLK3104SA performs the parallel-to-serial, serial-to-parallel conversion, and clock extraction functions for a physical layer interface. The TLK3104SA also provides a selectable 8-bit/10-bit (8b/10b) encode/decode function. The serial transmitter and receiver is implemented using differential pseudo-emitter coupled logic (PECL) compatible signaling called voltage mode logic (VML) that eliminates the need for external components.

The four transceivers in the TLK3104SA can be configured as either four separate links, or synchronized together as a single data path. The TLK3104SA supports both the 32-bit data path, 4-bit control, 10 gigabit media independent interface (XGMII) and the extended auxiliary unit interface (XAUI) currently proposed in the IEEE 802.3ae 10 gigabit ethernet task force. Figure 1 shows an example system block diagram for the TLK3104SA used as an XGMII extended sublayer (XGXS) device to provide an additional trace distance on PCB for data being transferred between the switching fabric and optical transceiver modules.

pin assignments

Pin Out
(Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
17	VDDQ	GND	RDB3	VDDQ	GND	RCB	VDDQ	GND	VREF	GND	VDDQ	RCC	GND	VDDQ	RDC3	GND	VDDQ	17
16	MFA	MFB	RDB2	RDB6	RDB9	TCB	TDB5	TDB8	VDDQ	TDC8	TDC5	TCC	RDC9	RDC6	RDC2	MFC	MFD	16
15	VDDQ	GND	RDB1	RDB5	RDB8	TDB2	TDB4	TDB7	TDC9	TDC7	TDC4	TDC2	RDC8	RDC5	RDC1	GND	VDDQ	15
14	RDA9	RDA8	RDB0	VDDQ	GND	TDB1	VDDQ	GND	VDDQ	GND	VDDQ	TDC1	GND	VDDQ	RDC0	RDD8	RDD9	14
13	RDA7	RDA6	RDA5	RDB4	RDB7	TDB0	TDB3	TDB6	TDB9	TDC6	TDC3	TDC0	RDC7	RDC4	RDD5	RDD6	RDD7	13
12	VDDQ	GND	RDA4	RDA3	RDA2	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	RDD2	RDD3	RDD4	GND	VDDQ	12
11	RCA	RDA1	RDA0	VDDQ	GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	GND	VDDQ	RDD0	RDD1	RCD	11
10	TCA	TDA9	TDA8	TDA7	TDA6	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	TDD6	TDD7	TDD8	TDD9	TCD	10
9	VDDQ	GND	TDA5	TDA4	TDA3	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	TDD3	TDD4	TDD5	GND	VDDQ	9
8	TDA2	TDA1	TDA0	VDDQ	GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	GND	VDDQ	TDD0	TDD1	TDD2	8
7	VDDA	GNDA	GNDA	VDD	GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	GND	VDD	GNDA	GNDA	VDDA	7
6	VDDA	RXAN	VDDA	TXAN	GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	T–GND	GND	TXDN	VDDA	RXDN	VDDA	6
5	VDDA	RXAP	VDDA	TXAP	GND	GNDA	GNDA	GND	GND	GND	GNDA	GNDA	GND	TXDP	VDDA	RXDP	VDDA	5
4	GNDA	GNDA	GNDA	VDD	VDD	TXBP	TXBN	VDD	VDD	VDD	TXCN	TXCP	VDD	VDD	GNDA	GNDA	GNDA	4
3	TCLK	TDI	LPENA	LPENB	GNDA	VDDA	VDDA	GND	RFCP	GND	VDDA	VDDA	GNDA	LPENC	LPEND	DVAD2	MDIO	3
2	TDO	TMS	CONFIG0	CONFIG1	GNDA	RXBP	RXBN	GND	RFCN	GND	RXCN	RXCP	GNDA	TESTEN	DVAD4	DVAD3	MDC	2
1	TRSTN	RSTN	PSYNC	SYNCEN	GNDA	VDDA	VDDA	VDD	PRBSEN	VDD	VDDA	VDDA	GNDA	CODE	DVAD0	DVAD1	ENABLE	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

system block diagram

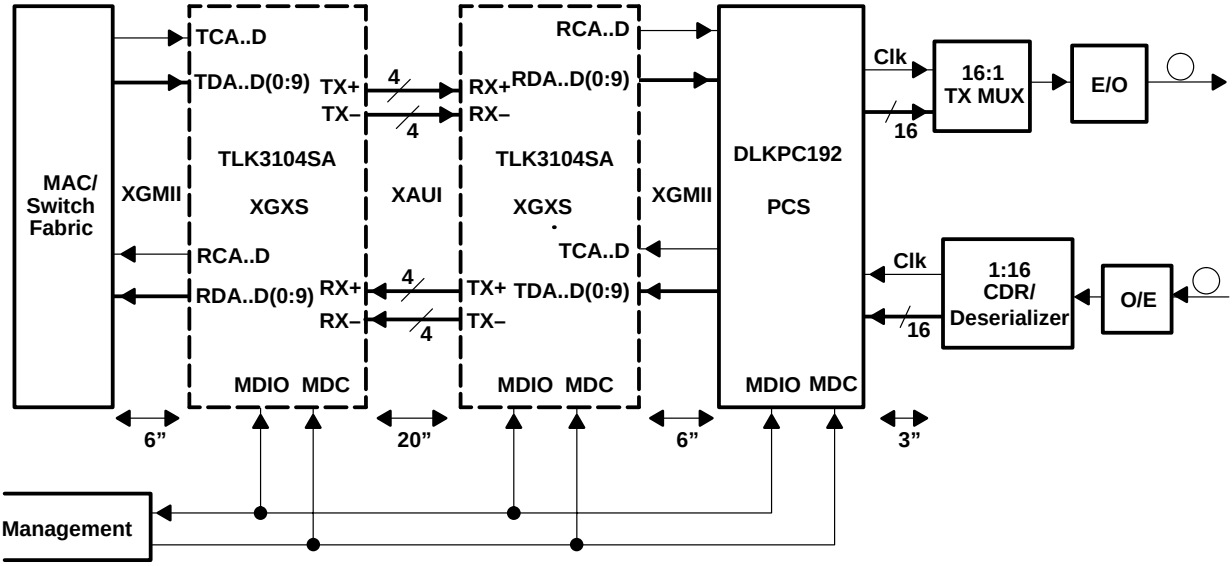


Figure 1. System Block Diagram (Chip-to-Chip Implementation)

Figure 2 shows an example system block diagram for TLK3104SA used to provide the 10 Gbps ethernet physical coding sublayer (as defined in IEEE802.3ae Clause 48) to coarse wave-length division multiplexed (CWDM) optical transceiver

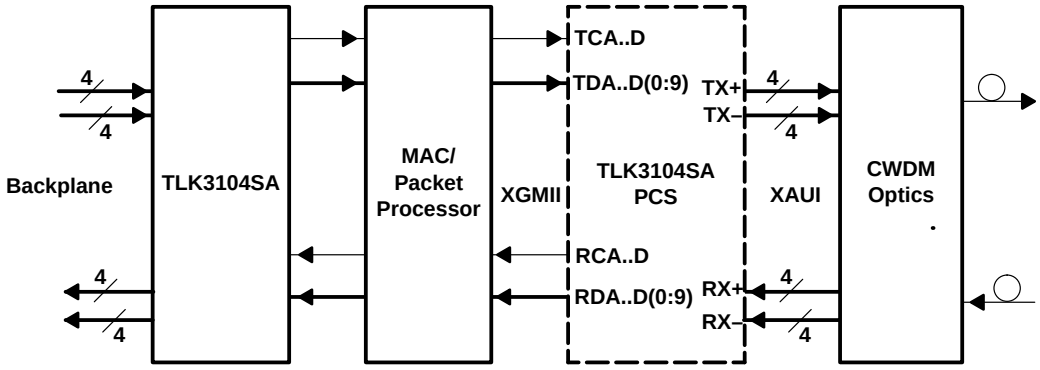


Figure 2. System Block Diagram (PCS Implementation)

system block diagram (continued)

Figure 3 shows an example system block diagram for TLK3104SA used to provide the system backplane interconnect.

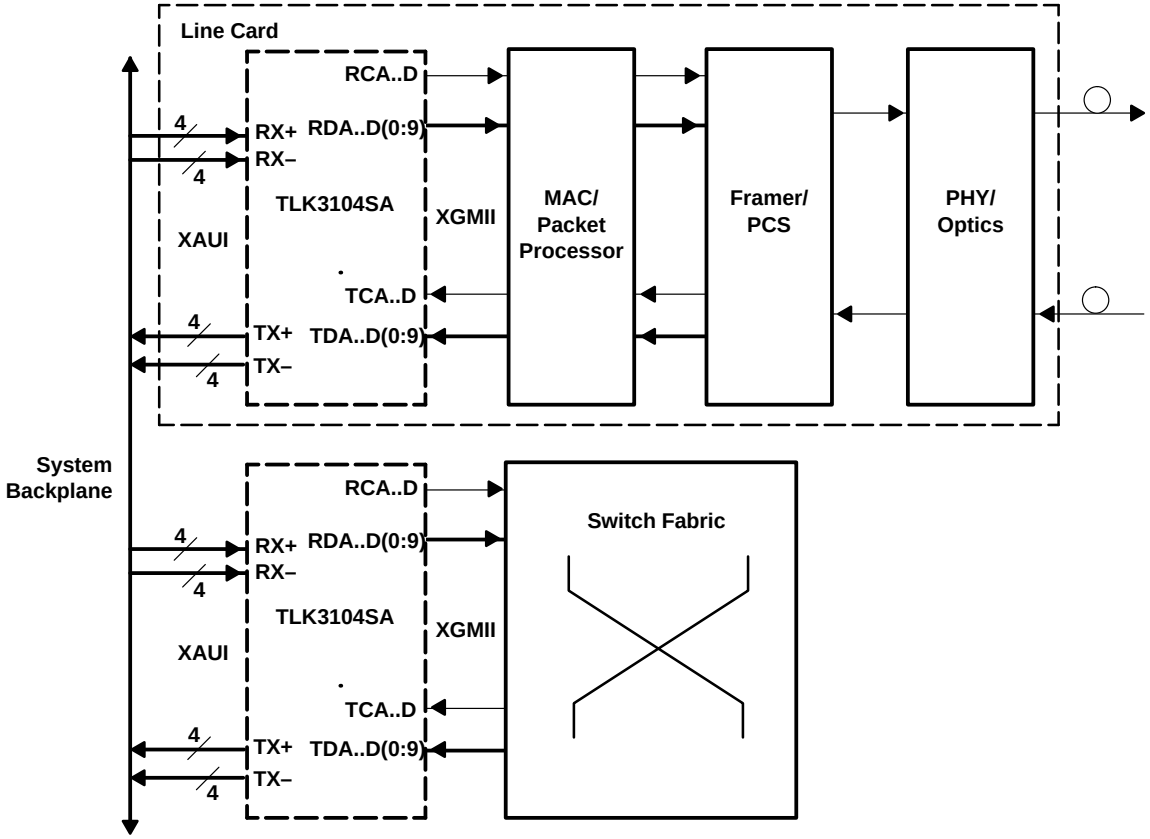


Figure 3. System Block Diagram (Backplane Interconnect Implementation)

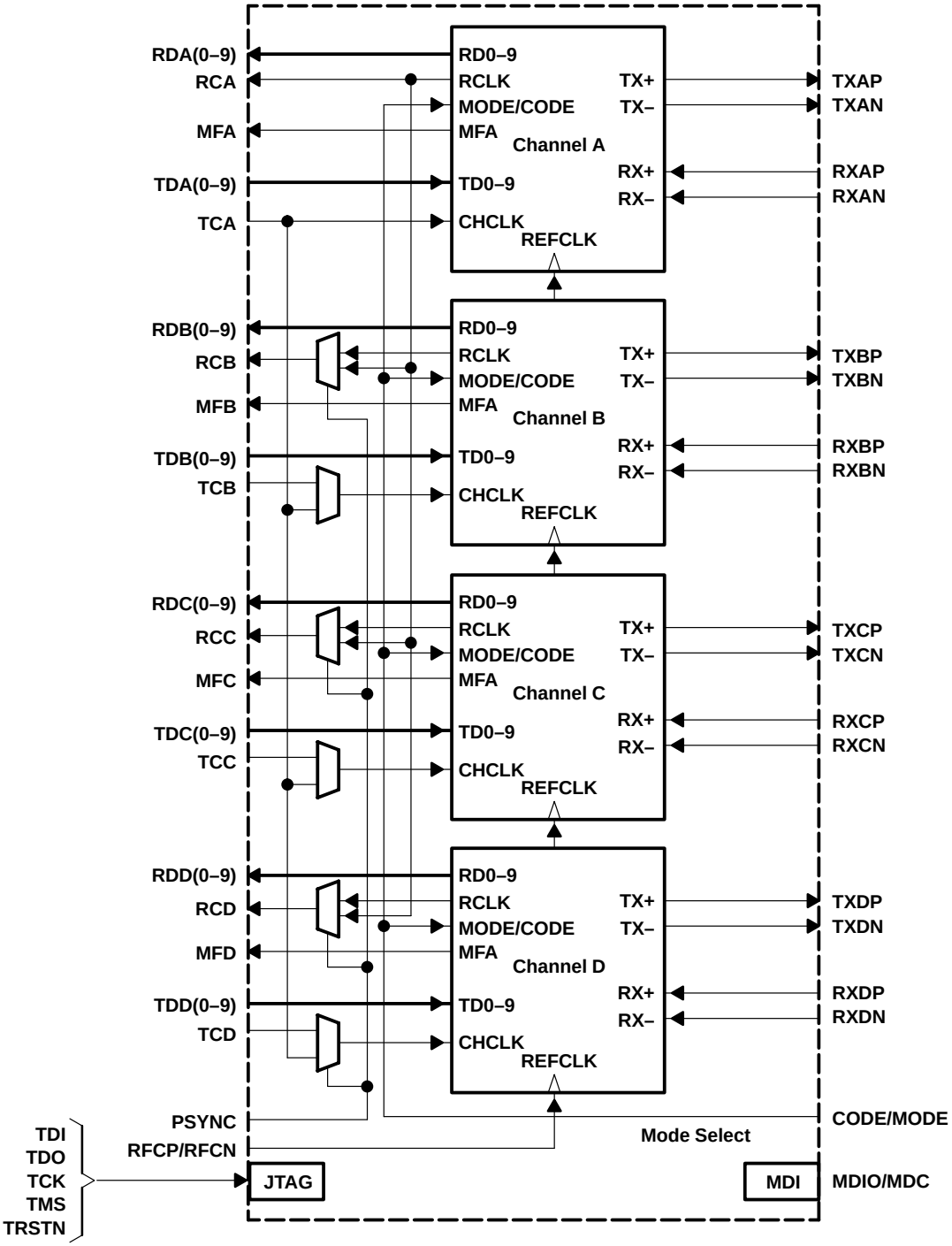
The TLK3104SA supports the IEEE802.3 defined management data input/output (MDIO) Interface to allow ease in configuration and status monitoring of the link. It does not currently support the proposed changes to the management interface in the IEEE P802.3ae D2.0 Clause 45.

The TLK3104SA supports the IEEE 1149.1 defined JTAG test port for ease in board manufacturing test. It also supports a comprehensive series of built-in tests for self-test purposes including internal serial loopback and PRBS generation and verification.

The TLK3104SA operates with a single 2.5-V supply and dissipates less than 3.0 watts. The device is packaged in a 19x19 mm, 289-pin plastic ball grid array (PBGA) package and is characterized for operation from 0°C to 70°C.

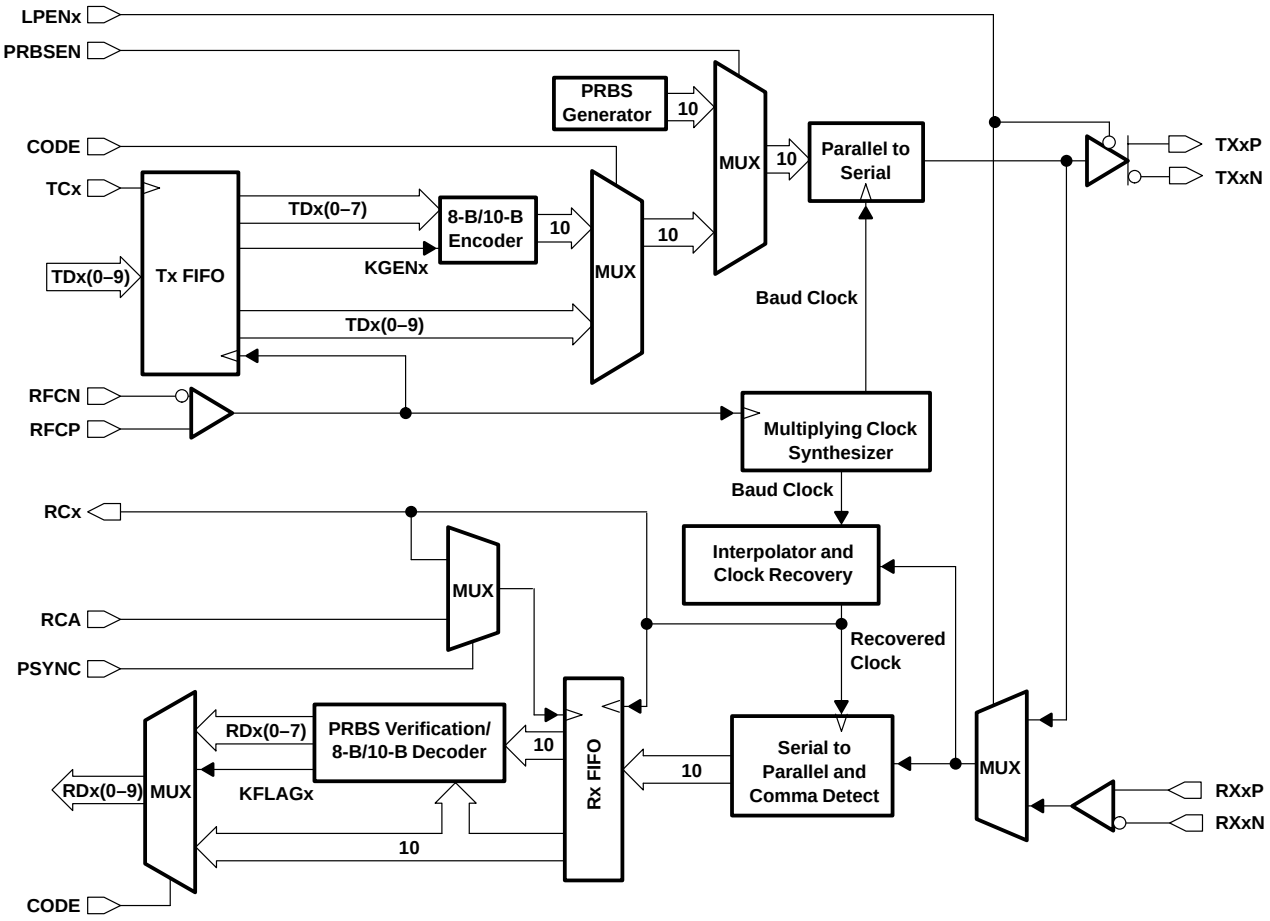
block diagram

The following block diagram provides a high level description of the TLK3104SA. For a detailed diagram of the individual channels, see the detailed block diagram of the individual channel.



block diagram

Following is a more detailed block diagram description of each channel core.



detailed description

The TLK3104SA has four operational interface modes controlled by the state of pins CODE and PSYNC. These operational interface modes are listed in Table 1.

Table 1. Operational Modes

CODE	PSYNC	DESCRIPTION
Low	Low	Four independent serializer/deserializers (SERDES)
Low	High	Four synchronized serializer/deserializers (SERDES)
High	Low	Four independent transceivers with on-chip 8-B/10-B encode/decode
High	High	10 Gigabit ethernet XGXS† transceiver

† XGXS: XGMII extended sublayer

serdes modes

When CODE is low, the TLK3104SA performs serialization and deserialization of encoded data across four ten bit interfaces (TBI) similar to that done in fibre channel and 802.3z gigabit ethernet SERDES devices. The channels can be synchronized to allow use of one transmit data clock and one receive data clock.

detailed description (continued)

10 Gbps ethernet transceiver modes

When CODE is high, the TLK3104SA supports the 32-bit data path, 4-bit control, 10 gigabit media independent interface (XGMII) and full encoding scheme currently proposed in the IEEE 802.3ae 10 gigabit ethernet task force. In these modes, the TLK3104SA performs the serialization/deserialization and channel synchronization function of an extended auxiliary unit interface (XAUI) also currently proposed in the IEEE 802.3ae 10 gigabit ethernet task force.

The TLK3104SA is intended as a prestandard XAUI transceiver. The device supports most of the functions defined in clause 47 and 48 of the IEEE 802.3ae proposed 10 gigabit ethernet draft 2.0 standard. However, some functions that have been included in the current draft of the standard are not currently supported in the TLK3104SA. These are:

- Clock Tolerance Compensation—The TLK3104SA currently does not compensate for differences in frequency between the reference clock and the incoming serial data as defined in P802.3ae D2.0 clause 48.
- XAUI Interpacket Gap Management—The TLK3104SA currently does not generate /A/, /K/, and /R/ codes for bit and channel alignment on the XAUI interface as defined in P802.3ae D2.0 clause 48.
- Remote Fault/Local Fault Reporting—The TLK3104SA currently does not report local or remote faults on the XGMII or report faults as 0xFE as defined in P802.3ae D2.0 clause 46.
- MDIO Timing and Registers—The TLK3104SA currently does not support the timing and register extensions for the management data input/output interface as defined in P802.3ae D2.0 clause 45.
- HSTL Class 1 voltage levels—The TLK3104SA currently does not support HSTL class 1 voltage levels on the XGMII as defined in P802.3ae D2.0 clause 46.

parallel interface clocking

There are two clocking choices selectable via the PSYNC pin detailed in Table 2. Under channel sync mode (PSYNC = high), TCA is used as the transmit data clock for all four channels. Under independent channel mode (PSYNC = low), each channel uses its own transmit data clock (TCA–TCD) to latch data into the TLK3104SA. A data FIFO is placed in the transmit data path to resolve any phase difference between the transmit data clocks and differential reference clock, RFCP/N.

Table 2. Parallel Interface Clocking Modes

PSYNC	PARALLEL INTERFACE CLOCKING OPERATION
Low	Independent channel mode. TC[A–D]/RC[A–D] are used to clock in/out each individual channel.
High	Channel sync mode. TCA/RCA are used to clock in/out all channels of data.

On the receive data path, in independent channel mode, the data for each channel is output referenced to each channel's extracted receive clock. In channel sync mode, the data on all channels are synchronized and output referenced to the extracted receive clock for channel A, RCA. A FIFO is enabled in the parallel receive data path on each channel to compensate for channel skew and clock phase tolerance differences between the recovered clocks for each channel and the receive output clock, RCA. This FIFO has a total depth of eleven bytes.

parallel interface data

There are two data mode choices selectable via the CODE pin detailed in Table 3. In SERDES mode, the transmit data bus for each channel accepts 10-bit wide 8-B/10-B encoded data at the TDx[0..9] pins. Data is latched on the rising and falling edge of the transmit data clock. The 8-B/10-B encoded data is then phase aligned to the reference clock (RFCP/RFCN), serialized, then transmitted sequentially beginning with bit 0 (TDx0) over the differential high-speed serial transmit pins.

parallel interface data (continued)

In SERDES mode, the receive data bus for each channel outputs 10-bit wide 8-B/10-B encoded data on RDx[0..9]. The 8-B/10-B encoded data input to the differential high-speed serial receive pins is deserialized with the first bit (bit 0) output on RDx0 and the last bit (bit 9) output on RDx9. Data is output relative to both the rising and falling edge of the receive clock.

Table 3. Parallel Data Modes

CODE	PARALLEL INTERFACE DATA OPERATION
Low	SERDES mode. On-chip 8-B/10-B encoder/ decoder is disabled. Data on TDx[0..9] and RDx[0..9] is treated as 8-B/10-B encoded data.
High	Transceiver mode. Enables 8-B/10-B encode/decode for each channel. Data TDx[0..7] and RDx[0..7] is treated as uncoded data. TDx8 is used as the K-character generator control. RDx8 is the K-character indicator to the host device. Data on TDx9 is ignored. RDx9 asserts high on either a disparity or code error.

In transceiver mode, the transmit data bus for each channel accepts 8-bit wide parallel data at the TDx[0..7] pins. Data is sampled on the rising and falling edge of the transmit clock as shown in Figure 4. The data is first aligned to the reference clock (RFCP/RFCN), then 8-B/10-B encoded and passed to the serializer. The generation of K-characters on each channel is controlled by TDx8(KGEN). When KGEN is asserted along with the 8 bits of data TDx[0..7], the appropriate 8-B/10-B K-character is transmitted.

In transceiver mode, the receive data bus for each channel outputs 8-bit wide parallel data on RDx[0..7]. Reception of K-characters is reported on RDx8 (KFLAG). When KFLAG is asserted, the 8 bits of data on RDx[0..7] should be interpreted as a K-character. If an error is uncovered in decoding the data, KFLAG and RDx9 (RX_ER) are asserted high and all 1s (0xFF) are placed on the receive data bus for that channel.

transmit data bus timing

For each channel, the transmitter portion of the TLK3104SA latches the data on transmit data bus TDx[0..9] on both the rising and falling edges of the transmit data clock, as shown in Figure 4. Depending on the state of PSYNC pin the transmit data clock is either TCA (channel sync mode) or the individual transmit channel clocks, TCA–TCD (independent channel mode). When in the channel sync mode, signals on TCB, TCC, and TCD are ignored.

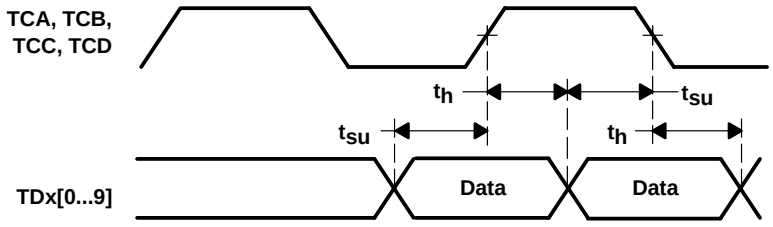


Figure 4. Transmit Interface Timing

transmission latency

For each channel, the data transmission latency of the TLK3104SA is defined as the delay from the rising or falling edge of the selected transmit clock when valid data is on the transmit data pins to the serial transmission of bit 0, as shown in Figure 5. The minimum latency $t_{d(T\_Latency)}$ is 84 bit times; the maximum is 124 bit times. There are approximately 20 bit times required for the 8-B/10-B encoder.

transmission latency (continued)

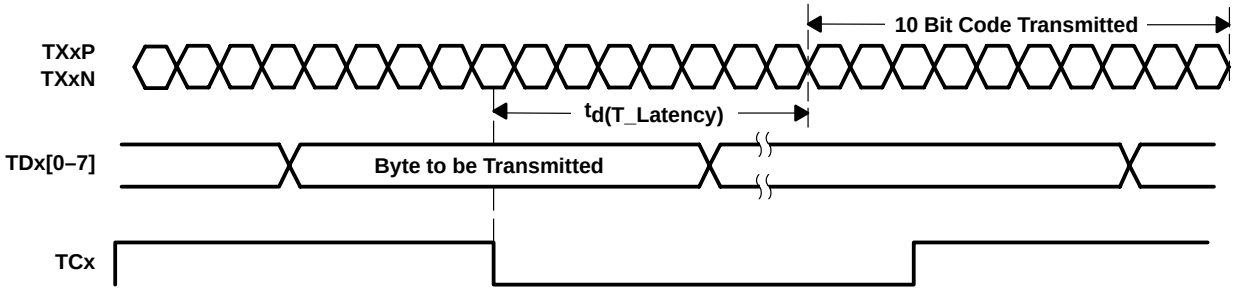


Figure 5. Transmitter Latency

channel clock to serial transmit clock synchronization

The TLK3104SA requires an external differential reference clock, RFCP/N, for the on-chip phase lock loop (PLL) and the clock/data recovery loop. To compensate for arbitrary clock phase tolerance differences between the reference clock and the data aligned to the transmit clock, a small FIFO in the parallel transmit data path on each channel is employed. This FIFO has a depth of four bytes.

The reference clock and the transmit data clock(s) are assumed to be from a common source and only phase misaligned due to different path delays as shown in Figures 6 and 7. The reference clock is multiplied in frequency 10x to produce the internal serialization clock. The internal serialization clock is used to clock out the serial transmit data.

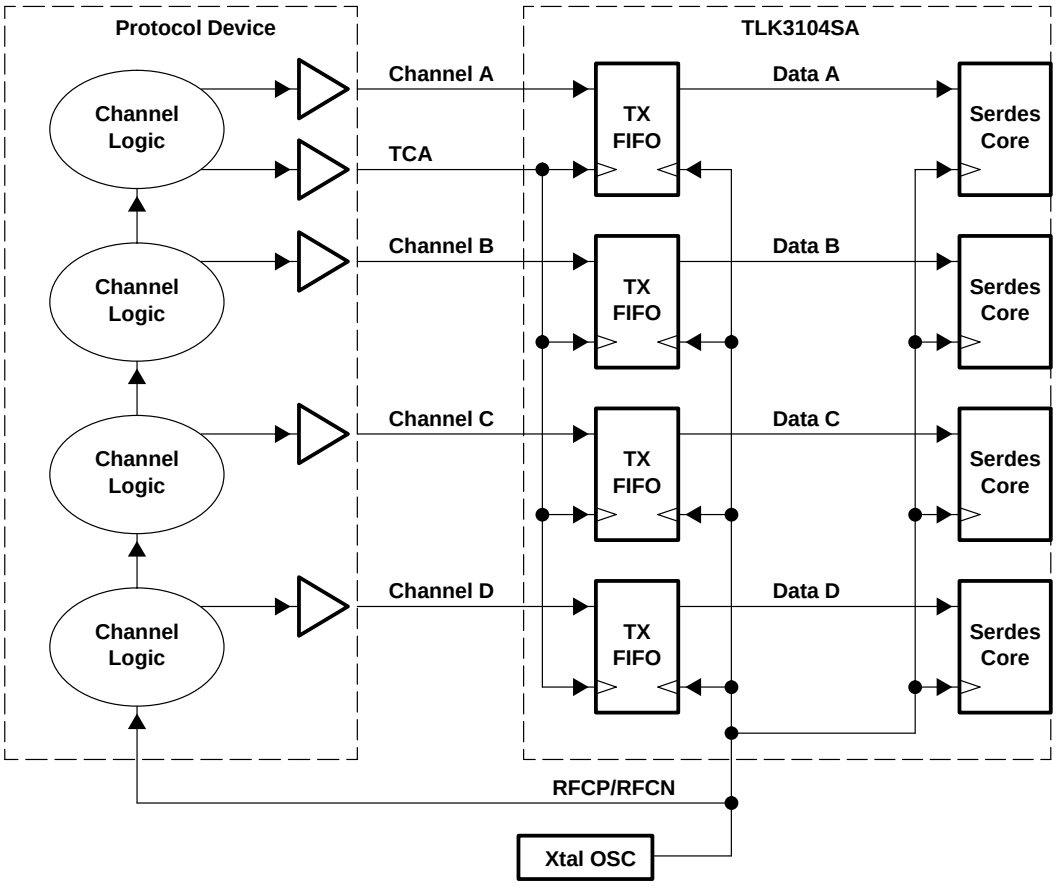


Figure 6. Transmit and Reference Clock Relationship (Channel Sync Mode)

channel clock to serial transmit clock synchronization (continued)

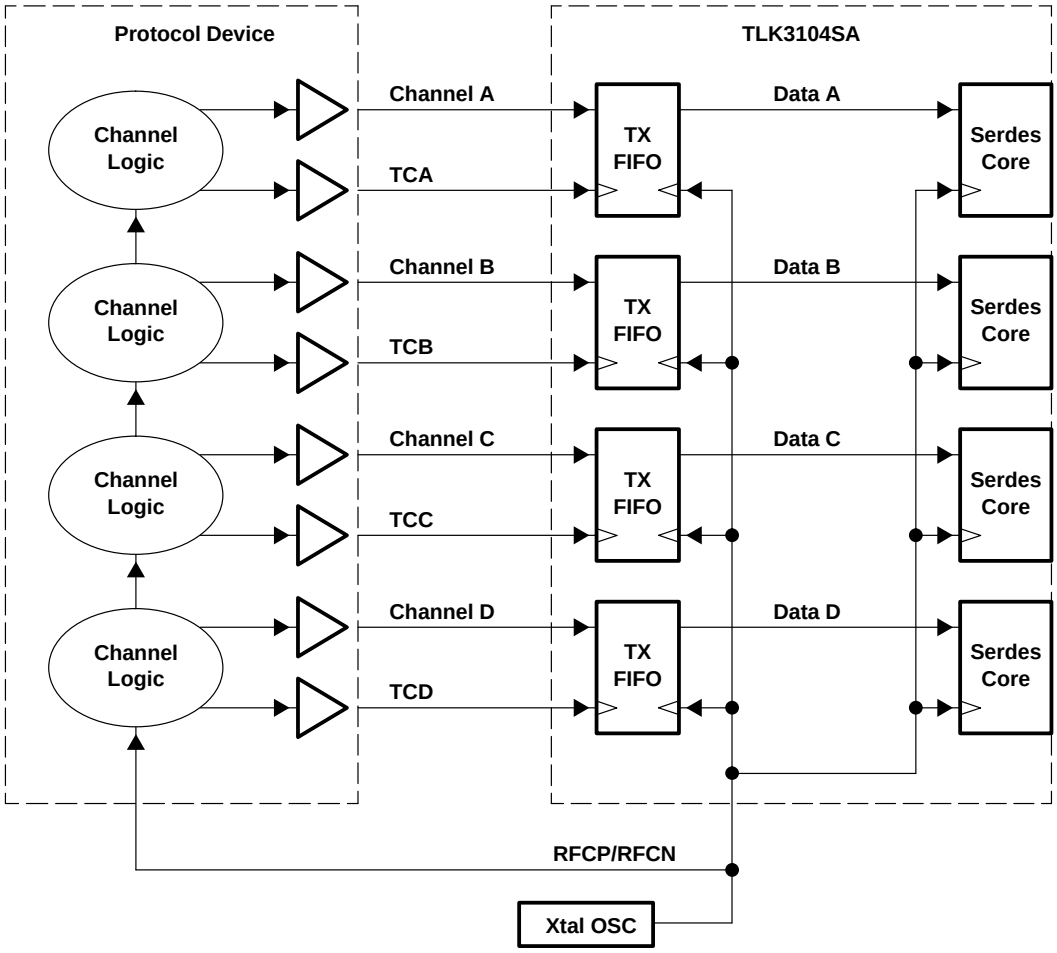


Figure 7. Transmit and Reference Clock Relationship (Independent Channel Mode)

receive data bus timing

For each channel, the receiver portion of the TLK3104SA outputs the recovered deserialized data on receive data bus TDx[0..9] on both the rising and falling edges of the receive data clock, as shown in Figure 8. Depending on the state of PSYNC pin the receive data clock is either RCA (channel sync mode) or the individual receive channel clocks, RCA–RCD (independent channel mode). When in the channel sync mode, RCB, RCC, and RCD pins are held low.

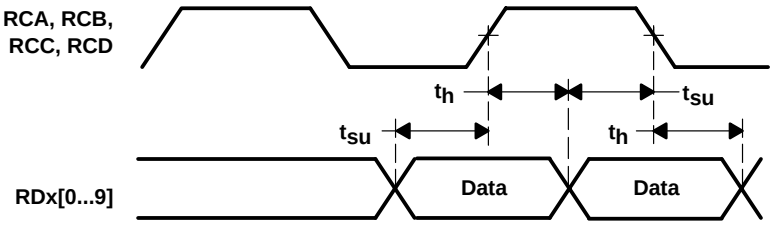


Figure 8. Receive Interface Timing

detailed description (continued)

data reception latency

For each channel, the serial-to-parallel data latency is the time from when the first bit arrives at the receiver input until it is output in the aligned parallel word with RDx0 received as first bit, as shown in Figure 9. The minimum latency $t_{d(R\_Latency)}$ is 46 bit times; the maximum is 166 bit times. There is approximately 20 bit times required for the 8-B/10-B decoder.

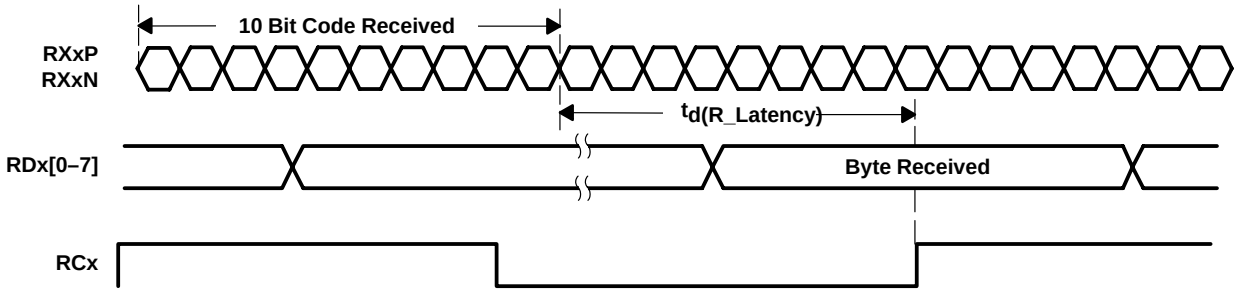


Figure 9. Receiver Latency

auto detectable 1.8 V HSTL/SSTL_2 class 1 I/O

The transmit and receive data bus of the TLK3104SA are compatible with both high-speed transfer logic (HSTL) scaled to 1.8 V supply and stub series terminated logic (SSTL) for 2.5 V class 1 buffer. The TLK3104 determines which buffer technology to use by sensing the voltage level on the VDDQ supply pins at power up. If the voltage on the VDDQ supply is between 2.3 and 2.7 V, the TLK3104 provides the necessary drive current to meet SSTL_2 class 1 requirements. If the voltage on the VDDQ supply is between 1.6 and 2.0 V, the TLK3104 provides 1.8 V HSTL compatible signaling. During normal operation, the voltage level on the VDDQ pins must not change.

All 1.8 V HSTL/SSTL_2 class 1 outputs are internally series terminated to provide direct connection to a 50-Ω transmission line signaling environment (see Figure 26).

8-B/10-B encoder

All true serial interfaces require a method of encoding to insure sufficient transition density for the receiving PLL to acquire and maintain lock. The encoding scheme also maintains the signal dc balance by keeping the number of ones and zeros the same which allows for ac-coupled data transmission. The TLK3104SA uses the 8-B/10-B encoding algorithm that is used by fibre channel and gigabit ethernet. This provides good transition density for clock recovery and improves error checking. The 8-B/10-B encoder/decoder function is enabled for all 4 channels by the assertion of the CODE pin. When enabled, the TLK3104SA internally encodes and decodes the data such that the user actually reads and writes 8-bit data on each channel.

When enabled, the 8-B/10-B encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transition density. This transmission code includes D-characters, used for transmitting data, and K-characters, used for transmitting protocol information. Each K or D character code word can also have both a positive and a negative disparity version. The disparity of a code word is selected by the encoder to balance the running disparity of the serialized data stream.

The generation of K-characters to be transmitted on each channel is controlled by TDx8(KGEN). When KGEN is asserted along with the 8 bits of data TDx[0..7], an 8-B/10-B K-character is transmitted. Similarly, reception of K–characters is reported by RDx8(KFLAG). When KFLAG is asserted, the 8 bits of data on RDx[0..7] must be interpreted as a K-character. The TLK3104SA transmits and receives all of the twelve valid K-characters defined in Table 6. Table 4 provides additional transmit data control coding and descriptions that have been proposed for 10 gigabits per second ethernet. Data patterns put on TDx[0:7] other than those defined in Table 6 when TDx8 is asserted results in an invalid K-character being transmitted which results in an code error at the receiver.

8-B/10-B encoder (continued)

Table 4. Transmit Data Controls

TDx[7:0]	TDx8 (KGENx)	K CODE TRANSMITTED	DESCRIPTION
XX	0	X	Normal data transmission
BC	1	K28.5	IdleE/not-busy
F7	1	K23.7	IdleO/not-busy
3C	1	K28.1	IdleE/busy
1C	1	K28.0	IdleO/busy
FB	1	K27.7	SOP(S)
FD	1	K29.7	EOP(T)
FE	1	K30.7	Error propagation
FC	1	K28.7	Code violation or parity error
7C	1	K28.3	Channel alignment precursor

comma detect and 8-B/10-B decoding

When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to be able to recognize the byte boundary again. Generally this is accomplished through the use of a synchronization pattern. This is a unique a pattern of 1s and 0s that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8-B/10-B encoding contains a character called the comma (b'0011111') which is used by the comma detect circuit to align the received serial data back to its original byte boundary. The decoder detects the K28.5 comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It then converts the data back into 8-bit data. It is important to note that the comma can be either a (b'0011111') or the inverse (b'1100000') depending on the running disparity. The TLK3104SA decoder detects only the (b'0011111') pattern. Therefore, since synchronization is achieved on the positive comma, two consecutive K-codes containing commas are required to assure byte boundary synchronization (see Table 6 for K-codes containing positive commas). Comma detect is not active in PRBS mode.

The reception of K-characters is reported by the assertion of RDx8(KFLAG) on each channel. When a code word error or running disparity error is detected in the decoded data on a channel, RDx9(ERROR DETECT) and KFLAG is asserted and all 1s (0xFF) are placed on the receive data bus for that channel. When a loss of signal (LOS) is detected on the differential receive inputs, ERROR DETECT is low, KFLAG is asserted, and 1s (0xFF) is placed on the receive data bus for that channel, as shown in Table 5. The LOS signal can be disabled using MDIO (see Table 15).

Table 5. Receive Data Controls

EVENT	RECEIVE DATA BUS (RDx[7–0])	KFLAG (RDx8)	ERROR DETECT (RDx9)
Normal data	XX	Low	Low
Normal K-character	Valid K-code (see Table 6)	High	Low
Loss of signal (LOS)	0xFF	High	Low
Code word error or running disparity error	0xFF†	High	High

† Does not comply with P802.3ae D2.0.

comma detect and 8-B/10-B decoding (continued)

Table 6 provides the list of valid K-characters and their bit patterns that the TLK3104SA receives and decode.

Table 6. Valid K Characters

K CHARACTER	RECEIVE DATA BUS (RDx[7–0])	ENCODED K-CODE	
		NEGATIVE RUNNING DISPARITY	POSITIVE RUNNING DISPARITY
K28.0	000 11100	001111 0100	110000 1011
K28.1	001 11100	001111 1001†	110000 0110
K28.2	010 11100	001111 0101	110000 1010
K28.3	011 11100	001111 0011	110000 1100
K28.4	100 11100	001111 0010	110000 1101
K28.5	101 11100	001111 1010†	110000 0101
K28.6	110 11100	001111 0110	110000 1001
K28.7	111 11100	001111 1000†	110000 0111
K23.7	111 10111	111010 1000	000101 0111
K27.7	111 11011	110110 1000	001001 0111
K29.7	111 11101	101110 1000	010001 0111
K30.7	111 11110	011110 1000	100001 0111

† A comma is contained within this K-code

receive synchronization and skew compensation

When the TLK3104SA is configured in channel sync mode, a FIFO is enabled in the parallel receive data path on each channel to compensate for channel skew and clock phase tolerance differences between the recovered clocks for each channel and the receive output clock, RCA, as is shown in Figure 10. This FIFO has a depth of eleven bytes.

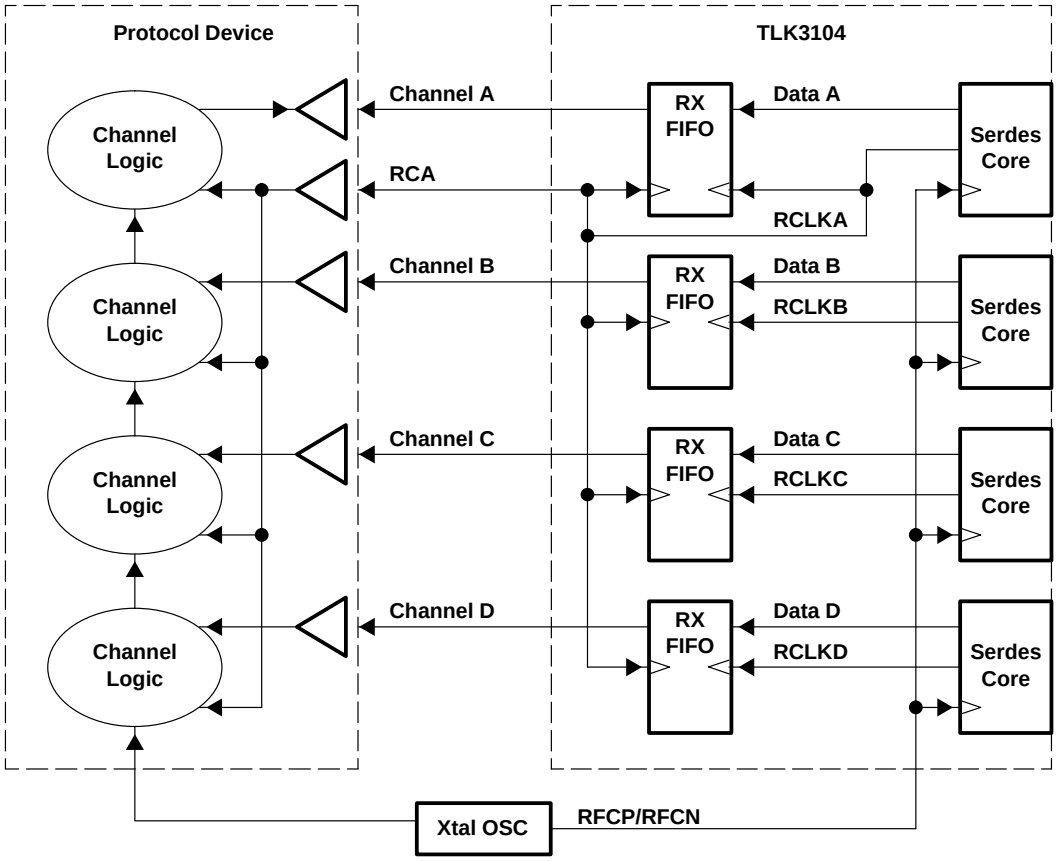


Figure 10. Receive and Reference Clock Relationship (Synchronized Channel Modes)

Channel synchronization is accomplished by alignment of the receive FIFOs on each channel to a K28.3 K-character sent during the interpacket gap (IPG) between data packets or during initial link synchronization. The K28.3 code (referred to as the A or alignment code) is transmitted on the first column following the end of the data packet as shown in Figure 11.

According to IEEE 802.3ae D2.0 clause 48, the channel alignment code is required to be retransmitted on the same data column a minimum of every 16 or maximum of every 32 columns during the IPG or whenever there is no data being transmitted to maintain channel synchronization. Because channel-to-channel skew is predominantly static in nature, the TLK3104SA requires alignment only when system conditions change (such as when line cards are hot plugged).

It is important to note that the protocol device must provide the appropriate data patterns (K28.3, K28.5, and K28.0) on TDx(0:8) pins of the TLK3104SA for the proper generation of the K-characters necessary for lane and channel synchronization.

receive synchronization and skew compensation (continued)

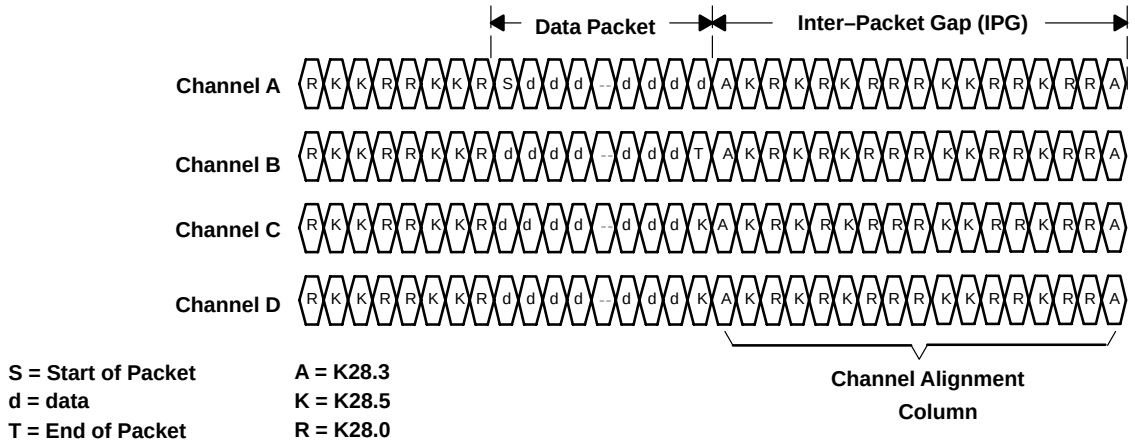


Figure 11. Channel Synchronization Using Alignment Code

According to IEEE 802.3ae D2.0 clause 46, a packet starts in channel A.

The repetition of the A pattern on each serial channel allows the FIFOs to remove or add the required phase delay to align the data from all four channels for output on a single edge of the receive clock for channel A, RCA, as shown in Figure 12.

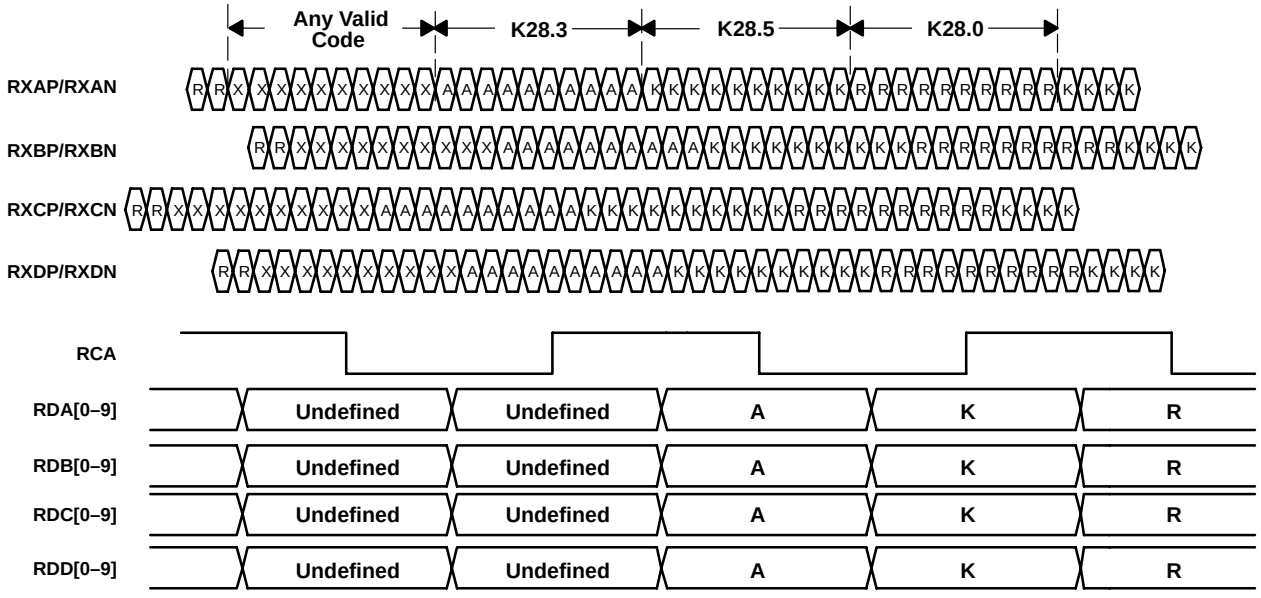


Figure 12. Channel Synchronization Using Alignment Code

receive synchronization and skew compensation (continued)

When the TLK3104SA is configured in independent channel mode, the recovered clocks for each channel are used to output the received data on the parallel interface. Thus, as is shown in Figure 13, in the independent channel modes, no FIFO is enabled.

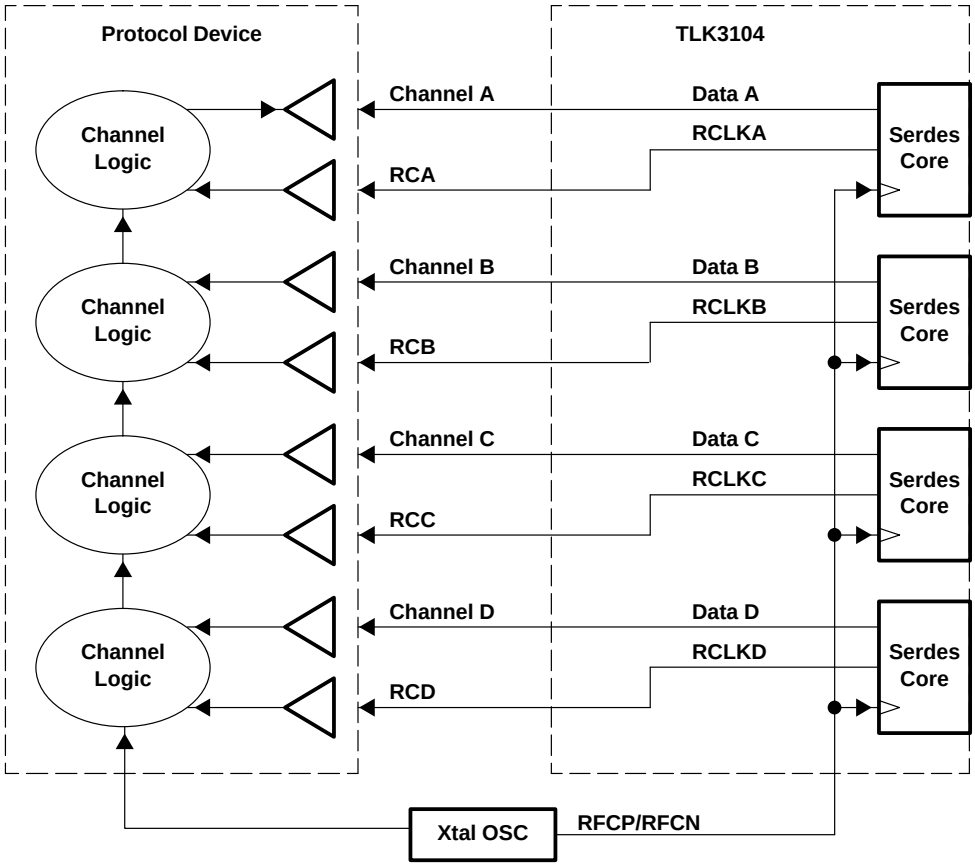


Figure 13. Receive and Reference Clock Relationship (Independent Channel Modes)

parallel to serial

The parallel-to-serial shift register on each channel takes in 10-bit wide data from either the 8-b/10-b encoders, if enabled, or directly from the transmit data bus and converts it to a serial stream. The shift register is clocked by the internally-generated bit clock, which is 10 times the reference clock (RFCP/RFCN) frequency. The least significant bit (LSB) for each channel is transmitted first.

serial to parallel

For each channel, serial data is received on the RXxP/RXxN pins. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within ±100 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. If enabled, the 10-bit wide parallel data is then fed into 8-b/10-b decoders. If the TLK3104SA is configured in one of the synchronized channel modes, the parallel data for each channel is fed into a FIFO buffer where the output is synchronized to RCA. If the TLK3104SA is configured in one of the independent channel modes, the parallel data for each channel is output synchronized to each channel's recovered clock.

high-speed VML output

The high-speed data output driver is implemented using voltage mode logic that offers PECL-compatible differential pair for a 100-Ω differential impedance environment with no external components. The line can be directly coupled or ac-coupled. Refer to Figure 24 and Figure 25 for termination details.

Both current mode logic (CML) and PECL drivers require external components to provide a rising edge (CML) or a falling edge (PECL). The disadvantage of the external edge control is a limited edge rate due to package and line parasitics. In contrast, VML drivers drive and control both the rising and falling edge inside the package and therefore provide optimum performance for increased speed requirements. Furthermore, the VML driver controls the output voltage swing and adjusts automatically for varying load conditions. The PECL-compatible output provides a nominal 850 mV (singled-ended) swing centered at $V_{DDA}/2$. The receiver input is internally biased to facilitate ac-coupling. The receiver internal circuitry sets the common mode voltage to $2\times V/_{DDA}/3$.

When transmitting data across long lengths of PCB trace or cable, the high frequency content of the signal is attenuated due to the skin effect of the media. This causes a smearing of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, the differential swing is increased or preemphasized for the bit immediately following a transition and subsequently reduced or de-emphasized for run lengths greater than one, as shown in Figure 14. This provides additional high frequency energy to compensate for PCB or cable loss. The level of the preemphasis is programmable via MDIO register bits 16-20.4:5. Users can control the strength of the preemphasis to optimize for a specific system requirement. There are two control bits in the user defined registers of MDIO to set the preemphasis level, as shown in Table 7. Refer to Table 15 for MDIO settings.

Table 7. Programmable Preemphasis

PRE1 (reg.16–20.4)	PRE2 (reg. 16–20.5)	PREEMPHASIS LEVEL ($V_{OD}(p)/V_{OD}(d)-1$)†
1	1	Preemphasis disabled
0	1	10%
1	0	20%
0	0	30%

† $V_{OD}(p)$: Magnitude of the voltage swing when there is a transition in the data stream
$V_{OD}(d)$: Magnitude of the voltage swing when there is no transition in the data stream

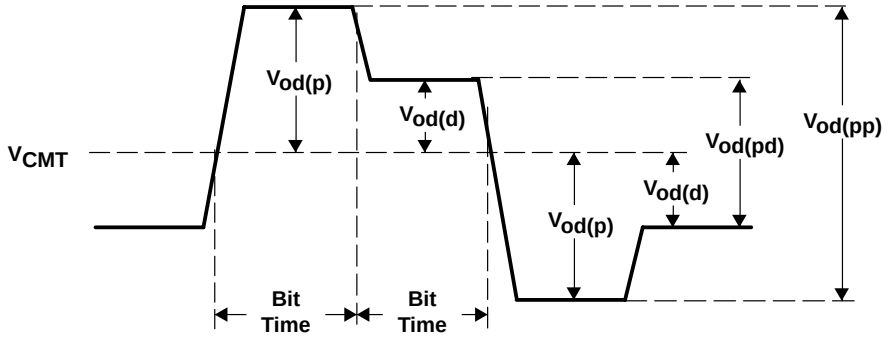


Figure 14. Output Differential Voltage Under Preemphasis

device configuration

The TLK3104SA has three operational configurations controlled by two configuration pins CONFIG0 and CONFIG1. These configurations are listed in Table 8 and controlled by the MDIO interface (refer to Table 15). When the device is put in a certain mode, unused circuit blocks are powered down to conserve the system power.

device configuration (continued)

Table 8. Device Configurations

CONFIG0	CONFIG1	CONFIGURATION
Low	Low	Full duplex transceiver mode—normal operation (default after reset).
Low	High	Transmit only mode—data on high-speed data inputs is ignored. Receive data bus is in a high-impedance state.
High	Low	Receive only mode—high speed data outputs are in a high impedance state. Data on the transmit data bus is ignored.
High	High	Reserved

PRBS generator

The TLK3104SA has a built-in 2^7-1 pseudo-random bit stream (PRBS) self-test function available on each channel. Compared to all 8-B/10-B data pattern combinations, the PRBS is worst case bit pattern. Therefore it is very sufficient to test the link and jitter tolerance. The self test function is a enabled using the PRBSEN pin or setting the PRBS Enable bit [16-20.2] in the MDIO channel configuration registers. When the self-test function is enabled, a PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data on the transmit data bus is ignored during the PRBS test mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a bit error rate tester (BERT), the receiver of another TLK3104SA channel, or looped back to the receive input of the same channel. Since the PRBS is not really random but a predetermined sequence of ones and zeros, the data can be captured and checked for errors by a BERT.

Result reporting of the PRBS test (PRBS_PASS) is available on each receive channel multifunction (MF[A-D]) pin. To enable the report of the PRBS tests, please refer to register 16.10:9. When PRBSEN = high and SYNCEN = high, then PRBS_PASS goes low and stay low on the first occurrence of a bit error. Toggling SYNCEN low then high resets the PRBS_PASS latch. If SYNCEN = low, then PRBS_PASS represents bit errors in real time. Basically, whenever a bit error is detected, the PRBS_PASS goes low for one recovered clock, RCx, half cycle.

MDIO management interface

The TLK3104SA supports the management data input/output (MDIO) Interface as defined in clause 22 of the IEEE 802.3 ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK3104SA is possible without use of this interface since all of the essential signals necessary for operations are accessible via the device pins. However, some additional features are accessible only through the MDIO.

The MDIO management interface consists of a bidirectional data path (MDIO) and a clock reference (MDC). The timing required to read from the internal registers is shown in Figure 15. The timing required to write to the internal registers is shown in Figure 16.

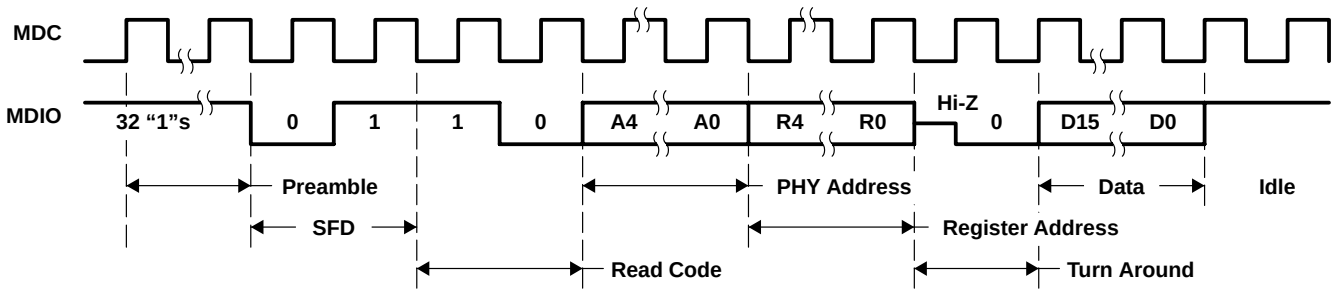


Figure 15. Management Interface Read Timing

MDIO management interface (continued)

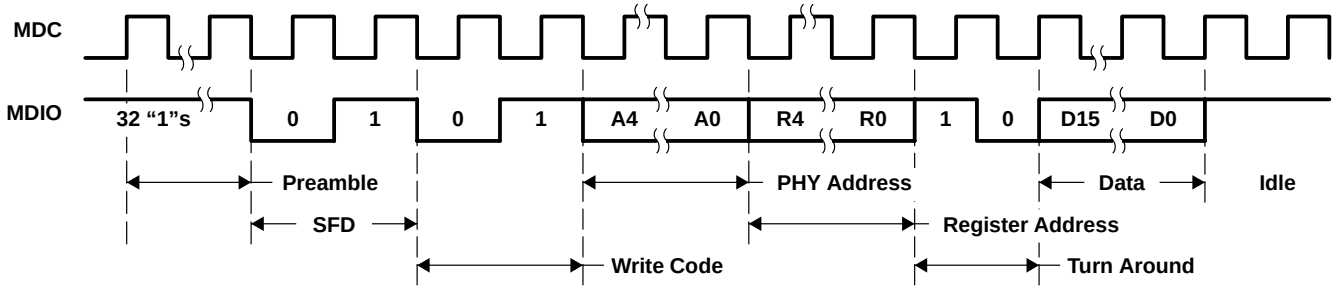


Figure 16. Management Interface Write Timing

The MDIO Interface allows up to 32 (16-bit) internal registers. Sixteen registers are defined by the IEEE 802.3 clause 22 specification. Additional registers are allowed for expanded functionality. The TLK3104SA implements five IEEE defined registers. The TLK3104SA also implements seven registers for expanded functionality. Both the IEEE defined registers and the expanded functionality registers are outlined in Table 9.

Table 9. MDIO Registers

REGISTER ADDRESS	REGISTER NAME	DEFINITION
0	Control	IEEE 802.3 Defined. See Table 10
1	Status	IEEE 802.3 Defined. See Table 12
2,3	PHY identifier	IEEE 802.3 Defined. See Tables 12 and 13
4-14	Not applicable	
15	Extended status	IEEE 802.3 Defined. See Table 14
16	Global configuration	See Table 15
17:20	Channel A-D configuration	See Tables 16 through 19
21	Reserved	Reserved
22	Channel status	See Table 20
23	Channel sync status	See Table 21

Table 10. Control Register Bit Definitions (Register 0)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
0.15	Reset	Logically ORed with the inverse of RSTN pin. 1= Global resets including FIFO clear 0= Normal operation	Read/Write Self Clearing†
0.14	Loopback	1=Enable loopback mode on all channels. 0=Disable loopback mode on all channels (default).	Read/Write
0.13	Speed selection (LSB)	Not applicable. Read returns a 1.	Read only‡
0.12	Auto-negotiation enable	Not applicable. Read returns a 0.	Read only†
0.11	Power down	Logically ORed with the inversion of the ENABLE pin. 1 = Power down mode is enabled. 0 = Normal operation (default).	Read/Write
0.10	Isolate	Not applicable. Read returns a 0.	Read only†
0.9	Restart auto-negotiation	Not applicable. Read returns a 0.	Read only†
0.8	Duplex mode	Only full duplex is supported. Write is ignored, read returns a 1.	Read only†
0.7	Collision test	Not applicable. Read returns a 0.	Read only†
0.6	Speed selection (MSB)	Not applicable. Read returns a 1.	Read only†
0.5:0	Reserved	Write as 0. Ignore on read	-

† After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.
‡ Writing to this bit position is ignored.

MDIO management interface (continued)

Table 11. Status Register Bit Definitions (Register 1)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
1.15:9		Read returns 0	Read only
1.8	Extended status	Read returns 1 indicating extended status information is held in register 15	Read only
1.7	Reserved	Ignore when read	Read only
1.6:3	Various configurations	Read returns 0	Read only
1.2	Link status	Read returns 0	Read only
1.1	Jabber detect	Read returns 0	Read only
1.0	Extended capability	Read returns 1 indicating extended register capability	Read only

Registers 2 and 3 contain the identifier for the 10 Gbps ethernet XGXS device.

The identifier code is composed of bits 3–24 of the 25-bit organizationally unique identifier (OUI) assigned to Texas Instruments by the IEEE. The 6-bit manufacturer model number is unique to the TLK3104SA. The manufacturer revision number denotes the current revision of the TLK3104SA.

Table 12. PHY Identifier Bit Definitions (Register 2)

OUI ADDRESS BITS 3–18															
2.15	**2.14**	**2.13**	**2.12**	**2.11**	**2.10**	**2.9**	**2.8**	**2.7**	**2.6**	**2.5**	**2.4**	**2.3**	**2.2**	**2.1**	**2.0**
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 13. PHY Identifier Bit Definitions (Register 3)

OUI ADDRESS BITS 19–-24						MANUFACTURER MODEL NUMBER						MANUFACTURER REVISION NUMBER			
3.15	**3.14**	**3.13**	**3.12**	**3.11**	**3.10**	**3.9**	**3.8**	**3.7**	**3.6**	**3.5**	**3.4**	**3.3**	**3.2**	**3.1**	**3.0**
0	1	0	1	0	0	0	0	0	1	1	1	0	0	0	0

Table 14. Extended Status Register Bit Definitions (Register 15)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
15.15:12	Various configurations	Read returns 0, write is ignored.	Read only
15.11:0	Reserved		Read only

Writing to register 16 overwrites any previous settings to registers 17–20.

**Table 15. Global Configuration Register Bit Definitions (Register 16)
(see registers 17–20 for individual channel configurations)**

BIT(s)	NAME	DESCRIPTION	READ/WRITE
16.15:11	Reserved	Read returns 0, write is ignored.	Read only
16.10:9	Multifunction pin output	Multifunction (MF[A-D]) pin configuration 16.10 16.9 Output 0 0 HSTL=1, SSTL_2 = 0 (default) 0 1 1 = Comma detected, 0 = data. 1 0 Register bits 22.3:0 (LOS) 1 1 Register bits 22.7:4 (PRBS Pass)	Read/Write
16.8	Loss of signal detection	1 = Enable loss of signal condition described in Table 5 for all channels (default). 0 = Disable this function.	Read/Write
16.7	Configuration: CONFIG1	Configuration bits (see Table 8), default value = 0. When CONFIG1 = low, this bit can be set to 1. When CONFIG1 = high, this bit is read only. Logically ORed with external input CONFIG1	Read/Write
16.6	Configuration: CONFIG0	Configuration bits (see Table 8), default value = 0 When CONFIG0 = low, this bit can be set to 1. When CONFIG0 = high, this bit is read only. Logically ORed with external input CONFIG0	Read/Write
16.5	Preemphasis: PRE2	Programmable preemphasis control (see Table 7), default value = 0	Read/Write
16.4	Preemphasis: PRE1	Programmable preemphasis control (see Table 7), default value = 0	Read/Write
16.3	Reserved	Read returns 0, write is ignored.	Read only
16.2	PRBS enable	1 = Enable pseudo-random bit stream internal generation and verification on all channels 0 = Normal operation (default). When PRBSEN = low, this bit can be set to 1. When PRBSEN = high, this bit is read only. Logically ORed with PRBSEN	Read/Write
16.1	Comma detect enable	1 = Enable K28.5 code detection and bit alignment on all channels (default). 0 = Disable K28.5 code detection on all channels. Logically ANDed with SYNCEN	Read/Write
16.0	Reserved	Read returns 0, write is ignored.	Read/Write

Table 16. Channel A Configuration Registers Bit Definitions (Register 17)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
17.15:11	Reserved	Read returns 0, write is ignored.	Read only
17.10:9	Multifunction pin output	Multi-function (MFA) pin configuration for channel A. 17.10 17.9 MFA output 0 0 HSTL=1, SSTL_2 = 0 (default) 0 1 1 = Comma detected, 0 = data. 1 0 Register bit 22:0 (LOS) 1 1 Register bit 22:4 (PRBS Pass) Logically ORed with register bit 16.10:9	Read/Write
17.8	Loss of signal detection	1 = Enable loss of signal condition described in Table 5 for channel A (default). 0 = Disable this function. Logically ANDed with register bit 16.8	Read/Write
17.7	Configuration: CONFIG1	Configuration bits (see Table 8), default value = 0 When CONFIG1 = low, this bit can be set to 1. When CONFIG1 = high, this bit read only. Logically ORed with external input CONFIG1 and register bit 16.7	Read/Write
17.6	Configuration: CONFIG0	Configuration bits (see Table 8), default value = 0 When CONFIG0 = low, this bit can be set to 1. When CONFIG0 = high, this bit read only. Logically ORed with external input CONFIG0 and register bit 16.6	Read/Write
17.5	Preemphasis: PRE2	Programmable preemphasis control (see Table 7), default value = 0 Logically ORed with register bit 16.5	Read/Write
17.4	Preemphasis: PRE1	Programmable preemphasis control (see Table 7), default value = 0 Logically ORed with register bit 16.4	Read/Write
17.3	Loopback	1 = Enable loopback mode on channel A. 0 = Disable loopback mode on channel A (default). Logically ORed with register bit 0.14 When LPENA = low, this bit can be set to 1. When LPENA = high, this bit read only.	Read/Write
17.2	PRBS enable	1 = Enable pseudo-random bit stream internal generation and verification on channel A 0 = Normal operation (default). Logically ORed with register bit 16.2 When PRBSEN = low, this bit can be set to 1. When PRBSEN = high, this bit read only.	Read/Write
17.1	Comma detect enable	1 = Enable K28.5 code detection and bit alignment on channel A (default). 0 = Disable K28.5 code detection on channel A. Logically ANDed with SYNCEN and register bit 16.1	Read/Write
17.0	Power down	1 = Power down mode is enabled for channel A. 0 = Normal operation (default). Logically ORed with register bit 0.11	Read/Write

Table 17. Channel B Configuration Registers Bit Definitions (Register 18)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
18.15:11	Reserved	Read returns 0, write is ignored.	Read only
18.10:9	Multifunction pin output	Multifunction (MFB) pin configuration for channel B 18.10 18.9 MFB output 0 0 HSTL=1, SSTL_2 = 0 (default) 0 1 1 = Comma detected, 0 = data. 1 0 Register bit 22:1 (LOS) 1 1 Register bit 22:5 (PRBS Pass) Logically ORed with register bit 16.10:9	Read/Write
18.8	Loss of signal detection	1 = Enable loss of signal condition described in Table 5 for channel B (default). 0 = Disable this function. Logically ANDed with register bit 16.8	Read/Write
18.7	Configuration: CONFIG1	Configuration bits (see Table 8), default value = 0 When CONFIG1 = low, this bit can be set to 1. When CONFIG1 = high, this bit read only. Logically ORed with external input CONFIG1 and register bit 16.7	Read/Write
18.6	Configuration: CONFIG0	Configuration bits (see Table 8), default value = 0 When CONFIG0 = low, this bit can be set to 1. When CONFIG0 = high, this bit read only. Logically ORed with external input CONFIG0 and register bit 16.6	Read/Write
18.5	Preemphasis: PRE2	Programmable preemphasis control (see Table 7), default value = 0 Logically ORed with register bit 16.5	Read/Write
18.4	Preemphasis: PRE1	Programmable preemphasis control (see Table 7), default value = 0 Logically ORed with register bit 16.4	Read/Write
18.3	Loopback	1 = Enable loopback mode on channel B. 0 = Disable loopback mode on channel B (default). Logically ORed with register bit 0.14	Read/Write
18.2	PRBS enable	1 = Enable pseudo-random bit stream internal generation and verification on channel B 0 = Normal operation (default). Logically ORed with register bit 16.2 When PRBSEN = low, this bit can be set to 1. When PRBSEN = high, this bit is read only.	Read/Write
18.1	Comma detect enable	1 = Enable K28.5 code detection and bit alignment on channel B (default). 0 = Disable K28.5 code detection on channel B. Logically ANDed with SYNCEN and register bit 16.1	Read/Write
18.0	Power down	1 = Power down mode is enabled for channel B. 0 = Normal operation (default). Logically ORed with register bit 0.11	Read/Write

Table 18. Channel C Configuration Registers Bit Definitions (Register 19)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
19.15:11	Reserved	Read returns 0, write is ignored.	Read only
19.10:9	Multifunction pin output	Multifunction (MFC) pin configuration for channel C 19.10 19.9 MFC output 0 0 HSTL=1, SSTL_2 = 0 (default) 0 1 1 = Comma detected, 0 = data. 1 0 Register bit 22:2 (LOS) 1 1 Register bit 22:6 (PRBS Pass) Logically ORed with register bit 16.10:9	Read/Write
19.8	Loss of signal detection	1 = Enable loss of signal condition described in Table 5 for channel C (default). 0 = Disable this function. Logically ANDed with register bit 16.8	Read/Write
19.7	Configuration: CONFIG1	Configuration bits (see Table 8), default value = 0 When CONFIG1 = low, this bit can be set to 1. When CONFIG1 = high, this bit read only. Logically ORed with external input CONFIG1 and register bit 16.7	Read/Write
19.6	Configuration: CONFIG0	Configuration bits (see Table 8), default value = 0 When CONFIG0 = low, this bit can be set to 1. When CONFIG0 = high, this bit read only. Logically ORed with external input CONFIG0 and register bit 16.6	Read/Write
19.5	Preemphasis: PRE2	Programmable preemphasis control (see Table 7), default value = 0 Logically ORed with register bit 16.5	Read/Write
19.4	Preemphasis: PRE1	Programmable preemphasis control (see Table 7), default value = 0 Logically ORed with register bit 16.4	Read/Write
19.3	Loopback	1 = Enable loopback mode on channel C. 0 = Disable loopback mode on channel C (default). Logically ORed with register bit 0.14	Read/Write
19.2	PRBS enable	1 = enable pseudo-random bit stream internal generation and verification on channel C 0 = Normal operation (default). Logically ORed with register bit 16.2 When PRBSEN = low, this bit can be set to 1. When PRBSEN = high, this bit is read only.	Read/Write
19.1	Comma detect enable	1 = Enable K28.5 code detection and bit alignment on channel C (default). 0 = Disable K28.5 code detection on channel C. Logically ANDed with SYNCEN and register bit 16.1	Read/Write
19.0	Power down	1 = Power down mode is enabled for channel C. 0 = Normal operation (default). Logically ORed with register bit 0.11	Read/Write

Table 19. Channel D Configuration Registers Bit Definitions (Register 20)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
20.15:11	Reserved	Read returns, write is ignored.	Read only
20.10:9	Multifunction pin output	Multifunction (MFD) pin configuration for channel D 20.10 20.9 MFD output 0 0 HSTL=1, SSTL_2 = 0 (default) 0 1 1 = Comma detected, 0 = data. 1 0 Register bit 22:3 (LOS) 1 1 Register bit 22:7 (PRBS Pass) Logically ORed with register bit 16.10:9	Read/Write
20.8	Loss of signal detection	1 = Enable loss of signal condition described in Table 5 for channel D (default). 0 = Disable this function. Logically ANDed with register bit 16.8	Read/Write
20.7	Configuration: CONFIG1	Configuration bits (see Table 8), default value = 0 When CONFIG1 = low, this bit can be set to 1. When CONFIG1 = high, this bit read only. Logically ORed with external input CONFIG1 and register bit 16.7	Read/Write
20.6	Configuration: CONFIG0	Configuration bits (see Table 8), default value = 0 When CONFIG0 = low, this bit can be set to 1. When CONFIG0 = high, this bit read only. Logically ORed with external input CONFIG0 and register bit 16.6	Read/Write
20.5	Preemphasis: PRE2	Programmable preemphasis control (see Table 7), default value = 0 Logically ORed with register bit 16.5	Read/Write
20.4	Preemphasis: PRE1	Programmable preemphasis control (see Table 7), default value = 0 Logically ORed with register bit 16.4	Read/Write
20.3	Loopback	1 = Enable loopback mode on channel D. 0 = Disable loopback mode on channel D (default). Logically ORed with register bit 0.14	Read/Write
20.2	PRBS enable	1 = Enable pseudo-random bit stream internal generation and verification on channel D 0 = Normal operation (default). Logically ORed with register bit 16.2 When PRBSEN = low, this bit can be set to 1. When PRBSEN = high, this bit is read only.	Read/Write
20.1	Comma detect enable	1 = Enable K28.5 code detection and bit alignment on channel D (default). 0 = Disable K28.5 code detection on channel D. Logically ANDed with SYNCEN and register bit 16.1	Read/Write
20.0	Power down	1 = Power down mode is enabled for channel D. 0 = Normal operation (default). Logically ORed with register bit 0.11	Read/Write

Table 20. Channel Status Registers (Register 22)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
22.15	Channel D transmit FIFO collision error	1 = Collision error is detected to cause the transmit FIFO self reset. 0 = No error. (default) After being read, this bit is reset to zero.	Read only
22.14	Channel C transmit FIFO collision error	1 = Collision error is detected to cause the transmit FIFO self reset. 0 = No error. (default) After being read, this bit is reset to zero.	Read only
22.13	Channel B transmit FIFO collision error	1 = Collision error is detected to cause the transmit FIFO self reset. 0 = No error. (default) After being read, this bit is reset to zero.	Read only
22.12	Channel A transmit FIFO collision error	1 = Collision error is detected to cause the transmit FIFO self reset. 0 = No error. (default) After being read, this bit is reset to zero.	Read only
22.11	Channel D decode error	1 = code word or running disparity error detected. 0 = No error. (default) After being read, this bit is reset to zero.	Read only
22.10	Channel C decode error	1 = code word or running disparity error detected. 0 = No error. (default) After being read, this bit is reset to zero.	Read only
22.9	Channel B decode error	1 = code word or running disparity error detected. 0 = No error. (default) After being read, this bit is reset to zero.	Read only
22.8	Channel A decode error	1 = code word or running disparity error detected. 0 = No error. (default) After being read, this bit is reset to zero.	Read only
22.7	Channel D PRBS pass	1 = PRBS testing passes without error (default). 0 = Error is detected during PRBS test. After being read, this bit is reset to one.	Read only
22.6	Channel C PRBS pass	1 = PRBS testing passes without error (default). 0 = Error is detected during PRBS test After being read, this bit is reset to one.	Read only
22.5	Channel B PRBS pass	1 = PRBS testing passes without error (default). 0 = Error is detected during PRBS test After being read, this bit is reset to one.	Read only
22.4	Channel A PRBS pass	1 = PRBS testing passes without error (default). 0 = Error is detected during PRBS test After being read, this bit is reset to one.	Read only
22.3	Channel D LOS output	1 = LOS condition is reported. 0 = No LOS. (default) After being read, this bit is reset to zero.	Read only
22.2	Channel C LOS output	1 = LOS condition is reported. 0 = No LOS. (default) After being read, this bit is reset to zero.	Read only
22.1	Channel B LOS output	1 = LOS condition is reported. 0 = No LOS. (default) After being read, this bit is reset to zero.	Read only
22.0	Channel A LOS output	1 = LOS condition is reported. 0 = No LOS. (default) After being read, this bit is reset to zero.	Read only

Table 21. Channel Synchronization Status Register (Register 23)

BIT(s)	NAME	DESCRIPTION	READ/WRITE
23.15:5	Reserved	Read returns 0.	Read only
23.4	Channel sync flag	1 = Channel synchronization circuit has detected a K28.3/A/code word on all channels. 0 = No /A/ has been detected. After being read, this bit is reset to zero.	Read only
23.3	Channel D receive FIFO collision error	1 = Collision error is detected to cause the receive FIFO self reset. 0 = No error After being read, this bit is reset to zero.	Read only
23.2	Channel C receive FIFO collision error	1 = Collision error is detected to cause the receive FIFO self reset. 0 = No error After being read, this bit is reset to zero.	Read only
23.1	Channel B receive FIFO collision error	1 = Collision error is detected to cause the receive FIFO self reset. 0 = No error After being read, this bit is reset to zero.	Read only
23.0	Channel A receive FIFO collision error	1 = Collision error is detected to cause the receive FIFO self reset. 0 = No error After being read, this bit is reset to zero.	Read only

operating frequency range

The TLK3104SA is optimized for operation at a serial data rate of 3.125 Gbps. The TLK3104SA may operate at a serial data rate between 2.5 Gbps and 3.125 Gbps. The external differential reference clock has an operating frequency from 125 MHz to 156.25 MHz. The reference clock frequency must be within ±100 PPM of the recovered clock and have less than 40 ps of jitter.

powerdown mode

When the ENABLE pin is held low the TLK3104SA goes into a low power quiescent state. In this state, all analog and digital circuitry is disabled. In the power-down mode, the serial transmit and the receive data bus pins for all channels are in a high impedance state.

loop-back testing

The TLK3104SA can provide a self-test function by enabling the internal loop-back path with the assertion of LPENx for each channel or by setting the loopback bit [16-20:3] in the MDIO channel configuration registers. Enabling this pin or bit causes serial transmitted data to be routed internally to the receiver for that channel (see the block diagram of individual channel). The parallel data output can be compared to the parallel input data for that channel to provide functional verification. The external differential output is held in a high-impedance state during the loop-back testing.

power-on reset

Upon application of minimum valid power, the TLK3104SA generates an internal power-on reset. During the power-on reset the receive data pins RDx[0..9] are held high (high-impedance) and the recovered receive clock pins RC[A-D] are held low. The length of the power-on reset cycle is dependent upon the frequency of the reference clock, RFCP/RFCN, but is less than 1 ms in duration.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
CLOCK PINS			
RCA	A11	1.8V HSTL/SSTL_2 Output	Receive data clock, channel A—The data on RDA(0 - 9) is output off the rising and falling edge of RCA. When PSYNC = high, RCA acts as the receive clock for all channels. This pin has internal series termination to provide direct connection to a 50-Ω transmission line.
RCB, RCC, RCD	F17, M17, U11	1.8V HSTL/SSTL_2 Output	Receive data clock, channels B–D—When PSYNC=low, the data on RDx(0–9) is output on the rising and falling edges of the receive clocks. When PSYNC = high, these pins are held low. These pins have internal series termination to provide direct connection to a 50-Ω transmission line.
RFCP/RFCN	J3, J2	PECL compatible or LVDS input	Differential reference input clock—This differential pair accepts LVDS or PECL compatible signals. When interfacing with 3.3-V PECL, ac-coupling is required. An on-chip 100-Ω termination resistor is placed differentially between the pins. Internal biasing is provided.
TCA	A10	1.8V HSTL/SSTL_2 input	Transmit data clock, channel A—The data on TDA(0–9) is latched on the rising and falling edge of TCA. When PSYNC = high, TCA acts as the transmit clock for all channels.
TCB, TCC, TCD	F16, M16, U10	1.8V HSTL/SSTL_2 input	Transmit data clock, channels B–D—When PSYNC=low, the data on TDx(0–9) is latched on the rising and falling edges of the transmit clocks. When PSYNC = high, these pins are undefined.
SERIAL SIDE DATA PINS			
RXAP/RXAN RXBP/RXBN RXCP/RXCN RXDP/RXDN	B5, B6 F2, G2 M2, L2 T5, T6	PECL Compatible Input	Receive differential pairs, channel A–D, High speed serial inputs with on-chip 100-Ω differential termination. Each input pair is terminated differentially across an on-chip 100-Ω resistor (see Figures 23 and 24).
TXAP/TXAN TXBP/TXBN TXCP/TXCN TXDP/TXDN	D5, D6 F4, G4 M4, L4 P5, P6	PECL Compatible Output	Transmit differential pairs, channel A–D, High speed serial outputs.
PARALLEL SIDE DATA PINS			
RDA(0–7)	C11, B11, E12, D12, C12, C13, B13, A13	1.8V HSTL/ SSTL_2 Output	Receive data pins, channel A, Parallel data on this bus is valid on the rising and falling edge of RCA. These pins have internal series termination to provide direct connection to a 50-Ω transmission line.
RDA8	B14	1.8V HSTL/ SSTL_2 Output	Receive data/K-flag, channel A When CODE = low, this pin is the 9th bit of a received 8-B/10-B encoded byte. When CODE = high, this pin acts as the K- character flag. When high, this indicates the data on RDA(0–7) is a valid K–character. Data on this pin is valid on the rising and falling edge of RCA. These pins have internal series termination to provide direct connection to a 50-Ω transmission line.
RDA9	A14	1.8V HSTL/ SSTL_2 Output	Receive data pin/error detect, channel A, When CODE = low, this pin is the 10th bit of a 8-B/10-B encoded byte. When CODE = high, this pin goes high to signify the occurrence of either a disparity error or an invalid code word during the decoding of the received data. Data on this pin is valid on the rising and falling edge of RCA. These pins have internal series termination to provide direct connection to a 50-Ω transmission line.
RDB(0–7)	C14, C15, C16, C17, D13, D15, D16, E13	1.8V HSTL/ SSTL_2 Output	Receive data pins, channels B–D, When PSYNC=low, parallel data on these buses is valid on the rising and falling edge of the recovered data clock (RCB, RCC, or RCD). When PSYNC=high, data on each bus is valid on the rising and falling edge of RCA. These pins are series terminated to provide direct connection to a 50-Ω transmission line.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
PARALLEL SIDE DATA PINS (CONTINUED)			
RDC(0–7)	R14, R15, R16, R17, P13, P15, P16, N13	1.8V HSTL/ SSTL_2 Output	valid on the rising and falling edge of the recovered data clock (RCB, RCC, or RCD). When PSYNC=high, data on each bus is valid on the rising and falling edge of RCA. These pins are series terminated to provide direct connection to a 50-Ω transmission
RDD(0–7)	R11, T11, N12, P12, R12, R13, T13, U13	1.8V HSTL/ SSTL_2 Output	valid on the rising and falling edge of the recovered data clock (RCB, RCC, or RCD). When PSYNC=high, data on each bus is valid on the rising and falling edge of RCA. These pins are series terminated to provide direct connection to a 50-Ω transmission
RDB8 RDC8 RDD8	E15, N15, T14	1.8V HSTL/ SSTL_2 Output	Receive data/K-flag, channels B–D When PSYNC=low, data on this pin is valid on the rising and falling edge of the recovered clock (RCB, RCC, or RCD). When PSYNC=high, data on this pin is valid on the rising and falling edge of RCA. When CODE = low, these pins is the 9th bit of a received 8-B/10-B encoded byte. When CODE = high, these pins act as the K- character flag. When asserted high, this indicates the data on RDx(0–7) is a valid K-character. These pins are series terminated to provide direct connection to a 50-Ω transmission line.
RDB9 RDC9 RDD9	E16, N16, U14	1.8V HSTL/ SSTL_2 Output	Receive data pin/error detect, channels B–D. When PSYNC=low, data on these pins are valid on the rising and falling edge of recovered channel clock (RCB, RCC, RCD). When PSYNC=high, data on these pins are valid on the rising and falling edge of RCA. When CODE = low, these pins are the 10th bit of a 8-B/10-B encoded byte. When CODE = high, these pins provide an error detection flag. The error detect is asserted high to signify the occurrence of either a disparity error or an invalid code word during the decoding of the received data. These pins have internal series termination to provide direct connection to a 50-Ω transmission line.
TDA(0–7)	C8, B8, A8, E9, D9, C9, E10, D10	1.8V HSTL/ SSTL_2 Input	Transmit data pins, channel A, Parallel data on this bus is clocked on the rising and falling edge of TCA.
TDA8	C10	1.8V HSTL/ SSTL_2 Input	Transmit Data/KGEN, channel A When CODE = low, this pin is the 9th bit of a 8-B/10-B encoded byte to be transmitted. When CODE = high, this pin acts as the K-character generator indicator. When high, this pin causes the data on TDA(0–7) to be encoded into a K-character.
TDA9	B10	1.8V HSTL/ SSTL_2 Input	Transmit data pin, channel A, When CODE = low, this pin is the 10th bit of a 8-B/10-B encoded byte. When CODE = high, this pin is ignored.
TDB(0–7)	F13, F14, F15, G13, G15, G16, H13, H15	1.8V HSTL/ SSTL_2 Input	Transmit data pins, channels B–D, When PSYNC=low, parallel data on this bus is clocked on the rising and falling edge of the transmit channel clock (TCB, TCC, TCD). When PSYNC=high, data on these buses is clocked on the rising and falling edge of TCA.
TDC(0–7)	M13, M14, M15, L13, L15, L16, K13, K15		
TDD(0–7)	R8, T8, U8, N9, P9, R9, N10, P10		
TDB8 TDC8 TDD8	H16, K16, R10	1.8V HSTL/ SSTL_2 Input	Transmit data/KGEN, channels B–D, When PSYNC=low, data on this pin is clocked on the rising and falling edge of the transmit channel clock (TCB, TCC, or TCD). When PSYNC=high, data on this pin is clocked on the rising and falling edge of TCA. When CODE = low, these pins are the 9th bit of a 8-B/10-B encoded byte to be transmitted. When CODE = high, these pins act as the K-character generator indicator. When driven high, these pins cause the data on TDx (0–7) to be encoded into a K-character.
TDB9 TDC9 TDD9	J13, J15, T10	1.8V HSTL/ SSTL_2 Input	Transmit data pin, channels B–D, When PSYNC=low, data on this pin is clocked on the rising and falling edge of the transmit channel clock (TCB, TCC, TCD). When PSYNC=high, data on these pins are clocked on the rising and falling edge of TCA. When CODE = low, these pins are the tenth bit of a 8-B/10-B encoded byte. When CODE=high, these pins are ignored.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
JTAG TEST PORT INTERFACE			
TCLK	A3	LVTTL Input	JTAG clock. TCLK is used to clock state information and test data into and out of the device during the operation of the test port.
TDI	B3	LVTTL Input†	JTAG input data. TDI is used to serially shift test data and test instructions into the device during the operation of the test port.
TDO	A2	LVTTL Output	JTAG output data. TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state.
TMS	B2	LVTTL Input†	JTAG mode select. TMS is used to control the state of the internal test-port controller.
TRSTN	A1	LVTTL Input	JTAG reset. TRSTN is used to reset the internal JTAG controller.
MANAGEMENT DATA INTERFACE			
DVAD(0–4)	R1, T1, T3, T2, R2	LVTTL Input	Management address. Device address: DVAD(0-4) is the externally set physical address given to this device used to distinguish one device from another.
MDC	U2	LVTTL Input	Management data clock. MDC is the clock reference for the transfer of management data to and from the protocol device.
MDIO	U3	LVTTL I/O	Management data I/O. MDIO is the bidirectional serial data path for the transfer of management data to and from the protocol device.
MISCELLANEOUS PINS			
CODE	P1	LVTTL Input†	Encode enable. When CODE = high, the 8-B/10-B encoder and decoder is enabled.
CONFIG0 CONFIG1	C2, D2	LVTTL Input‡	Configuration pins. These pins put the device under one of the three operation modes: 00–Transceiver mode 01–Transmit only mode 10–Receive only mode 11 – Reserved
ENABLE	U1	LVTTL Input†	Standby enable. When this pin is held low, the device is in a low power state. When high the device operates normally.
LPEN(A–D)	C3, D3, P3, R3	LVTTL Input‡	Internal loop enable. channels A–D. When high, the serial output for each channel is internally looped back to its serial input.
MF(A–D)	A16, B16, T16, U16	1.8V HSTL_/ SSTL_2 Output	Multifunction outputs, channels A–D. The functions of these pins are enabled via the MDIO. Currently defined functions are: 1. Pin indicates 1 for HSTL, 0 for SSTL_2 Signaling (default) 2. LOS (Loss of Signal) for each channel, 3. COMMA_DET (K28.5 character detected) for each channel, and 4. PRBS_STATUS (pseudo-random bit stream test status) for each channel.
PRBSEN	J1	LVTTL Input‡	PRBS enable. When this pin is asserted high, the pseudo-random bit stream generator and comparator circuits are inserted into the transmit and receive data paths on all channels. PRBS_PASS is indicated on the MFx pins once they are enabled using MDIO.
PSYNC	C1	LVTTL Input‡	Channel synchronization enable. When PSYNC = high, all transmit data is latched on the rising and falling edge of TCA, all receive data is valid on the rising and falling edge of RCA.
RSTN	B1	LVTTL Input†	Chip reset (FIFO clear). Pulling this pin low re-centers the transmit skew buffers, receive channel synchronization FIFO's, and resets MDIO flags.
SYNCEN	D1	LVTTL Input†	Comma detect enable. When high, comma detection and byte alignment for all channels is enabled.
TESTEN	P2	LVTTL Input‡	Test mode enable. This pin is used for manufacturing test. This pin should be left unconnected or tied low.

† With 10 kΩ internal pullup
‡ With 10 kΩ internal pulldown

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
VOLTAGE SUPPLY AND REFERENCE PINS			
GND	B17, B15, B12, B9, E5, E6, E7, E8, E11, E14, E17, H2, H3, H17, H14, H5, J5, K2, K3, K17, K14, K5, N5, N6, N7, N8, N11, N14, N17, T17, T15, T12, T9	Ground	Digital logic ground. Supply reference for core logic and SSTL_2 CLASS 1 buffers.
GNDA	B7, C7, A4, B4, C4, E3, E2, E1, F5, G5, L5, M5, N3, N2, N1, R7, R4, T7, T4, U4	Ground	Analog ground. Supply reference for analog circuitry.
T-GND	F6, F7, F8, F9, F10, F11, F12, G6, G7, G8, G9, G10, G11, G12, H6, H7, H8, H9, H10, H11, H12, J6, J7, J8, J9, J10, J11, J12, K6, K7, K8, K9, K10, K11, K12, L6, L7, L8, L9, L10, L11, L12, M6, M7, M8, M9, M10, M11, M12	Ground	Thermal grounds. Electrically connected to GND, these pins provide a thermal path for heat dissipation.
VDDQ	A9, D11, A12, D14, D8, A15, A17, D17, G17, G14, J16, J14, L17, L14, P17, P14, P8, U9, U17, U15, U12, P11	Supply	1.8V HSTL/SSTL_2 CLASS 1 Supply voltage. Nominally 1.8 V for HSTL or 2.5 V for SSTL_2 CLASS 1.
VDD	D7, D4, E4, H1, H4, J4, K1, K4, N4, P4, P7	Supply	Core supply (2.5V), Digital logic power. Provides power for all digital circuitry.
VDDA	A7, A6, A5, C6, C5, F1, F3, G1, G3, L1, L3, M1, M3, R5, R6, U5, U6, U7	Supply	Analog voltage supply (2.5 V). Provides power for all analog circuitry.
VREF	J17	Input	Input voltage reference for 1.8 V HSTL/SSTL_2 CLASS 1 I/O

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} , $V_{(DDQ)}$, $V_{(DDA)}$ (see Note 1) . . . . . –0.3 to 3 V
Input voltage: V_I (LVTTL) . . . . . –0.5 to 4 V
1.8V HSTL/ SSTL_2 CLASS 1 . . . . . –0.5 to 4 V
DC input voltage (I/O) . . . . . –0.3 to 3 V
Storage temperature . . . . . –65°C to 150°C
Electrostatic discharge . . . . . HBM: 2KV, CDM:750V
Characterized free-air operating temperature range (see Note 2) . . . . . 0°C to 70°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are stated with respect to network ground terminal.
2. To achieve 70°C ambient temperature requires 1 m/s air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Core supply voltage, V_{DD}		2.3	2.5	2.7	V
I/O supply voltage, $V_{(DDQ)}$	SSTL_2 Class 1	2.3	2.5	2.7	V
	1.8 V HSTL Class 1	1.7	1.8	1.9	
Analog supply voltage, $V_{(DDA)}$		2.3	2.5	2.7	V
Core supply current, I_{DD}	f_I = 156.25 MHz		400	540	mA
I/O supply current, $I_{(DDQ)}$	SSTL_2 Class 1, f_I = 156.25 MHz		160	270	mA
	1.8V HSTL Class 1, f_I = 156.25 MHz		125	195	
Analog supply current, $I_{(DDA)}$	f_I = 156.25 MHz		300	350	mA
Total power consumption, (SSTL), P_D	Transceiver mode, f_I = 156.25 MHz		2.2	3.1	W
	Transmit mode, f_I = 156.25 MHz		1.3	1.6	W
	Receive mode, f_I = 156.25 MHz		2.2	2.9	W
Total power consumption, (HSTL), P_D	Transceiver mode, f_I = 156.25 MHz		2.1	2.7	W
	Transmit mode, f_I = 156.25 MHz		1.3	1.42	W
	Receive mode, f_I = 156.25 MHz		1.8	2.2	W
Input reference voltage‡, $V_{(REF)}$	SSTL_2 Class 1	1.15	1.25	1.35	V
	1.8V HSTL Class 1	0.85	0.90	0.95	V
Analog shutdown current, $I_{(SDA)}$	Enable = low		60		µA
Core shutdown current, $I_{(SDD)}$	Enable = low		1		mA
Core shutdown current, $I_{(SDQ)}$	Enable = low		5		µA

‡ The value of $V_{(REF)}$ may be selected to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be $0.4 \times V_{(DDQ)}$ of the transmitting device, and $V_{(REF)}$ is expected to track variations in $V_{(DDQ)}$. Peak-to-peak ac noise on $V_{(REF)}$ may not exceed +2% $V_{(REF)}$(dc).

reference clock timing requirements (RFCP/N) over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_I	Frequency	Minimum data rate	TYP–0.01%	125	TYP+0.01%	MHz
		Maximum data rate	TYP–0.01%	156.25	TYP+0.01%	
	Accuracy		–100		100	ppm
	Duty cycle		40%	50%	60%	
	Jitter	Random and deterministic			40	ps

NOTE: This clock should be crystal referenced to meet the requirements of the above table. Contact TI for specific clocking recommendations.

reference clock electrical characteristics (RFCP/N) over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage		825		1675	mV
V_{ID}	Differential input voltage	at 3.125 Gbps	200			$mV_{p–p}$
		at 2.5 Gbps	175			$mV_{p–p}$
C_I	Input capacitance				3	pF
Z_I	Input differential impedance		80	100	120	Ω

LVTTL electrical characteristics over recommended operating conditions (unless otherwise noted) (see terminal function table for a list of LVTTL signals)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –400 µA, V_{DD} = MIN	2.1		V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, V_{DD} = MIN	0	0.25	0.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High input current	V_{IN} = 2 V, V_{DD} = MAX			40	µA
I_{IL}	Low input current	V_{IN} = 0.4 V, V_{DD} = MAX			–600	µA
C_I	Input capacitance				4	pF

SSTL_2 CLass 1 signals (see terminal function table for a list of SSTL_2 Class 1 signals) (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(dc)}$	High-level output voltage	Without line termination, See Note 3	1.57	$V_{(DDQ)}$ –0.1	$V_{(DDQ)}$ –0.1	V
$V_{OL(dc)}$	Low-level output voltage	Without line termination, See Note 3	0.04		0.1	V
$V_{IH(dc)}$	High-level dc input voltage	DC input, logic high	$V_{(REF)}$+0.18		$V_{(DDQ)}$+0.3	V
$V_{IL(dc)}$	Low-level dc input voltage	DC input, logic low	–0.30		$V_{(REF)}$–0.18	V
$V_{IH(ac)}$	High-level ac input voltage	AC input, logic high	$V_{(REF)}$+0.35			V
$V_{IL(ac)}$	Low-level ac input voltage	AC input, logic low			$V_{(REF)}$–0.35	V
$I_{OH(dc)}$	High output current	$V_{(DDQ)}$ = 2.3 V, V_O = $V_{(DDQ)}$ – 0.62 V	–7.6			mA
$V_{OL(dc)}$	Low output current	$V_{(DDQ)}$ = 2.3 V, V_O = 0.54 V	7.6			mA
C_I	Input capacitance				4	pF

NOTE 3: See Figure 26, for more information on SSTL_2 CLASS 1 specifications and test conditions, refer to EIA/JEDEC, Stub Series Terminated Logic for 2.5 V (SSTL_2), EIA/JESD8–9A, Dec 2000.

1.8V HSTL signals (see terminal function table for a list of 1.8V HSTL signals)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(dc)}$	High-level output voltage		$V_{(DDQ)}$–0.4		$V_{(DDQ)}$	V
$V_{OL(dc)}$	Low-level output voltage				0.40	V
$V_{IH(dc)}$	High-level dc input voltage	DC input, logic high	V_{ref}+0.1		$V_{(DDQ)}$+0.3	V
$V_{IL(dc)}$	Low-level dc input voltage	DC input, logic low	–0.30		$V_{(REF)}$–0.1	V
$V_{IH(ac)}$	High-level ac input voltage	AC input, logic high	$V_{(REF)}$+0.2			V
$V_{IL(ac)}$	Low-level ac input voltage	AC input, logic low			$V_{(REF)}$–0.2	V
$I_{OH(dc)}$	High output current	$V_{(DDQ)}$ = 1.8 V	–8			mA
$I_{OL(dc)}$	Low output current	$V_{(DDQ)}$ = 1.8 V	8			mA
C_I	Input capacitance				4	pF

serial transmitter/receiver characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(p)}$	TX output voltage magnitude away from common mode	Maximum preemphasis enabled, See Figure 17	650	850	1050	mV
$V_{OD(d)}$		Preemphasis disabled, See Figure 17	600			
$V_{OD(pp)}$	TX output differential peak-to-peak voltage swing	Maximum preemphasis enabled, See Figure 17	1300	1700	2100	mVp-p
$V_{OD(pd)}$		Preemphasis disabled, See Figure 17	1200			
$V_{O(CMT)}$	RX output common mode voltage range	See Figure 17	1000		1450	mV
V_{ID}	RX input voltage magnitude away from common mode	See Figure 17	100		1150	mV
$V_{ID(p)}$	RX input differential peak-to-peak voltage swing	See Figure 17	200		2300	mV
$V_{I(CMR)}$	RX input common mode voltage range	See Figure 17	1000		2000	mV
I_{lkg}	RX input leakage current		–10		10	µA
C_i	RX input capacitance				2	pF
t_r, t_f	Differential output signal rise/fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, See Figure 17	80		160	ps
$t_{(J\_TOL)}$	Jitter tolerance, total jitter at serial input	Zero crossing, See Figure 20§			0.55	UI†‡
$t_{(J\_IDR)}$	Serial input deterministic jitter	Zero crossing, See Figure 20			0.37	UI†
$t_{(J\_OT)}$	Serial output total jitter	PRBS at 3.125 GHz, See Figure 18		0.20	0.35	UI†
$t_{(J\_ODR)}$	Serial output deterministic jitter	PRBS at 3.125 GHz			0.17	UI†
$t_{d(R\_Latency)}$	Total delay from RX input to RD output	Serdes mode	46		50	Bits
		Encode/decode mode	86		90	Bits
		10 Gig mode	149		166	Bits
$t_{d(T\_Latency)}$	Total delay from TD input to TX output	See Figure 5	84		124	Bits

† Unit interval = one serial bit time (minimum 320 ps)
‡ Maximum eye closure
§ The receiver tolerates an additional sinusoidal jitter of 0.1 UI with cutoff frequency of 20 MHz, as specified in P802.3ae D2.0 Clause 47, to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

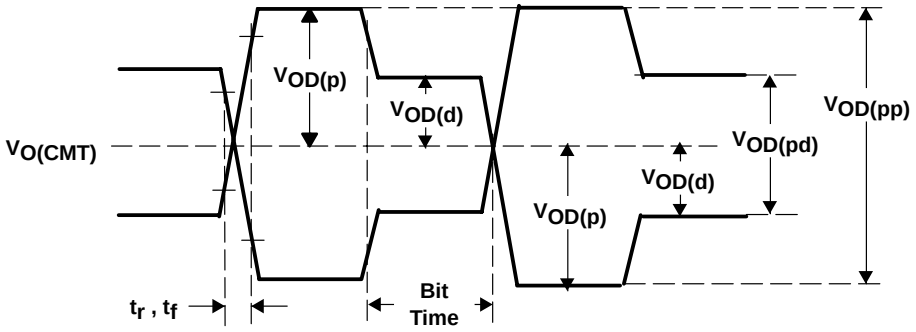


Figure 17. Differential and Common-Mode Output Voltage Definitions

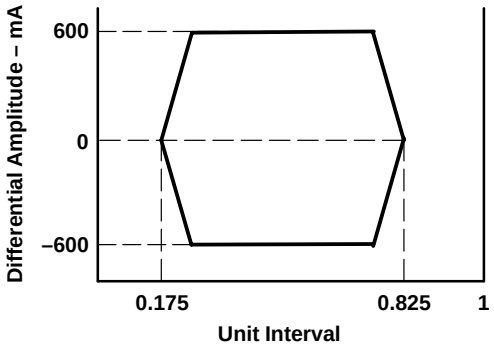


Figure 18. Transmit Template

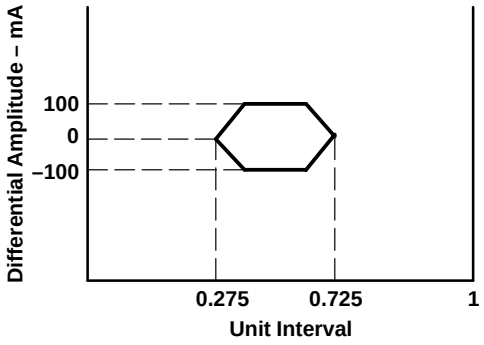
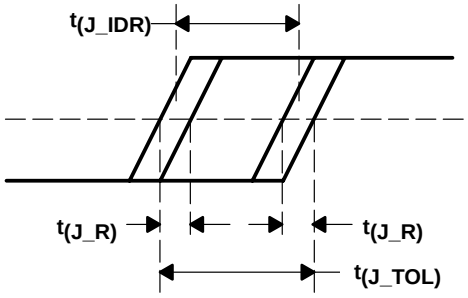


Figure 19. Receive Template



NOTE: $t_{(J\_TOL)} = t_{(J\_R)} + t_{(J\_IDR)}$, where $t_{(J\_TOL)}$ is the receive jitter tolerance, $t_{(J\_IDR)}$ is the received deterministic jitter, and $t_{(J\_R)}$ is the Gaussian random edge jitter distribution at a maximum BER = 10^{-12}.

Figure 20. Input Jitter

SSTL_2 CLASS 1/1.8V HSTL output switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{su}	RDx[0:9] setup prior to RCx transition high or low	Timing relative to $0.5 \times V_{(DDQ)}$, See Figure 21	960			ps
t_h	RDx[0:9] hold after RCx transition high or low		960			

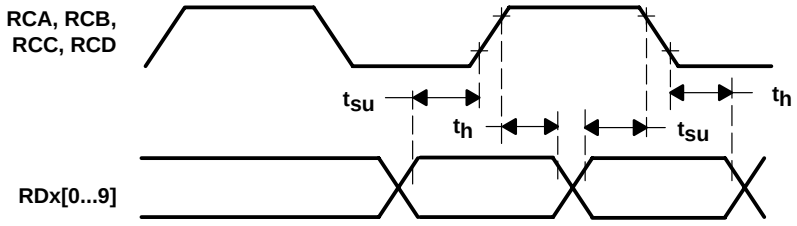


Figure 21. SSTL_2 CLASS1/1.8V HSTL Output Timing Requirements

SSTL_2 CLASS 1/1.8V HSTL input timing requirements over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{su}	TDx[0:9] setup prior to TCx transition high or low	Timing relative to V_{ref}, See Figure 22	480			ps
t_h	TDx[0:9] hold after TCx transition high or low		480			

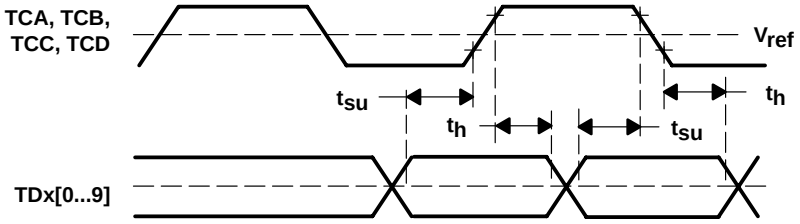


Figure 22. SSTL_2 CLASS1/1.8V HSTL Input Timing Requirements

MDIO timing requirements over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_p	MDC period	See Figure 23	50	400	500	ns
t_{su}	MDIO setup to ↑ MDC		10			ns
t_h	MDIO hold to ↑ MDC		10			ns

† All typical values are at 25°C and with a nominal supply.

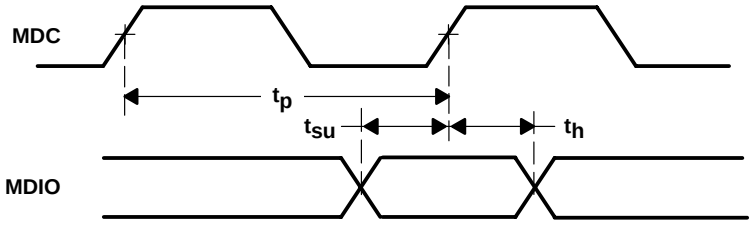


Figure 23. MDIO Read/Write Timing

PACKAGE DISSIPATION RATING

AIR FLOW	0 m/s	1 m/s	2 m/s
θ_{JA}(C/W)	21	17.3	16.7

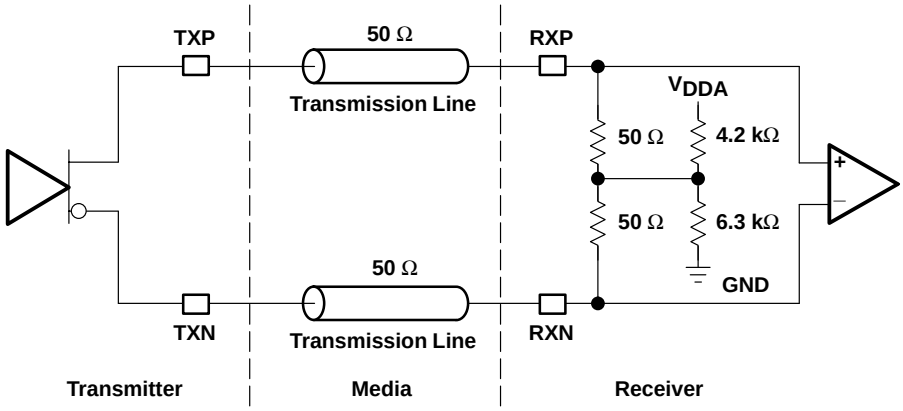


Figure 24. High-Speed I/O Directly-Coupled Mode

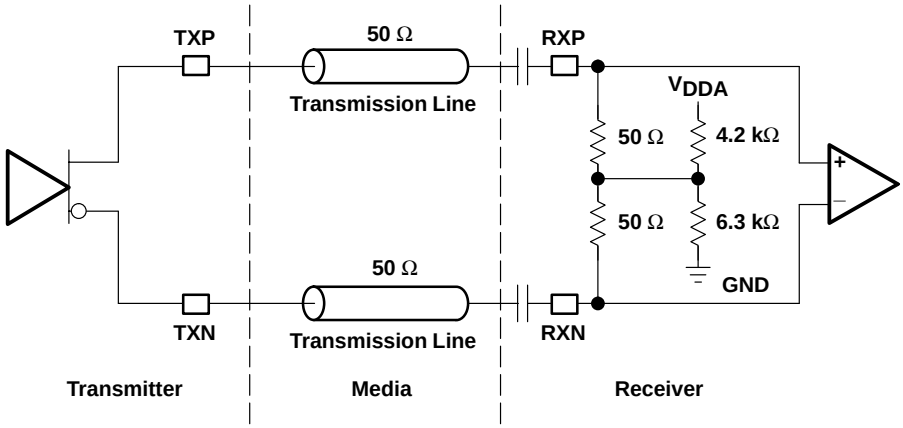
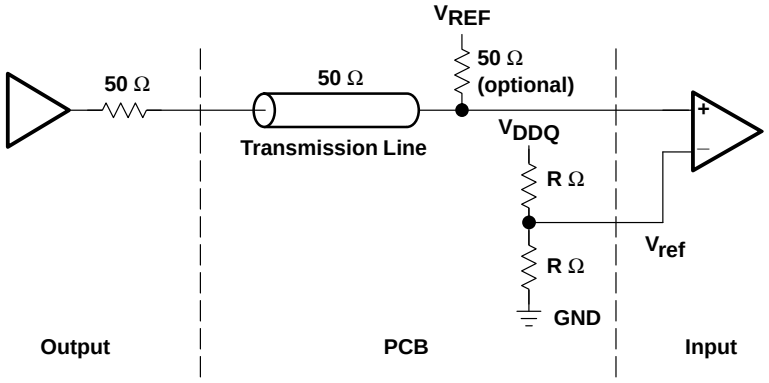
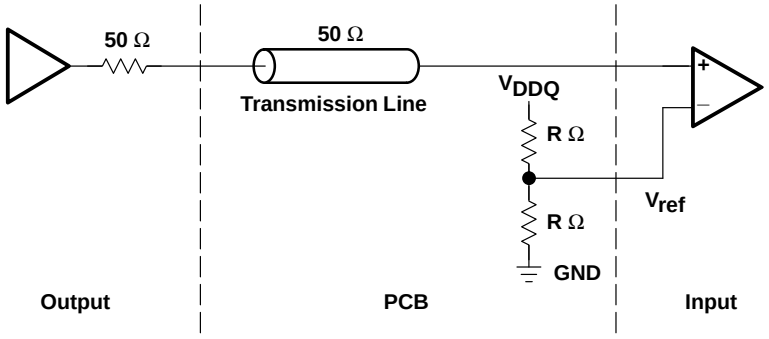


Figure 25. Example High-Speed I/O AC-Coupled Mode



NOTE: The output buffer of the TLK3104SA has on-chip termination of 50 Ω. The output signal is compliant with the JEDEC SSTL_2 Class 1 specification. Line termination on the receive end is optional and not recommended for low-power applications.

Figure 26. SSTL_2 Class 1 I/O

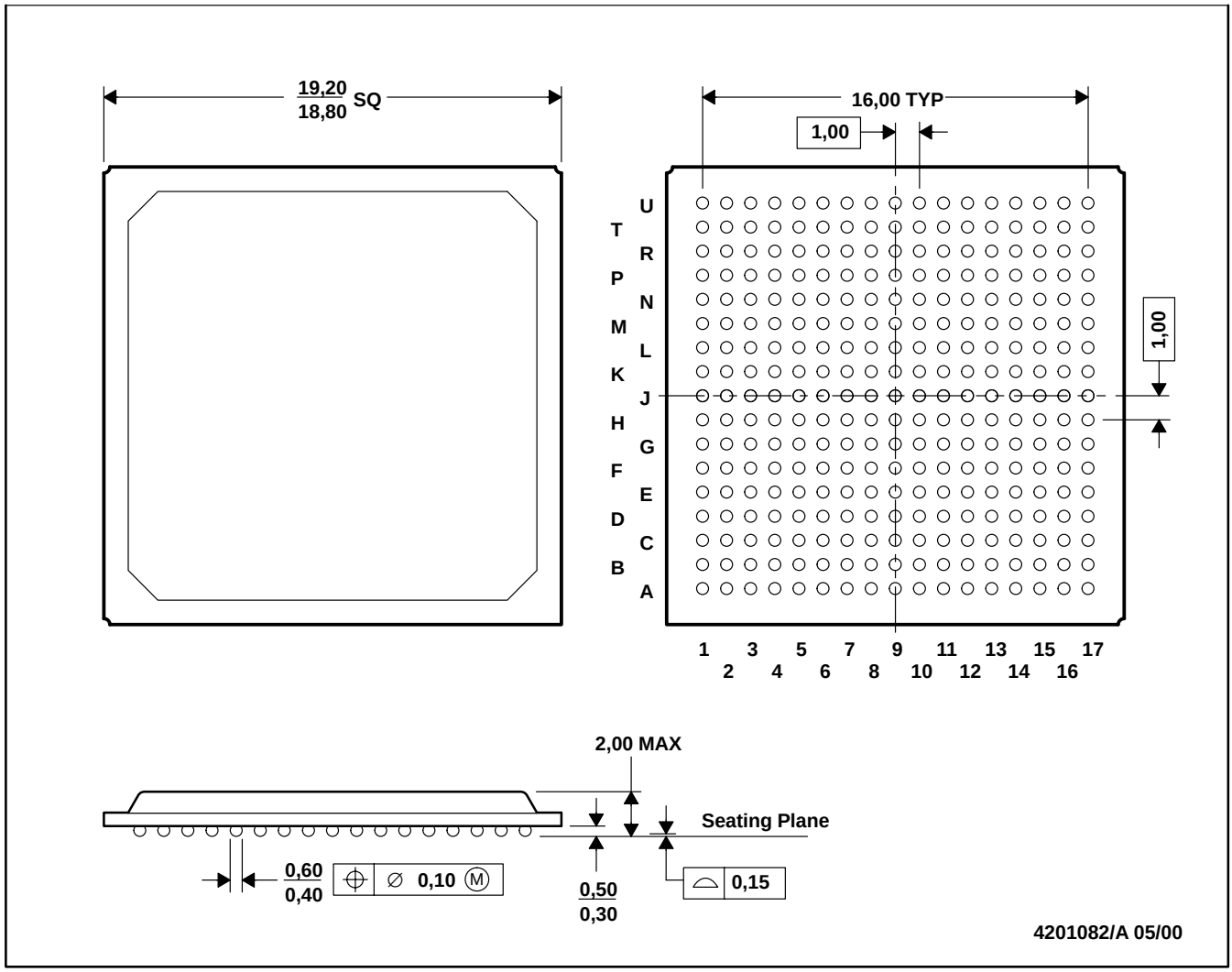


NOTE: The TLK3104SA provides a push-pull effect on the output buffer for externally sourced series terminated loads. In HSTL mode, the signal swing is very small, allowing for minimal power consumption and low electromagnetic emission (EME). To assure sufficient signal levels on the receive side, no termination resistor is used.

Figure 27. 1.8V HSTL I/O

MECHANICAL DATA

GNT (S-PBGA-N289) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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