1.5-Gbps LVDS/LVPECL/CML-TO-CML TRANSLATOR/REPEATER

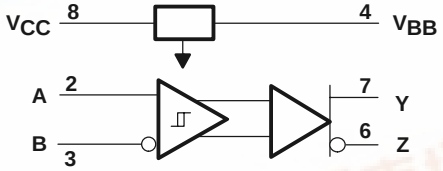
FEATURES

- Provides Level Translation From LVDS or LVPECL to CML, Repeating From CML to CML
- Signaling Rates[1] up to 1.5 Gbps
- CML Compatible Output Directly Drives Devices With 3.3-V, 2.5-V, or 1.8-V Supplies
- Total Jitter < 70 ps
- Low 100 ps (Max) Part-To-Part Skew
- Wide Common-Mode Receiver Capability Allows Direct Coupling of Input Signals
- 25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range
- Propagation Delay Times, 800 ps Maximum
- 3.3-V Supply Operation
- Available in SOIC and MSOP Packages

APPLICATIONS

- Level Translation
- 622-MHz Central Office Clock Distribution
- High-Speed Network Routing
- Wireless Basestations
- Low Jitter Clock Repeater

FUNCTIONAL DIAGRAM



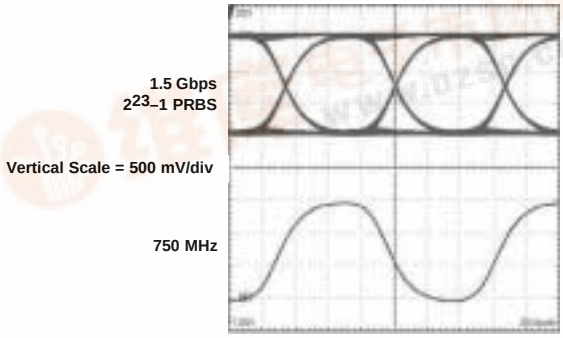
DESCRIPTION

This high-speed translator/repeater is designed for signaling rates up to 1.5 Gbps to support various high-speed network routing applications. The driver output is compatible with current-mode logic (CML) levels, and directly drives 50-Ω or 25-Ω loads connected to 1.8-V, 2.5-V, or 3.3-V nominal supplies. The capability for direct connection to the loads may eliminate the need for coupling capacitors. The receiver input is compatible with LVDS (TIA/EIA–644), LVPECL, and CML signaling levels. The receiver tolerates a wide common-mode voltage range, and may also be directly coupled to the signal source. The internal data path from input to output is fully differential for low noise generation and low pulse-width distortion.

The V_{BB} pin is an internally generated voltage supply to allow operation with a single-ended LVPECL input. For single-ended LVPECL input operation, the unused differential input is connected to V_{BB} as a switching reference voltage. When used, decouple V_{BB} with a 0.01-µF capacitor and limit the current sourcing or sinking to 400 µA. When not used, V_{BB} should be left open.

This device is characterized for operation from –40°C to 85°C.

EYE PATTERN



V_{CC} = 3.3 V, T_A = 25°C, $|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V, V_{TT} = 3.3 V, R_T = 50 Ω

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[1] The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE	STATUS
SN65CML100D	CML100	SOIC	Production
SN65CML100DGK	NWB	MSOP	Production

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNIT
Supply voltage range,(2) V_{CC}			–0.5 V to 4 V
Sink/source, I_{BB}			±0.5 mA
Voltage range, (A, B, Y, Z)			0 V to 4.3 V
Electrostatic discharge	Human Body Model(3)	A, B, Y, Z, and GND	±5 kV
		All pins	±2 kV
	Charged-Device Model(4)	All pins	±1500 V
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range, T_{stg}			–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Terminator supply voltage, V_{TT}	3.3-V nominal supply at terminator	3	3.3	3.6	V
	2.5-V nominal supply at terminator	2.375	2.5	2.625	
	1.8-V nominal supply at terminator	1.7		1.9	V
Magnitude of differential input voltage $\|V_{ID}\|$		0.1		1	V
Input voltage (any combination of common-mode or input signals)		0		4	V
Output current, V_{BB}				400	µA
Operating free-air temperature, T_A		–40		85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DGK	425 mW	3.4 mW/°C	221 mW
D	725 mW	5.8 mW/°C	377 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

DEVICE CHARACTERISTICS

PARAMETER		MIN	NOM	MAX	UNIT
I_{CC}	Supply current, device only		9	12	mA
V_{BB}	Switching reference voltage(1)	1890	1950	2010	mV

(1) V_{BB} parameter varies 1:1 with V_{CC}

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		–100			
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT+} - V_{IT-}$			25		mV
I_I	Input current (A or B inputs)	V_I = 0 V or 2.4 V, Second input at 1.2 V	–20		20	µA
		V_I = 4 V, Second input at 1.2 V			33	
$I_{I(OFF)}$	Power off input current (A or B inputs)	V_{CC} = 1.5 V, V_I = 0 V or 2.4 V, Second input at 1.2 V	–20		20	µA
		V_{CC} = 1.5 V, V_I = 4 V, Second input at 1.2 V			33	
I_{IO}	Input offset current ($\lvert I_{IA} - I_{IB} \rvert$)	$V_{IA} = V_{IB}$, $0 \le V_{IA} \le 4$ V	–6		6	µA
C_i	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
		V_{CC} = 0 V		3		

(1) All typical values are at 25°C and with a 3.3-V supply.

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	Output high voltage(2)	R_T = 50 Ω, V_{TT} = 3 V to 3.6 V or V_{TT} = 2.5 V ±5%, See Figure 2	V_{TT}–60	V_{TT}–10	V_{TT}	mV
V_{OL}	Output low voltage(2)		V_{TT}–1100	V_{TT}–800	V_{TT}–640	mV
$\lvert V_{OD} \rvert$	Differential output voltage magnitude		640	780	1000	mV
V_{OH}	Output high voltage(3)	R_T = 25 Ω, V_{TT} = 3 V to 3.6 V or V_{TT} = 2.5 V ±5%, See Figure 2	V_{TT}–60	V_{TT}–10	V_{TT}	mV
V_{OL}	Output low voltage(3)		V_{TT}–550	V_{TT}–400	V_{TT}–320	mV
$\lvert V_{OD} \rvert$	Differential output voltage magnitude		320	390	500	mV
V_{OH}	Output high voltage(2)	R_T = 50 Ω, V_{TT} = 1.8 V ±5%, See Figure 2	V_{TT}–170	V_{TT}–10	V_{TT}	mV
V_{OL}	Output low voltage(2)		V_{TT}–1100	V_{TT}–800	V_{TT}–640	mV
$\lvert V_{OD} \rvert$	Differential output voltage magnitude		570	780	1000	mV
V_{OH}	Output high voltage(3)	R_T = 25 Ω, V_{TT} = 1.8 V ±5%, See Figure 2	V_{TT}–85	V_{TT}–10	V_{TT}	mV
V_{OL}	Output low voltage(3)		V_{TT}–500	V_{TT}–400	V_{TT}–320	mV
$\lvert V_{OD} \rvert$	Differential output voltage magnitude		285	390	500	mV
C_o	Differential output capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
		V_{CC} = 0 V		3		

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) Outputs are terminated through 50-Ω resistors to V_{TT}; CML level specifications are referenced to V_{TT} and tracks 1:1 with variation of V_{TT}.
(3) Outputs are terminated through 25-Ω resistors to V_{TT}; CML level specifications are referenced to V_{TT} and tracks 1:1 with variation of V_{TT}.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_T = 50 Ω or R_T = 25 Ω, See Figure 4	250		800	ps
t_{PHL}	Propagation delay time, high-to-low-level output		250		800	ps
t_r	Differential output signal rise time (20% – 80%)				300	ps
t_f	Differential output signal fall time (20% – 80%)				300	ps
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)(2)			0	50	ps
$t_{sk(pp)}$	Part-to-part skew(3)	V_{ID} = 0.2 V			100	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)	750 MHz clock input(5)		1	5	ps
$t_{jit(cc)}$	Cycle-to-cycle jitter (peak)(4)	750 MHz clock input(6)		8	27	ps
$t_{jit(pp)}$	Peak-to-peak jitter(4)	1.5 Gbps 2^{23}–1 PRBS input(7)		30	70	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak(4)	1.5 Gbps 2^7–1 PRBS input(8)		25	65	ps

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL}.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Jitter parameters are ensured by design and characterization. Measurements are made with a Tektronix TDS6604 oscilloscope running Tektronix TDSJIT3 software. Agilent E4862B stimulus system jitter 2 ps $t_{jit(per)}$, 16 ps $t_{jit(cc)}$, 25 ps $t_{jit(pp)}$, and 10 ps $t_{jit(det)}$ has been subtracted from the values.
(5) V_{ID} = 200 mV, 50% duty cycle, V_{IC} = 1.2 V, $t_r = t_f \le 25$ ns (20% to 80%), measured over 1000 samples.
(6) V_{ID} = 200 mV, 50% duty cycle, V_{IC} = 1.2 V, $t_r = t_f \le 25$ ns (20% to 80%).
(7) V_{ID} = 200 mV, V_{IC} = 1.2 V, $t_r = t_f \le 0.25$ ns (20% to 80%), measured over 100k samples.
(8) V_{ID} = 200 mV, V_{IC} = 1.2 V, $t_r = t_f \le 0.25$ ns (20% to 80%). Deterministic jitter is sum of pattern dependent jitter and pulse width distortion.

PARAMETER MEASUREMENT INFORMATION

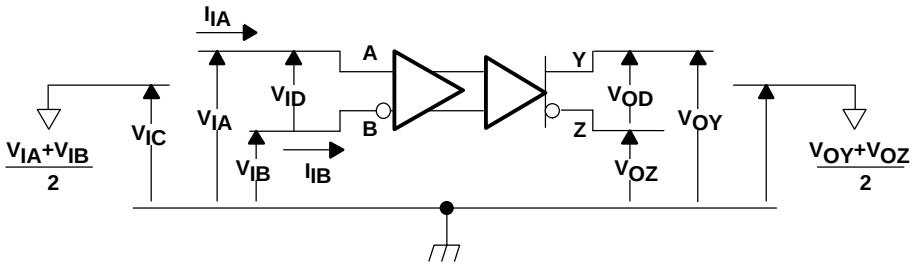


Figure 1. Voltage and Current Definitions

Table 1. Maximum Receiver Input Voltage Threshold

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	–100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4. 0 V	–100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.5 V	H
0.0 V	0.1 V	–100 mV	0.5 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	–1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	–1000 mV	0.5 V	L

H = high level, L = low level

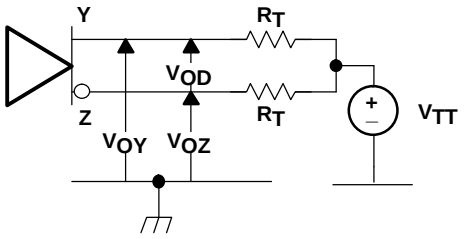


Figure 2. Output Voltage Test Circuit

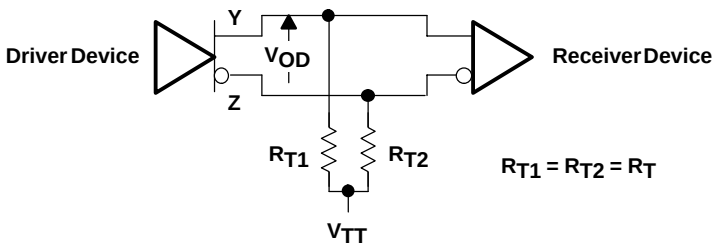
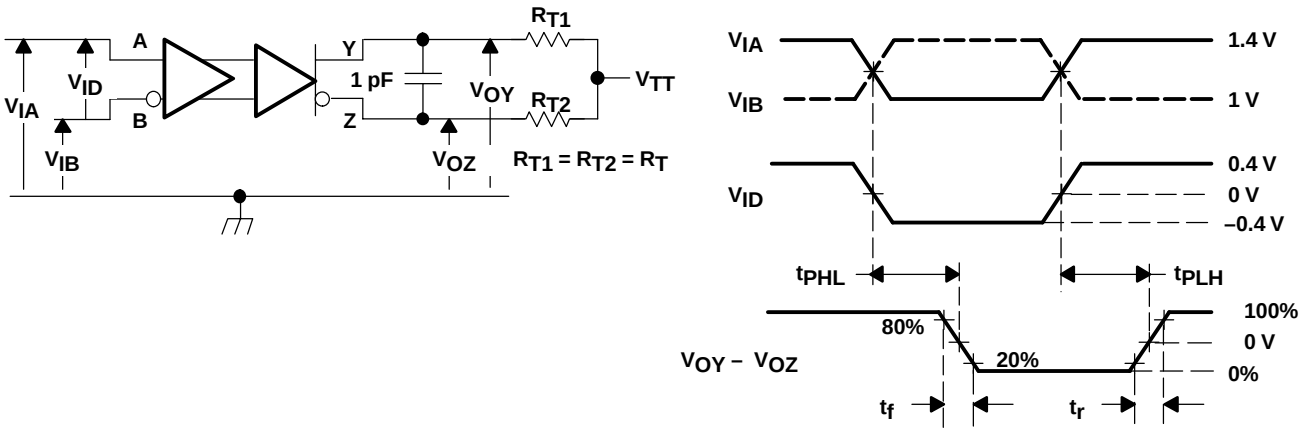


Figure 3. Typical Termination for Output Driver

PARAMETER MEASUREMENT INFORMATION

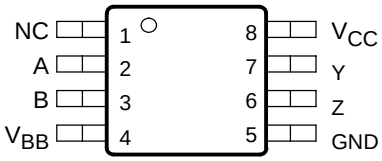


NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 0.25$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. Measurement equipment provides a bandwidth of 5 GHz minimum.

Figure 4. Timing Test Circuit and Waveforms

PIN ASSIGNMENTS

D AND DGK PACKAGE
(TOP VIEW)



PIN DESCRIPTIONS

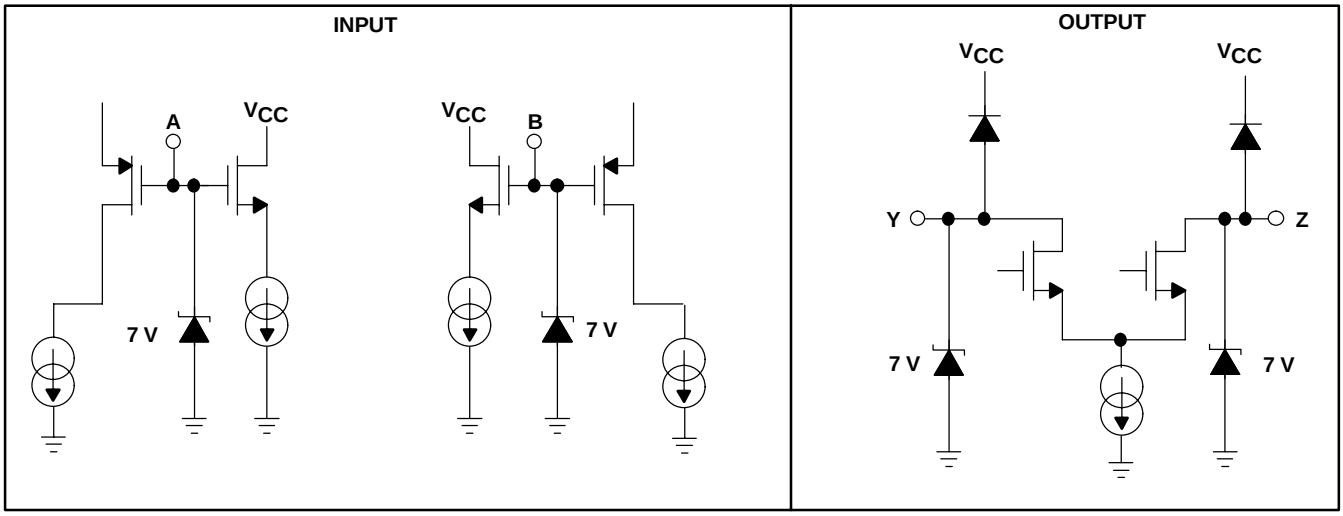
PIN	FUNCTION
A, B	Differential inputs
Y, Z	Differential outputs
V_{BB}	Reference voltage output
V_{CC}	Power supply
GND	Ground
NC	No connect

FUNCTION TABLE

DIFFERENTIAL INPUT	OUTPUTS	
$V_{ID} = V_A - V_B$	Y	Z
$V_{ID} \geq 100$ mV	H	L
–100 mV < V_{ID} < 100 mV	?	?
$V_{ID} \leq$ –100 mV	L	H
Open	?	?

H = high level, L = low level, ? = intermediate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

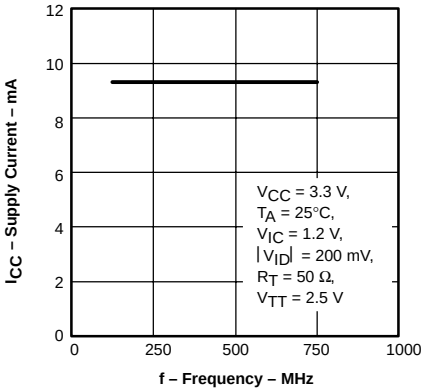


Figure 5

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

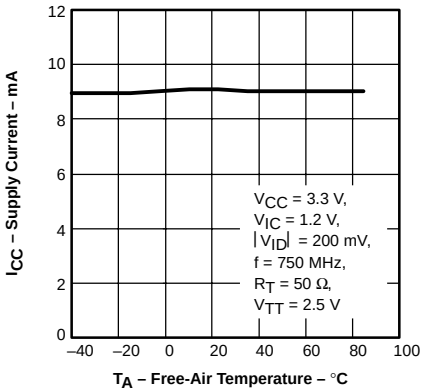


Figure 6

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

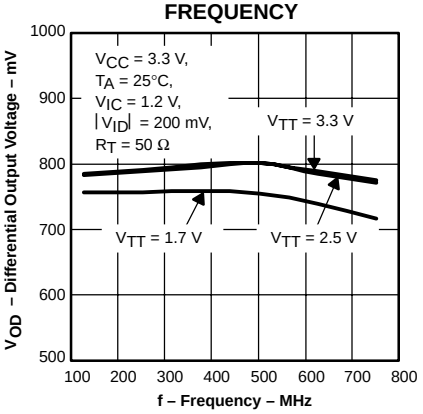


Figure 7

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

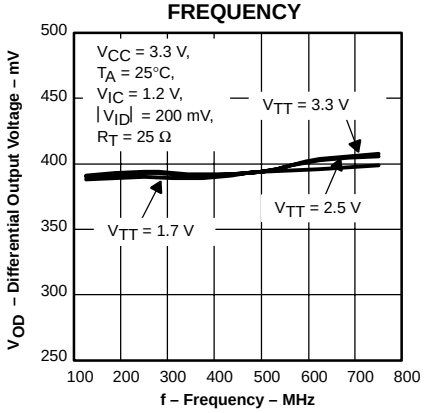


Figure 8

PROPAGATION DELAY TIME vs COMMON-MODE INPUT VOLTAGE

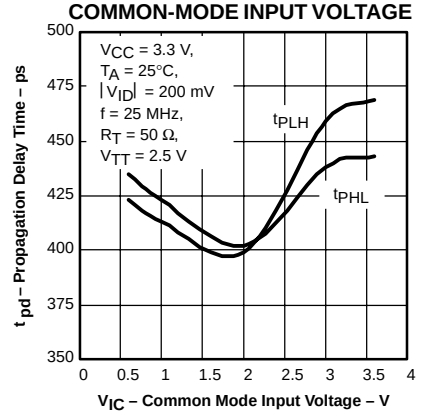


Figure 9

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

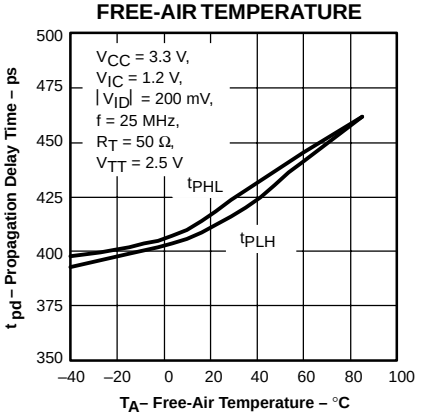


Figure 10

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

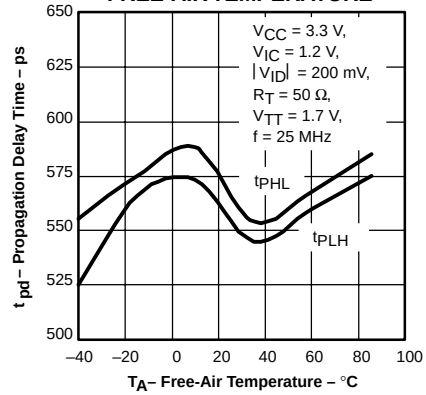


Figure 11

PEAK-TO-PEAK JITTER vs FREQUENCY

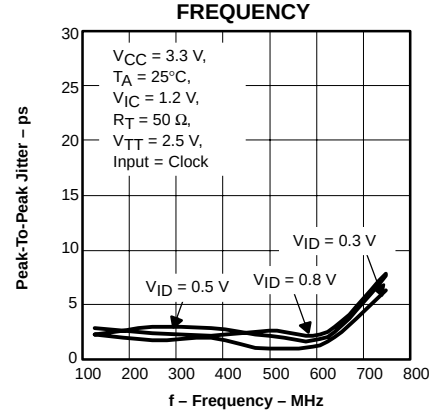


Figure 12

PEAK-TO-PEAK JITTER vs DATA RATE

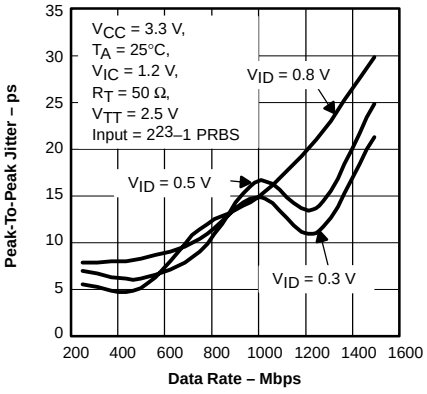


Figure 13

TYPICAL CHARACTERISTICS

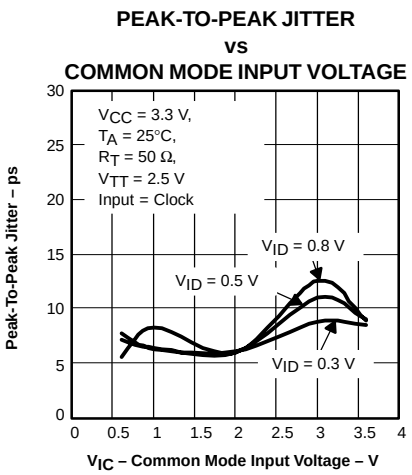


Figure 14

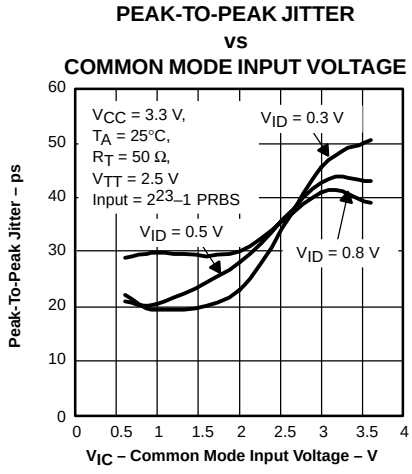


Figure 15

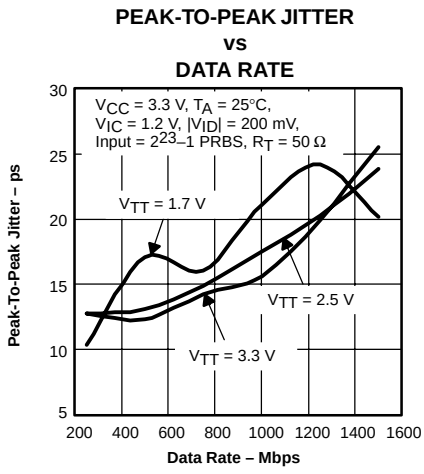


Figure 16

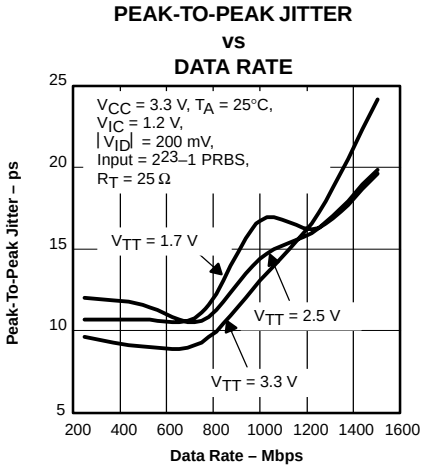
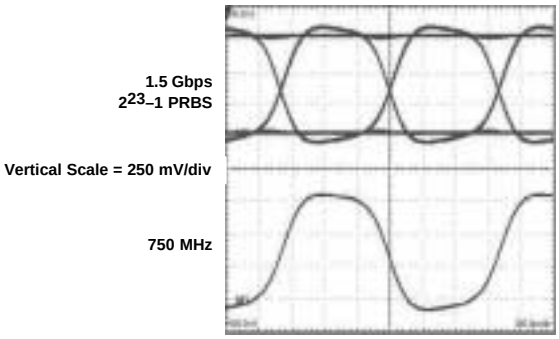
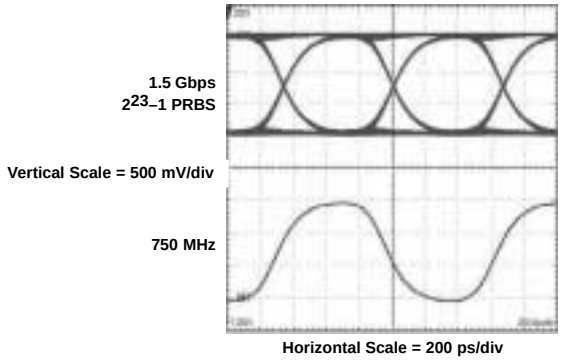


Figure 17



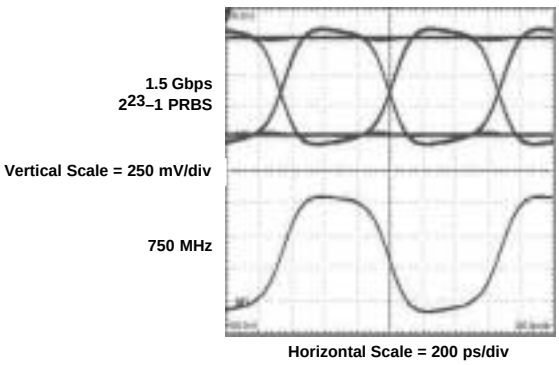
V_{CC} = 3.3 V, T_A = 25°C, $|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V, V_{TT} = 3.3 V, R_T = 25 Ω

Figure 18



V_{CC} = 3.3 V, T_A = 25°C, $|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V, V_{TT} = 2.5 V, R_T = 50 Ω

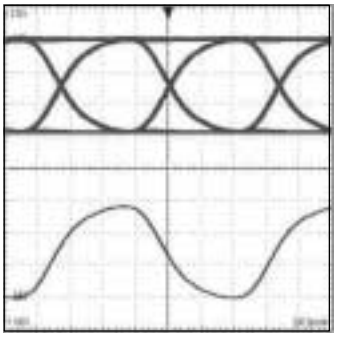
Figure 19



V_{CC} = 3.3 V, T_A = 25°C, $|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V, V_{TT} = 2.5 V, R_T = 25 Ω

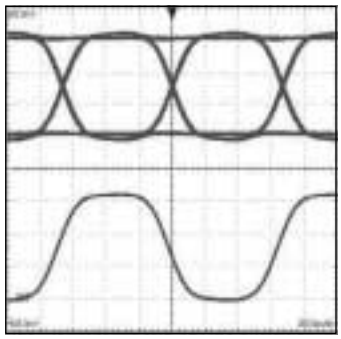
Figure 20

TYPICAL CHARACTERISTICS



V_{CC} = 3.3 V, T_A = 25°C, V_{IC} = 1.2 V, $|V_{ID}|$ = 200 mV, V_{TT} = 1.7 V, R_T = 50 Ω

Figure 21



V_{CC} = 3.3 V, T_A = 25°C, V_{IC} = 1.2 V, $|V_{ID}|$ = 200 mV, V_{TT} = 1.7 V, R_T = 25 Ω

Figure 22

TYPICAL CHARACTERISTICS

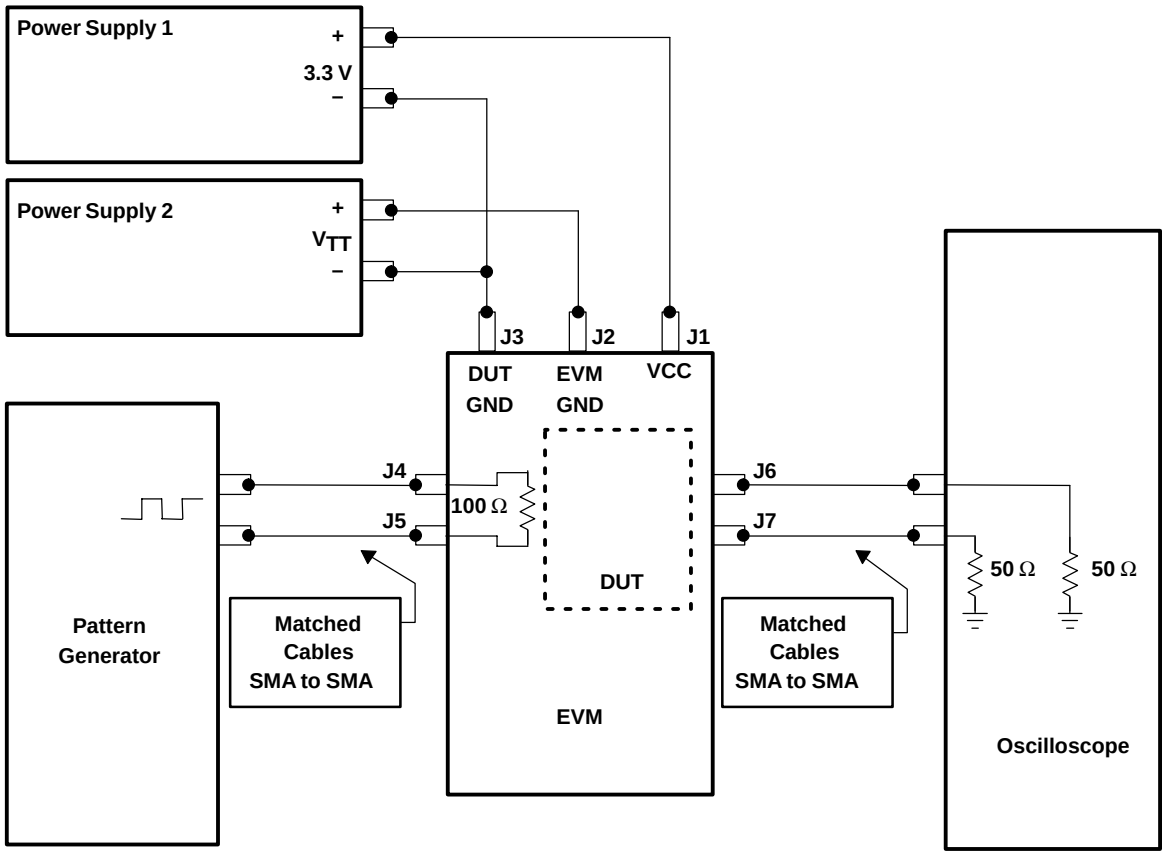


Figure 23. Jitter Setup Connections for SN65CML100

APPLICATION INFORMATION

For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. When V_{BB} is used, decouple V_{BB} via a 0.01-µF capacitor and limit the current sourcing or sinking to 0.4 mA. When not used, V_{BB} should be left open.

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, ETC.)

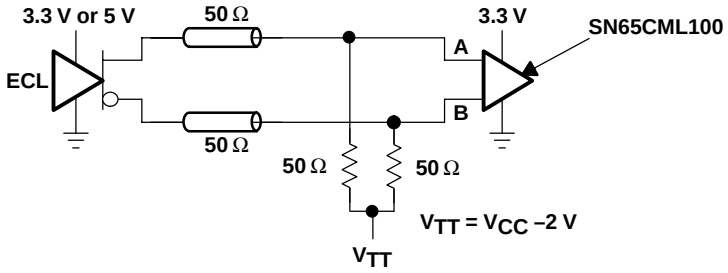


Figure 24. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

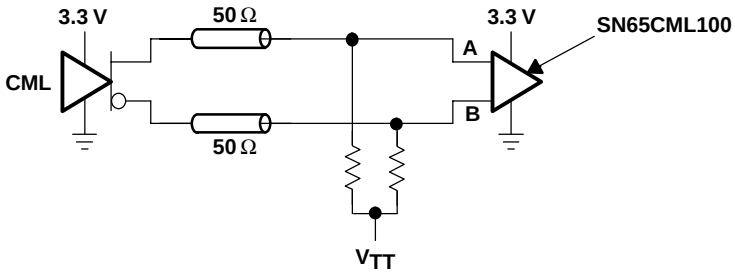


Figure 25. Current–Mode Logic (CML)

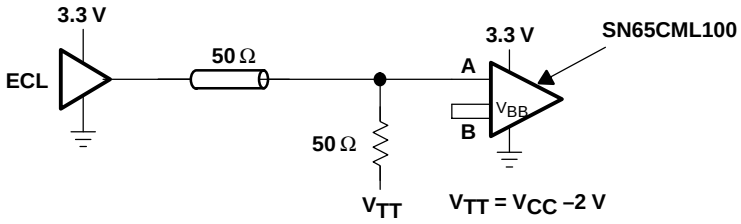


Figure 26. Single-Ended (LVPECL)

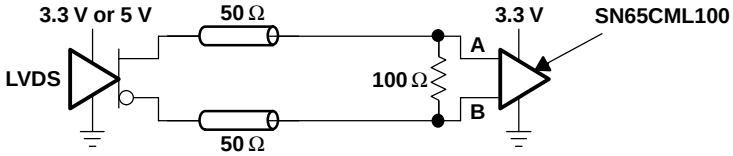
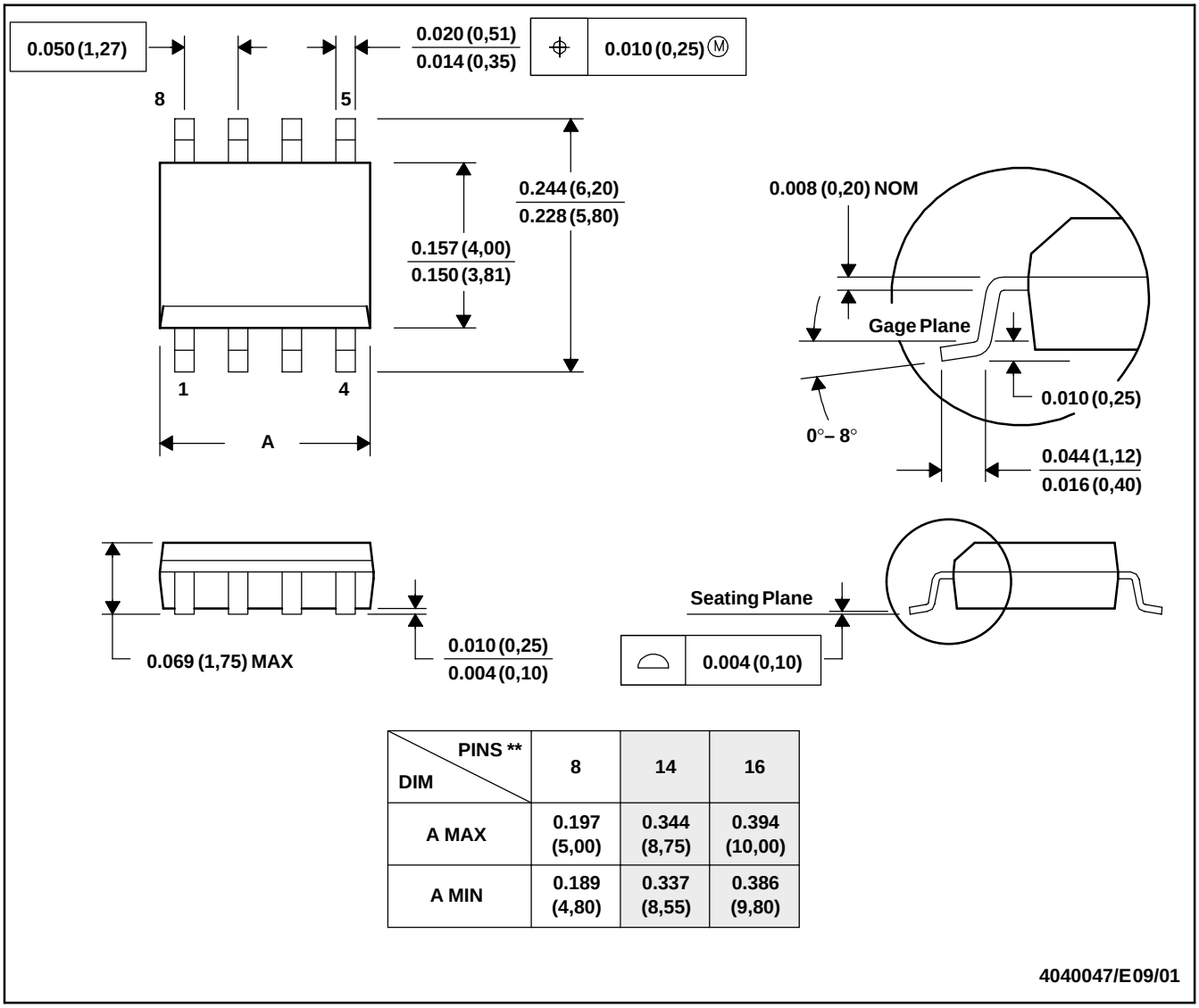


Figure 27. Low-Voltage Differential Signaling (LVDS)

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



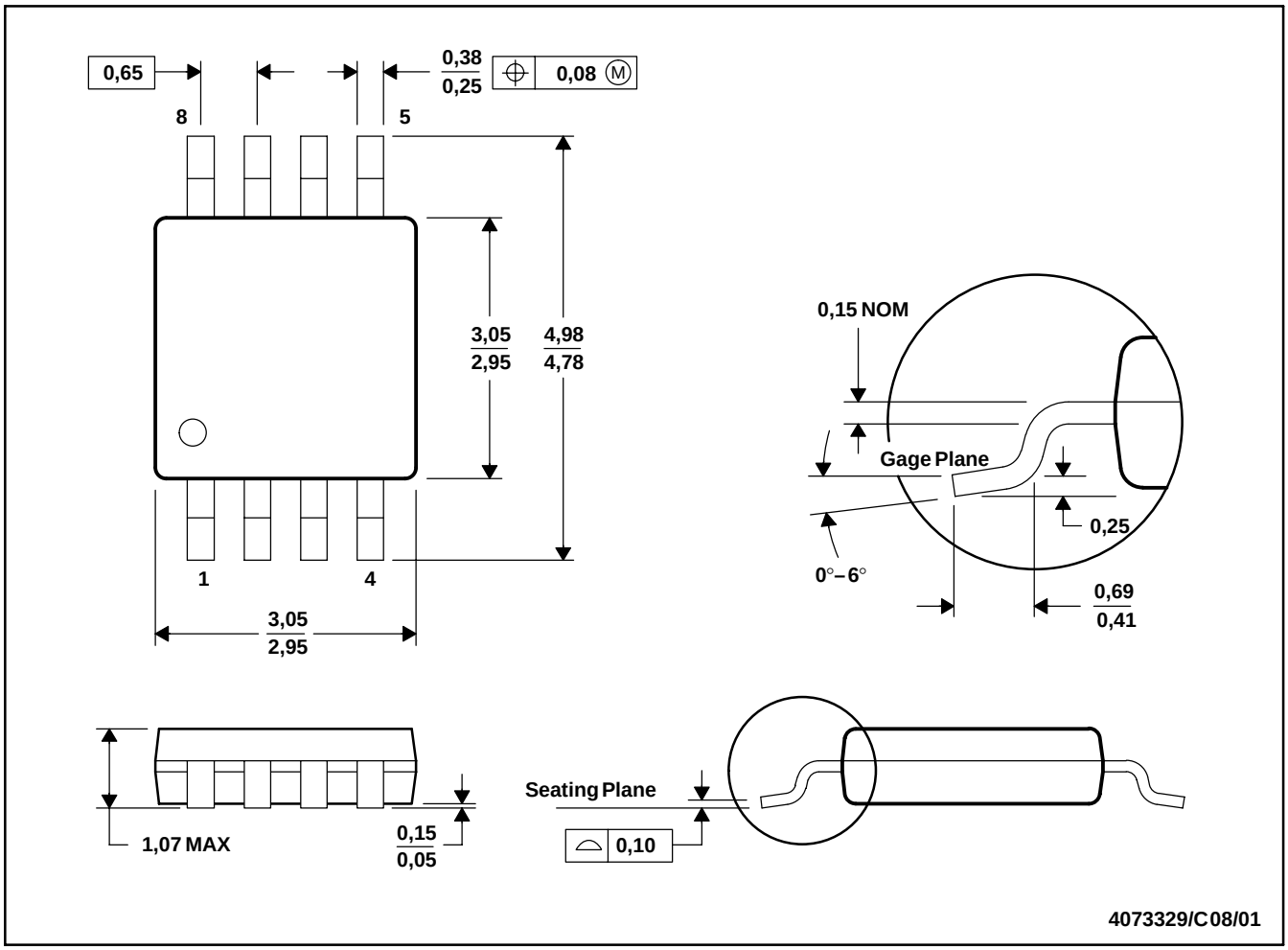
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES:A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

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