TEXAS INSTRUMENTS
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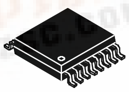
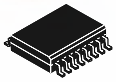




SN65LVDS122
SN65LVDT122

1.5-Gbps 2 x 2 LVDS CROSSPOINT SWITCH

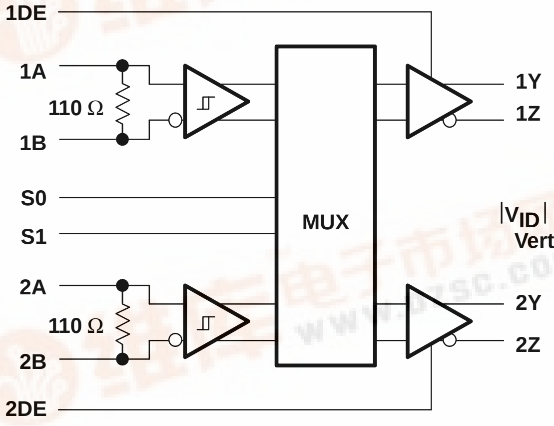
FEATURES

- Designed for Signaling Rates[1] Up To 1.5 Gbps
- Total Jitter < 65 ps
- Pin-Compatible With SN65LVDS22 and SN65LVDM22
- 25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range
- Inputs Electrically Compatible With CML, LVPECL and LVDS Signal Levels
- Propagation Delay Times, 900 ps Maximum
- LVDT Integrates 110-Ω Terminating Resistor
- Offered in SOIC and TSSOP

APPLICATIONS

- 10-G (OC–192) Optical Modules
- 622 MHz Central Office Clock Distribution
- Wireless Basestations
- Low Jitter Clock Repeater/Multiplexer
- Protection Switching for Serial Backplanes

FUNCTIONAL DIAGRAM



Integrated Termination On 65LVDT

DESCRIPTION

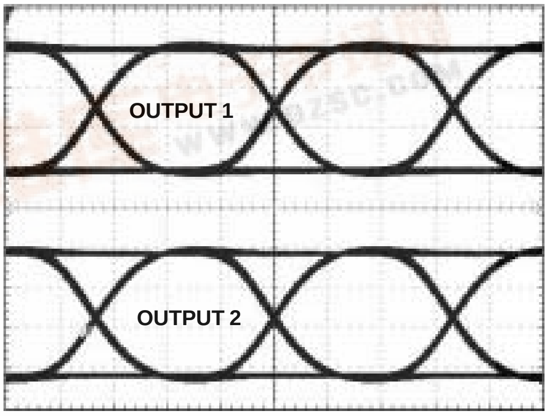
The SN65LVDS122 and SN65LVDT122 are crosspoint switches that use low voltage differential signaling (LVDS) to achieve signaling rates as high as 1.5 Gbps. They are pin-compatible speed upgrades to the SN65LVDS22 and SN65LVDM22. The internal signal paths maintain differential signaling for high speeds and low signal skews. These devices have a 0 V to 4 V common-mode input range that accepts LVDS, LVPECL, CML inputs. Two logic pins (S0 and S1) set the internal configuration between the differential inputs and outputs. This allows the flexibility to perform the following configurations: 2 x 2 crosspoint switch, 2:1 mux, 1:2 splitter or dual repeater/translator within a single device. Additionally, SN65LVDT122 incorporates a 110-Ω termination resistor for those applications where board space is a premium. Although these devices are designed for 1.5 Gbps, some applications at a 2-Gbps data rate can be supported depending on loading and signal quality.

The intended application of this device is ideal for loopback switching for diagnostic routines, fanout buffering of clock/data distribution provide protection in fault-tolerant systems, clock muxing in optical modules, and for overall signal boosting over extended distances.

The SN65LVDS122 and SN65LVDT122 are characterized for operation from –40°C to 85°C.

EYE PATTERNS OF OUTPUTS OPERATING SIMULTANEOUSLY

1.5 Gbps
$2^{23} - 1$ PRBS
$V_{CC} = 3.3$ V
$|V_{ID}| = 200$ mV, $V_{IC} = 1.2$ V
Vertical Scale=200 mV/div



Horizontal Scale= 200 ps/div

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[1] The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PACKAGE	TERMINATION RESISTOR	PART NUMBER(1)	SYMBOLIZATION
SOIC	No	SN65LVDS122D	LVDS122
SOIC	Yes	SN65LVDT122D	LVDT122
TSSOP	No	SN65LVDS122PW	LVDS122
TSSOP	Yes	SN65LVDT122PW	LVDT122

(1) Add the suffix R for taped and reeled carrier

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			SN65LVDS122 SN65LVDT122
Supply voltage range,(2) V_{CC}			–0.5 V to 4 V
Voltage range:	(A, B)		–0.7 V to 4.3 V
	$\lvert V_A – V_B \rvert$ (LVDT only)		1 V
	(DE, S0, S1)		–0.5 V to 4 V
	(Y, Z)		–0.5 V to 4 V
ESD	Human Body Model(3)	A, B, Y, Z, and GND	±4 kV
		All pins	±2 kV
	Charged-Device Model(4)	All pins	±1500 V
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range, T_{stg}			–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	S0, S1, 1DE, 2DE	2		5	V
Low-level input voltage, V_{IL}	S0, S1, 1DE, 2DE	0		0.8	V
Magnitude of differential input voltage $\lvert V_{ID} \rvert$	LVDS	0.1		1	V
	LVDT	0.1		0.8	
Input voltage (any combination of common-mode or input signals)		0		4	V
Operating free-air temperature, T_A		–40		85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
PW	774 mW	6.2 mW/°C	402 mW
D	950 mW	7.6 mW/°C	494 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		See Figure 1 and Table 1	–100[2]			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis ($V_{IT+} - V_{IT-}$)				25		mV
I_{IH}	High-level input current	DE	$V_{IH} = 2$	–10		0	µA
		S0, S1		0		20	
I_{IL}	Low-level input current	DE	$V_{IL} = 0.8$ V	–10		0	µA
		S0, S1				20	
I_{CC}	Supply current		$R_L = 100\ \Omega$		80	100	mA
			Disabled		35	45	
I_I	Input current (A or B inputs ’LVDS)		$V_I = 0$ V or 2.4 V, Other input at 1.2 V	–20		20	µA
			$V_I = 4$ V, Other input at 1.2 V	0		33	
	Input current (A or B inputs ’LVDT)		$V_I = 0$ V or 2.4 V, Other input open	–40		40	µA
			$V_I = 4$ V, Other input open	0		66	
$I_{I(OFF)}$	Input current (A or B inputs ’LVDS)		$V_{CC} = 1.5$ V, $V_I = 0$ V or 2.4 V, Other input at 1.2 V	–20		20	µA
			$V_{CC} = 1.5$ V, $V_I = 2.4$ V or 4 V, Other input at 1.2 V	0		33	
	Input current (A or B inputs ’LVDT)		$V_{CC} = 1.5$ V, $V_I = 0$ V or 2.4 V, Other input open	–40		40	µA
			$V_{CC} = 1.5$ V, $V_I = 2.4$ V or 4 V, Other input open	0		66	
I_{IO}	Input offset current ($\lvert I_{IA} - I_{IB} \rvert$)	’LVDS	$V_{IA} = V_{IB}$, $0 \le V_{IA} \le 4$ V	–6		6	µA
R_T	Termination resistance (’LVDT)		V_{ID}= 300 mV and 500 mV, V_{IC}= 0 V to 2.4 V	90	110	132	Ω
	Termination resistance (’LVDT with power-off)		V_{ID}= 300 mV and 500 mV, $V_{CC} = 1.5$ V, V_{IC}= 0 V to 2.4 V	90	110	132	
C_I	Differential input capacitance (’LVDT with power-off)		$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V		3		pF
			Powered down		3		

[1] All typical values are at 25°C and with a 3.3-V supply.
[2] The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$\lvert V_{OD} \rvert$	Differential output voltage magnitude	See Figure 2	247	310	454	mV
$\Delta\lvert V_{OD} \rvert$	Change in differential output voltage magnitude between logic states	$V_{ID} = \pm 100$ mV, See Figure 2	–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{OS}	Short-circuit output current	$V_{O(Y)}$ or $V_{O(Z)} = 0$ V	–24		24	mA
$I_{OS(D)}$	Differential short-circuit output current	$V_{OD} = 0$ V	–12		12	mA
I_{OZ}	High-impedance output current	$V_{OD} = 600$ mV	–1		1	µA
		$V_O = 0$ V or V_{CC}	–1		1	
C_o	Differential output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V		3		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

TIMING SPECIFICATIONS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{SET}	Input to select setup time		0			ns
t_{HOLD}	Input to select hold time		0.5			ns
t_{SWITCH}	Select to switch output		1	2	2.6	ns

SWITCHING CHARACTERISTICS

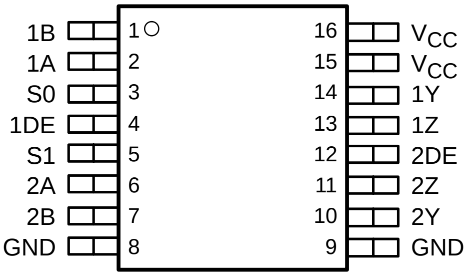
over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4	400	650	900	ps
t_{PHL}	Propagation delay time, high-to-low-level output		400	650	900	ps
t_r	Differential output signal rise time (20% – 80%)				280	ps
t_f	Differential output signal fall time (20% – 80%)				280	ps
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)(2)			10	50	ps
$t_{sk(pp)}$	Part-to-part skew(3)	V_{ID} = 0.2 V			100	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)	750 MHz clock input(5)		1	2.2	ps
$t_{jit(cc)}$	Cycle–to–cycle jitter (peak)(4)	750 MHz clock input(6)		10	17	ps
$t_{jit(pp)}$	Peak–to–peak jitter(4)	1.5 Gbps 2^{23}–1 PRBS input(7)		33	65	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak(4)	1.5 Gbps 2^{7}–1 PRBS input(8)		17	50	ps
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 5		6	8	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 5		6	8	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		4	6	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 5		4	6	ns
$t_{sk(o)}$	Output Skew(9)			15	40	ps

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(5) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 750 MHz, t_r = t_f = 50 ps (20% to 80%), measured over 1000 samples.
(6) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 750 MHz, t_r = t_f = 50 ps (20% to 80%).
(7) Input voltage = V_{ID} = 200 mV, 2^{23}–1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%), measured over 200 k samples.
(8) Input voltage = V_{ID} = 200 mV, 2^{7}–1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%).
(9) Output skew is the magnitude of the time delay difference between the outputs of a single device with all inputs tied together.

PIN ASSIGNMENTS

D OR PW PACKAGE
(TOP VIEW)



CROSSPOINT LOGIC TABLE

S1	S0	1Y/1Z	2Y/2Z	FUNCTION
0	0	1A/1B	1A/1B	splitter
0	1	2A/2B	2A/2B	splitter
1	0	1A/1B	2A/2B	router
1	1	2A/2B	1A/1B	router

PARAMETER MEASUREMENT INFORMATION

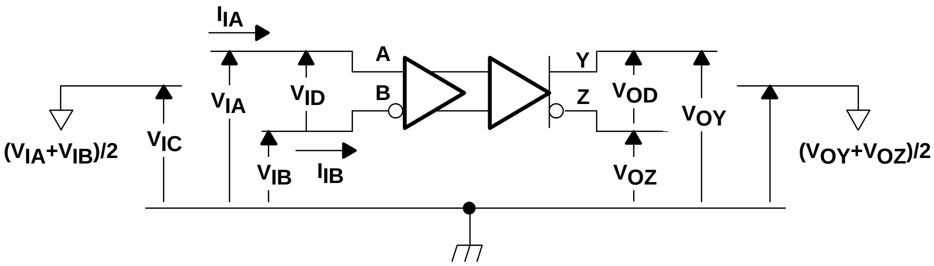


Figure 1. Voltage and Current Definitions

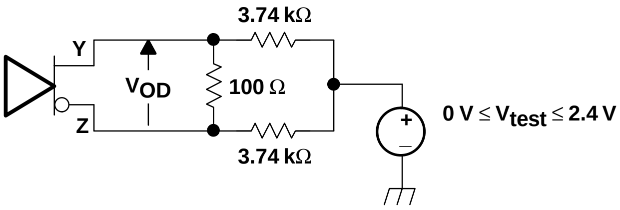
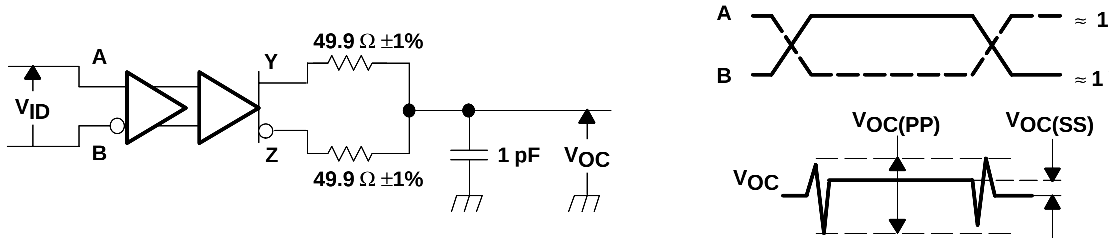
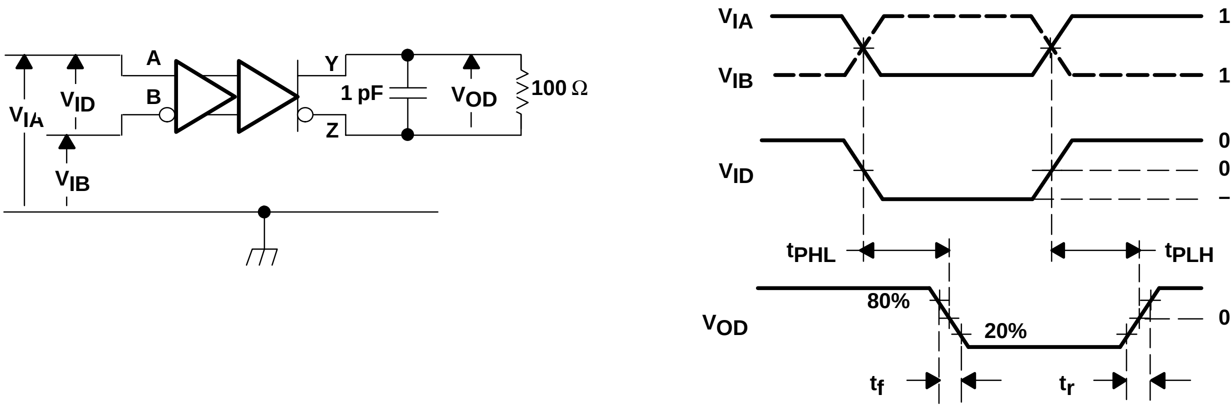


Figure 2. Differential Output Voltage (V_{OD}) Test Circuit



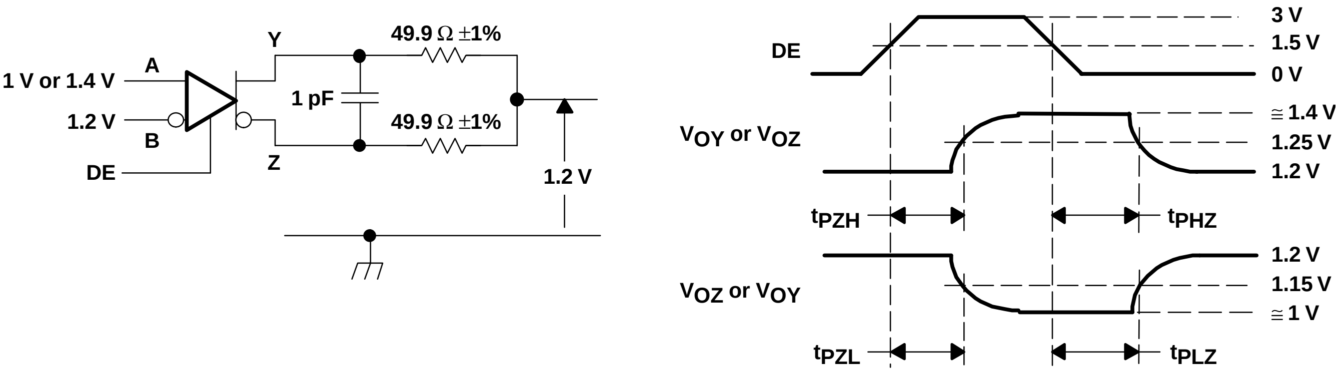
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 0.25$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns; $R_L = 100\ \Omega$; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 0.25$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Timing Test Circuit and Waveforms



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

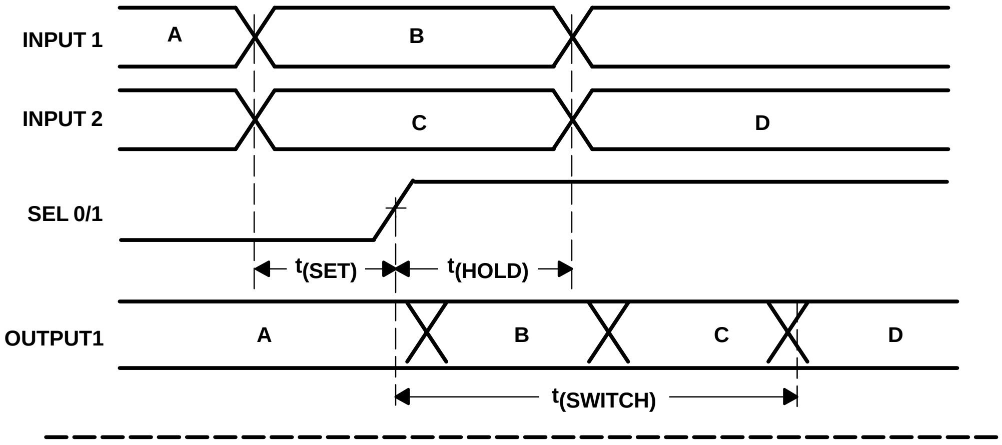


Figure 6. Example Switch, Setup, and Hold Times

$t_{(SET)}$ and $t_{(HOLD)}$ times specify that data must be in a stable state before and after mux control switches.

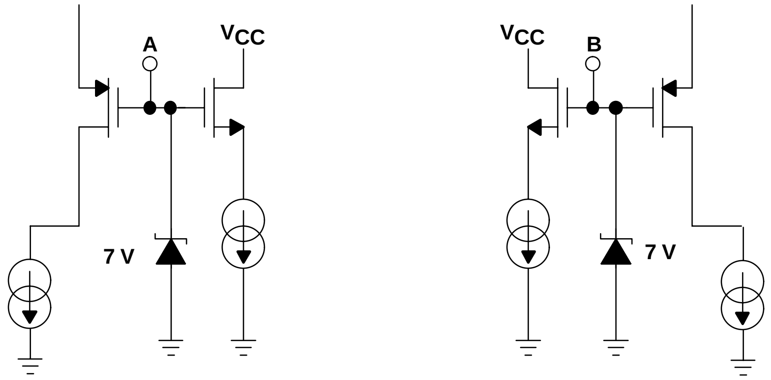
Table 1. Receiver Input Voltage Threshold Test

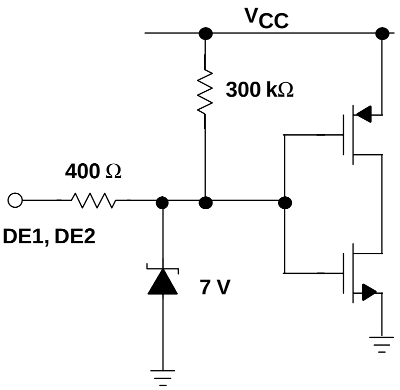
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	–100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4. 0 V	–100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	–100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	–1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	–1000 mV	0.5 V	L

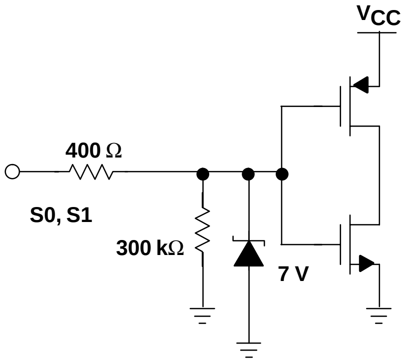
H = high level,   L = low level

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

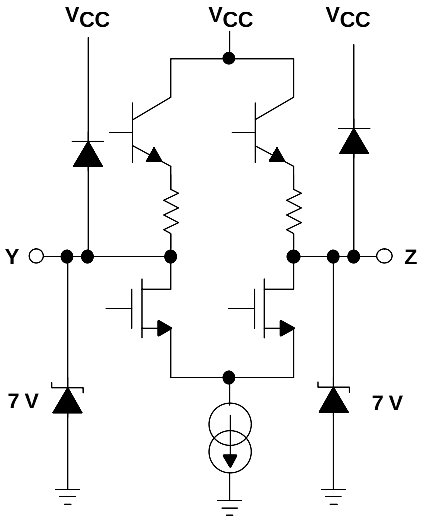
INPUT LVDS122







OUTPUT LVDS122



TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs FREQUENCY

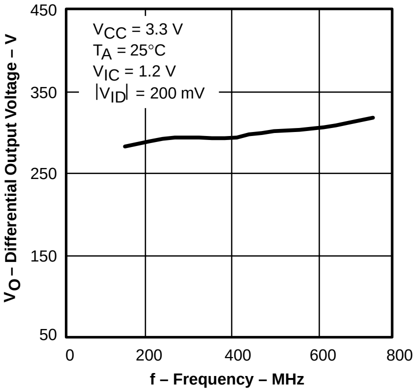


Figure 7

DIFFERENTIAL PROPAGATION DELAY vs COMMON-MODE INPUT VOLTAGE

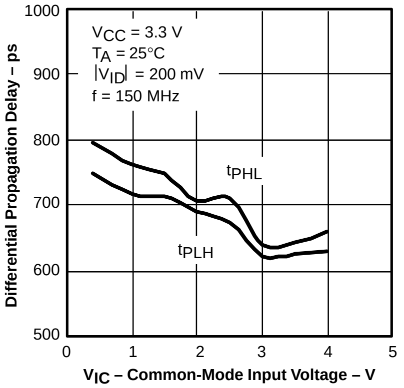


Figure 8

DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE

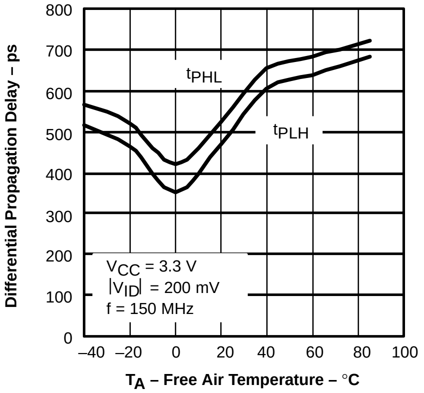


Figure 9

PEAK-TO-PEAK JITTER vs FREQUENCY

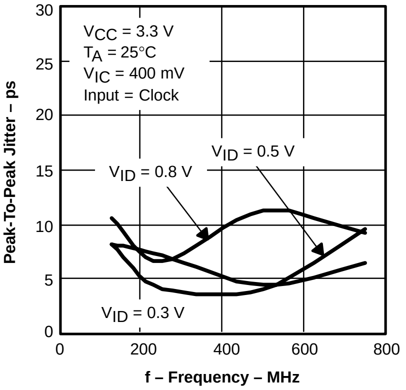


Figure 10

PEAK-TO-PEAK JITTER vs DATA RATE

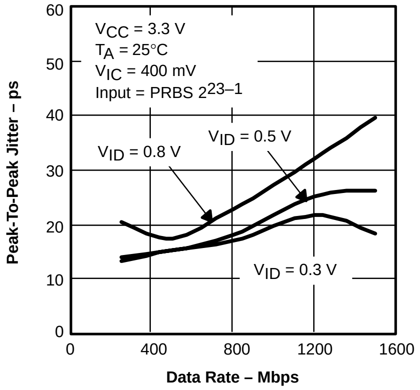


Figure 11

PEAK-TO-PEAK JITTER vs FREQUENCY

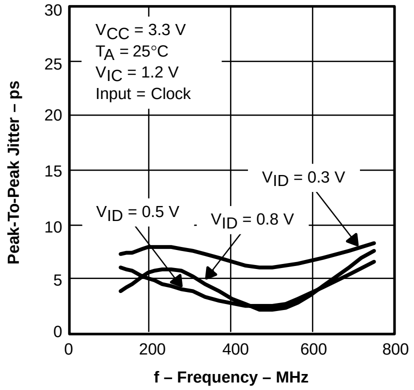


Figure 12

PEAK-TO-PEAK JITTER vs DATA RATE

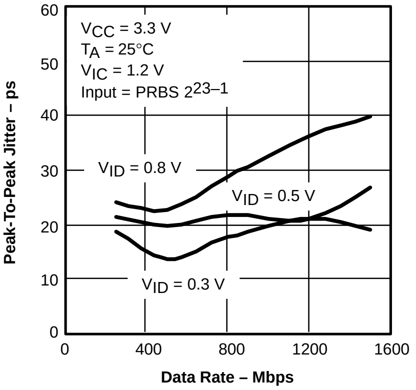


Figure 13

PEAK-TO-PEAK JITTER vs FREQUENCY

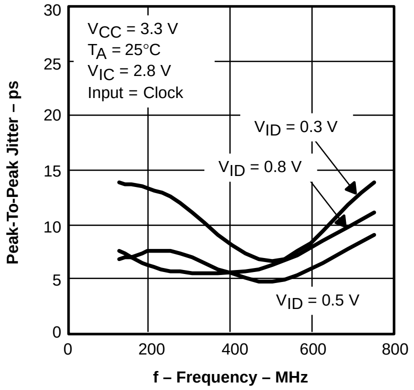


Figure 14

PEAK-TO-PEAK JITTER vs DATA RATE

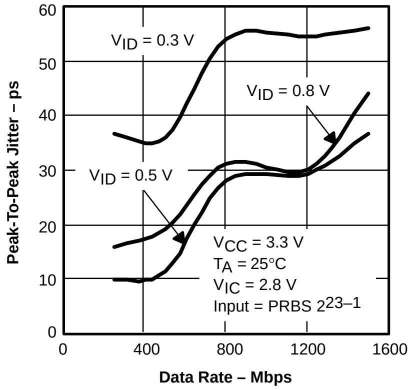


Figure 15

PEAK-TO-PEAK JITTER
vs
TEMPERATURE

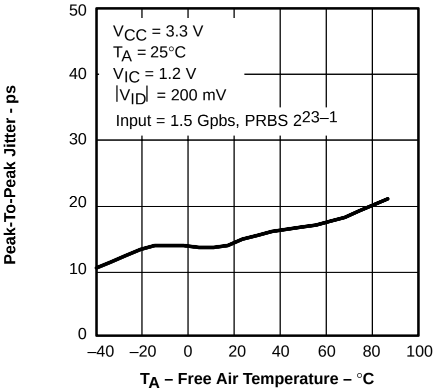
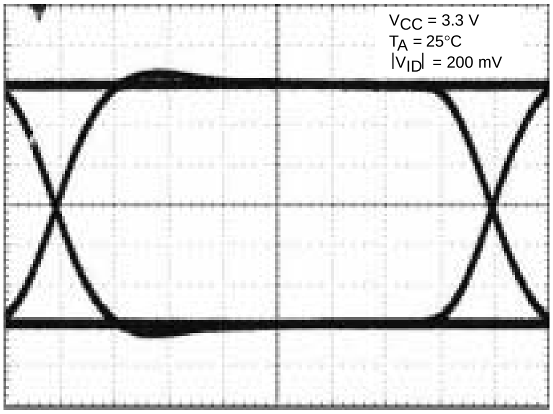


Figure 16

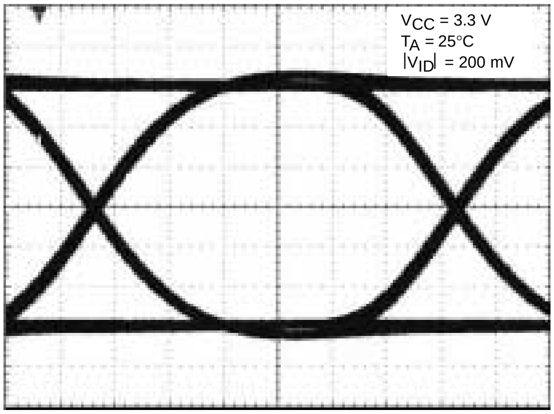
LVDS122
622 Mbps, 2^{23} – 1 PRBS



Horizontal Scale= 200 ps/div
LVPECL-to-LVDS

Figure 17

LVDS122
1.5 Gbps, 2^{23} – 1 PRBS

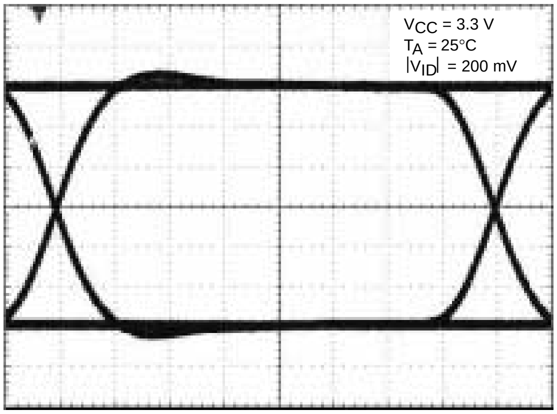


Horizontal Scale= 100 ps/div
LVPECL-to-LVDS

Figure 18

LVDS122

622 Mbps, 2^{23} – 1 PRBS

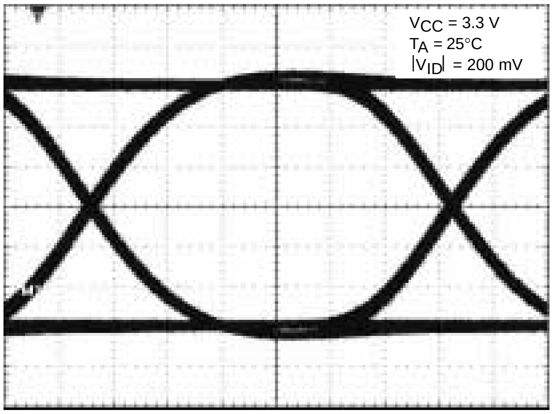


Horizontal Scale= 200 ps/div
LVDS-to-LVDS

Figure 19

LVDS122

1.5 Gbps, 2^{23} – 1 PRBS



Horizontal Scale= 100 ps/div
LVDS-to-LVDS

Figure 20

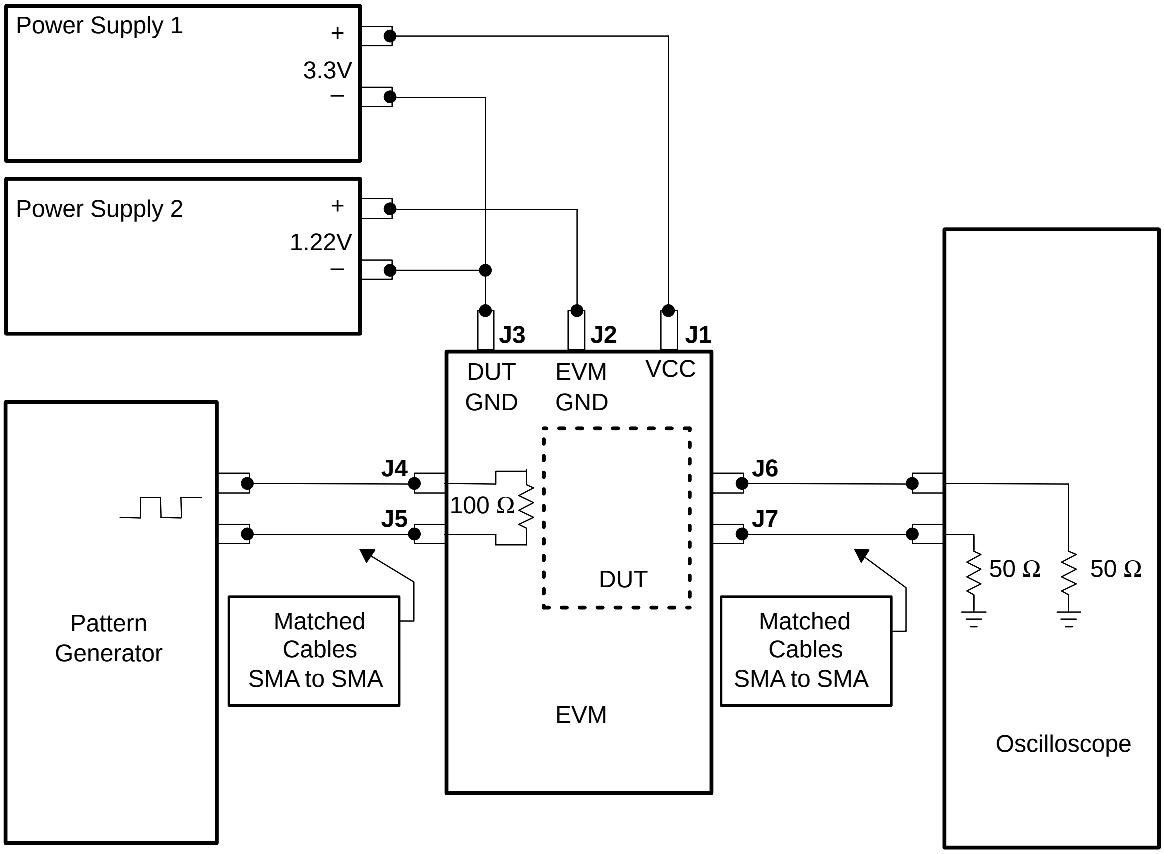


Figure 21. Jitter Setup Connections for SN65LVDS122

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, ETC.)

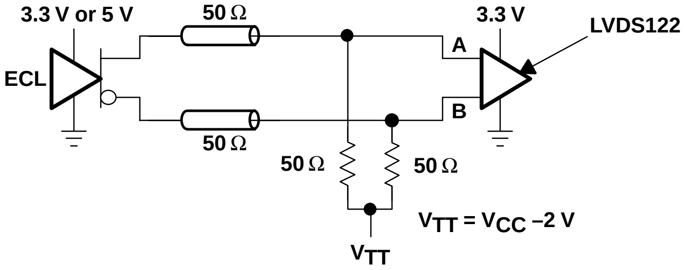


Figure 22. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

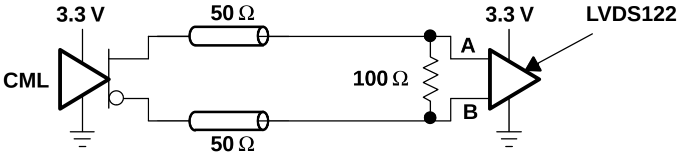


Figure 23. Common–Mode Logic (CML)

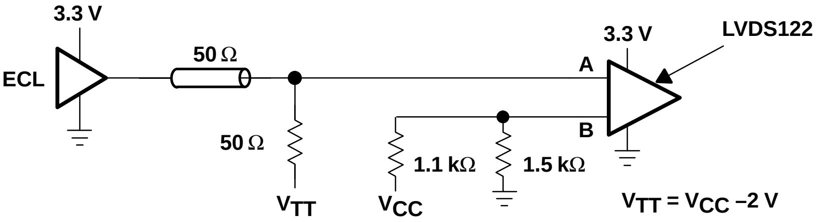


Figure 24. Single-Ended (LVPECL)

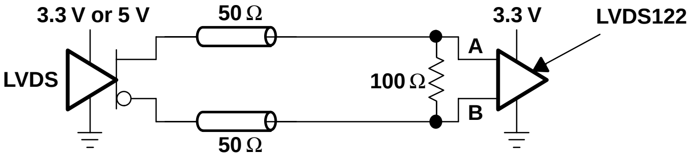


Figure 25. Low-Voltage Differential Signaling (LVDS)

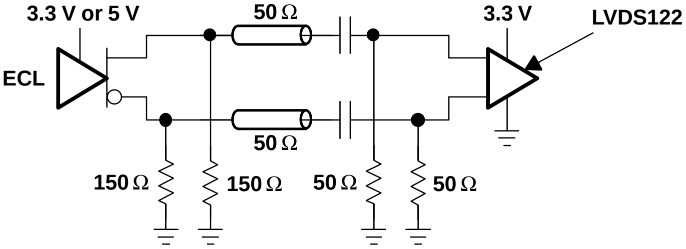


Figure 26. AC-Coupled Between ECL and LVDS or LVPECL

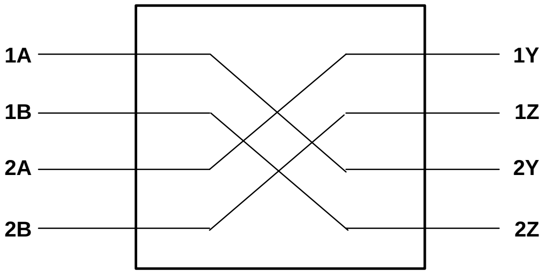


Figure 27. 2 x 2 Crosspoint

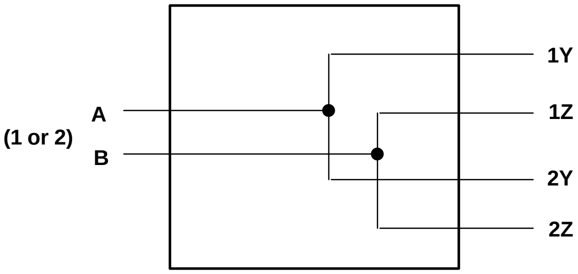


Figure 28. 1:2 Spitter

Figure 29. Dual Repeater

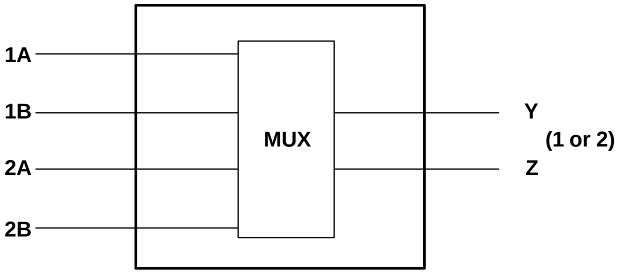
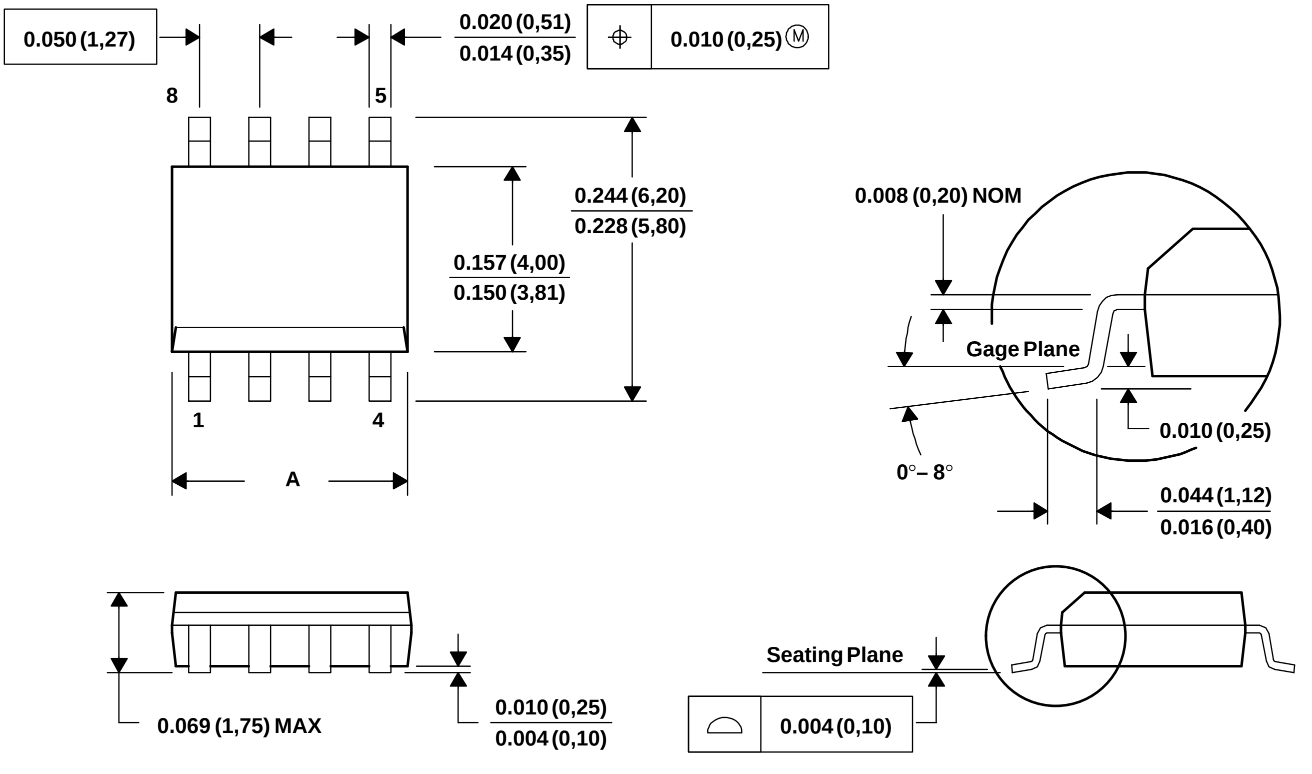


Figure 30. 2:1 MUX

MECHANICAL DATA

D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

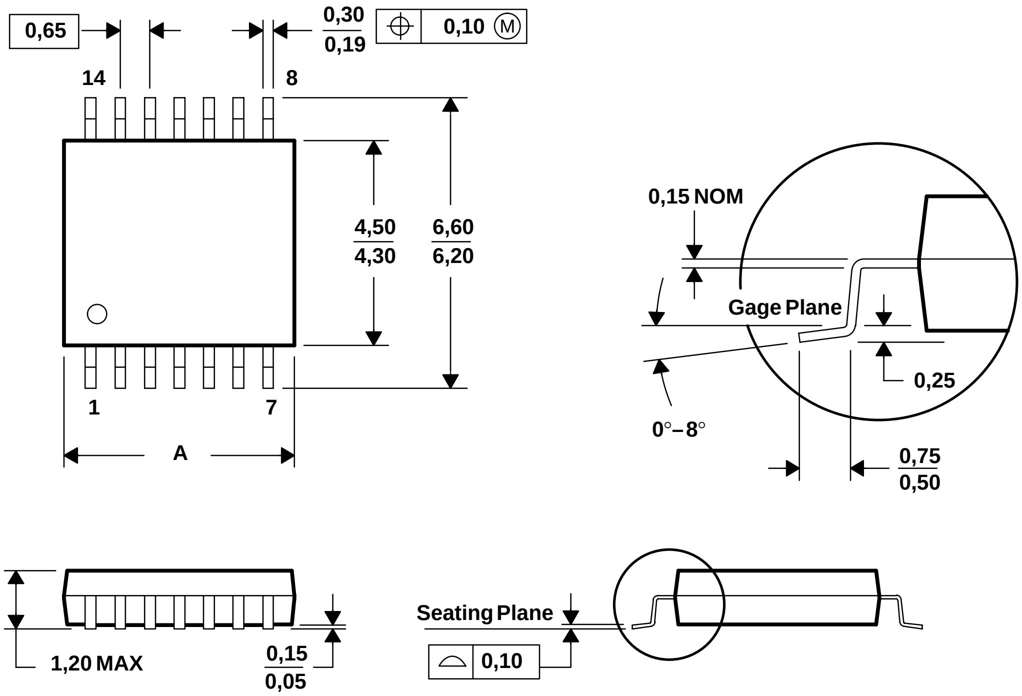
4040047/E 09/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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