



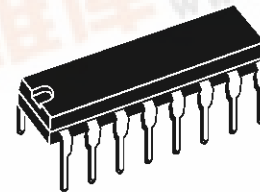
STV2145

I²C BUS CONTROLLED EAST-WEST AND VERTICAL INTERFACE

- INTEGRATED VERTICAL SAWTOOTH GENERATOR WITH AMPLITUDE CONTROL LOOP (50Hz - 60Hz)
- INTERLACE MODE INTRINSICALLY CONTROLLED BY STV2118A
- VERTICAL SIZE CORRECTION (BREATHING) TO ADAPT DEFLECTION SENSITIVITY TO THE CURRENT BEAM (HIGH VOLTAGE VARIATION)
- BUS ADJUSTED VERTICAL PARAMETERS : VERTICAL AMPLITUDE, VERTICAL POSITION AND S-CORRECTION
- EAST-WEST FUNCTION GENERATOR WITH INTEGRATED ERROR AMPLIFIER (THUS, ONLY 1 EXTERNAL POWER DARLINGTON IS NECESSARY FOR EW-FUNCTION)
- BUS CONTROLLED EAST-WEST FUNCTIONS : EW-AMPLITUDE, HORIZONTAL WIDTH, EW-TILT AND EW-SHAPE (CORNER CORRECTION)
- OVERSIZE BLANKING (VERTICAL AND HORIZONTAL) WHICH PERMIT ZOOM AND SUBTITLE FACILITIES FOR 4/3 AND 16/9 CRTs

DESCRIPTION

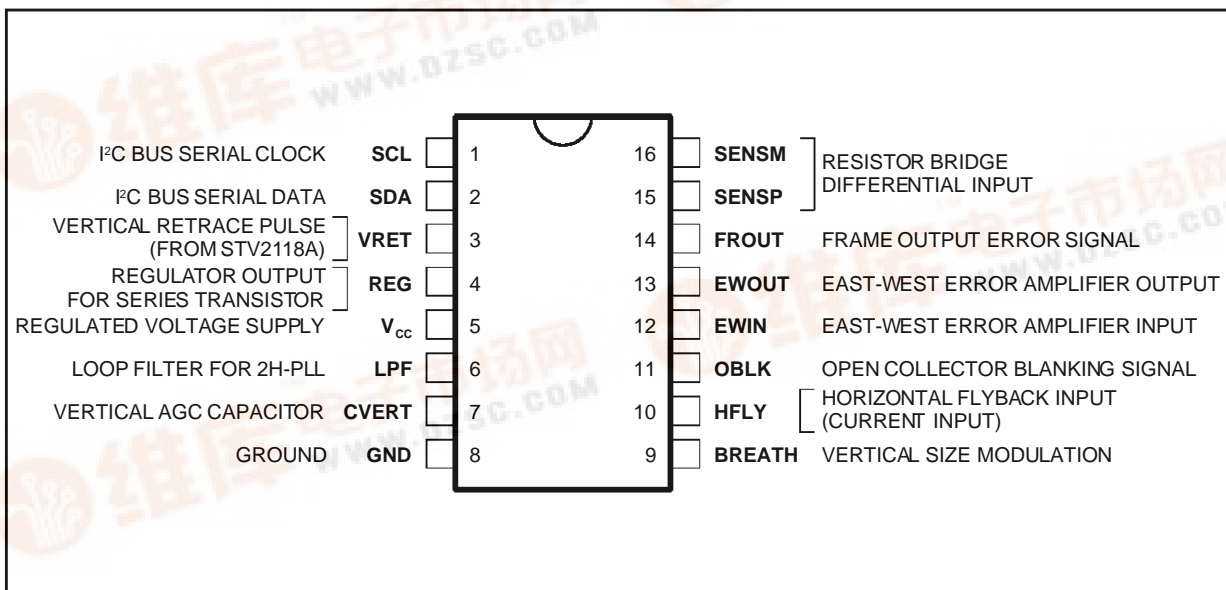
The STV2145 is an I²C bus processor containing the vertical deflection East-West functions and oversize blanking. This circuit is foreseen as ADD-ON for the Video Chroma Processor STV2118A to permit 110° CRT applications covering standard 4/3 screen format and new 16/9 format with zoom and subtitle facilities. STV2145 has been designed to drive a standard TDA8172/8177 vertical booster and an external transistor for East-West.



DIP16
(Plastic Package)

ORDER CODE : STV2145

PIN CONNECTIONS



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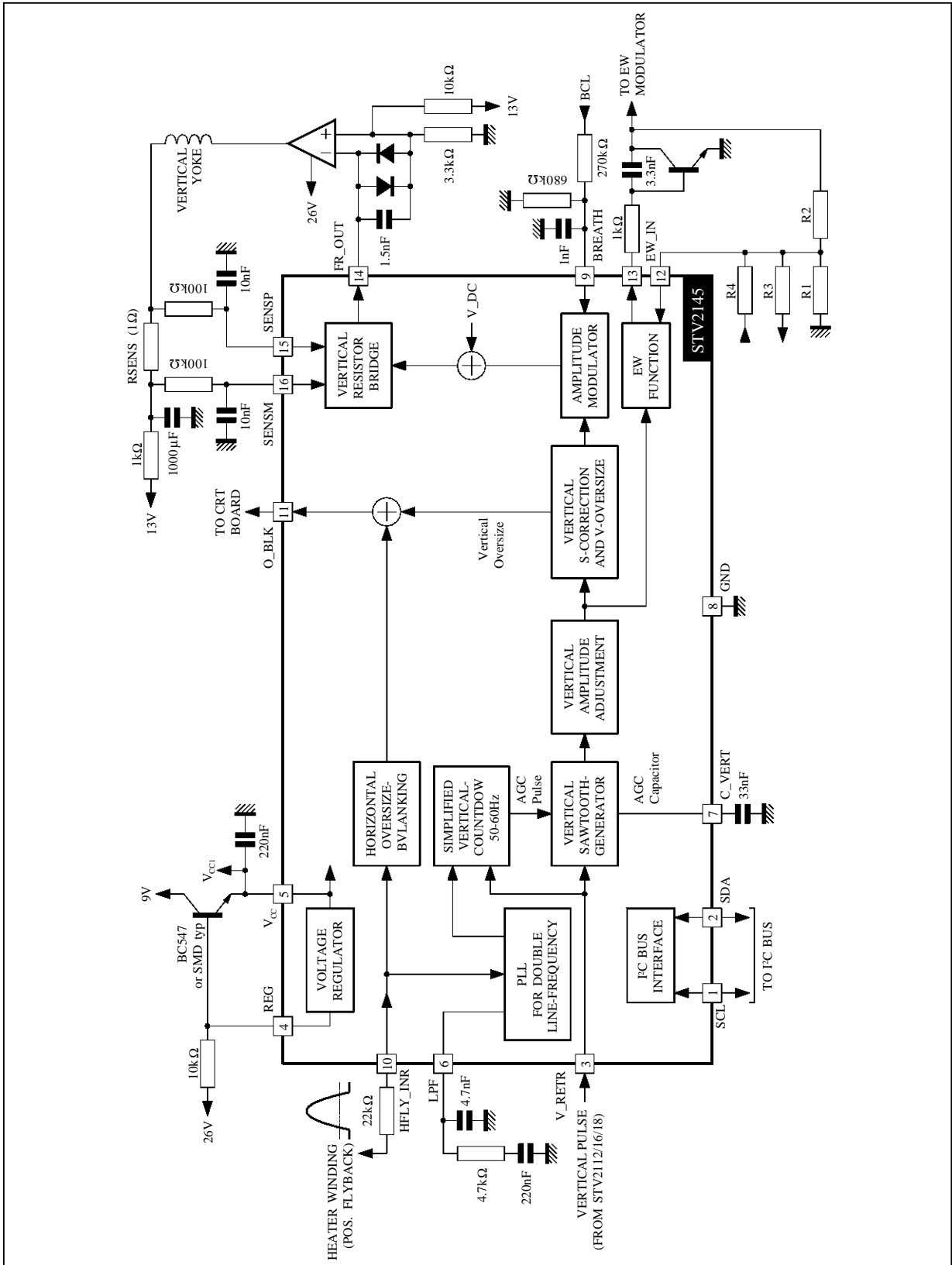
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PIN DESCRIPTION

Pin N°	Name	Function	Description
1	SCL	Serial Clock for I ² C Bus	Data input (no pull down - capability)
2	SDA	Serial Data for I ² C Bus	Data input and output (pull down - capability for acknowledge and data reply)
3	VRET	Vertical Reset Input	Vertical Synchronization Signal from STV2118A
4	REG	Control Pin for Regulator	Output for controlling the ext. series regulator transistor
5	V _{CC}	Supply Voltage Scanning	Supply voltage of scanning part, connected with external series regulator transistor
6	LPF	Loop Filter for PLL	Loop filter for horizontal 2 x F _{LINE} VCO
7	CVERT	Vertical AGC Capacitor	Regulation of vertical saw tooth amplitude
8	GND	Ground	Ground
9	BREATH	Breathing Input	Input voltage = 1 to 7.8V = vertical size compensation
10	HFLY	Horizontal Flyback Input	Voltage input for horizontal flyback, polarity positive
11	OBLK	Oversize Blanking Signal	Oversize blanking output : - open collector output : high ohmic = blanking - low (transistor saturated) = no blanking
12	EWIN	East-West Input	Input of the error amplifier for the East-West modulator
13	EWOUT	East-West Output	Output of the error amplifier for the East-West modulator (current output, biasing directly the darlington output transistor)
14	FROUT	Output for Frame Amplifier	Output of transconductance amplifier, pin has to be connected to the inverting input of the vertical power amplifier
15	SENSP	Sense Input, Positive	Input of internal resistor bridge for sensing the vertical deflection YOKE current
16	SENSM	Sense Input, Negative	Input of internal resistor bridge for sensing the vertical deflection YOKE current

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BLOCK DIAGRAM



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I²C BUS INFORMATION

Slave Address

hex 8C/8D

MSB							LSB
1	0	0	0	1	1	0	R/W

Address Mapping (write mode)

x = don't care bits, not used for the decoding of the subaddress.

Subaddress		Data Bits					
Binary	Hex	MSB					LSB
xxxxx000	x0 or x8		TEST_MODE	VERTICAL OVERSIZE BLANKING 2	VERTICAL OVERSIZE BLANKING 1	S_CORRECTION	
xxxxx001	x1 or x9		V_AMPLITUDE				
xxxxx010	x2 or xA		TEST_MODE	SUB_TITLE	V_DC		
xxxxx011	x3 or xB		HORIZONTAL OVERSIZE BLANKING 2	HORIZONTAL OVERSIZE BLANKING 1	EW_AMPLITUDE		
xxxxx100	x4 or xC					EW_SHAPE	
xxxxx101	x5 or xD		EW_LOW		EW_TILT		
xxxxx110	x6 or xE		TEST_MODE	H_WIDTH			

Subaddress 0 (hex 00) : Vertical Oversize Blanking & S_CORRECTION

MSB						LSB
TEST_MODE	OV_BLK_VERT2	OV_BLK_VERT1	S3	S2	S1	S0

TEST_MODE : 0 : Normal operations
 1 : Reserved for SGS-THOMSON test

OV_BLK_VERT1, : Vertical oversize blanking (register SUB_TITLE in subaddress X2 or XA)
 OV_BLK_VERT2 (see Table 1)

Table 1

TV Mode	Sent Frequency (via VRET)	OV_BLK_VERT ₂	OV_BLK_VERT ₁	SUB_TITLE	Start of Blanking (middle of line)	End of Blanking (middle of line)
STANDARD 4 :3	50Hz 60Hz	0	0	0	No Blanking	
SUBTITLE	50Hz 60Hz	Don't Care	Don't Care	1	302 259	67 59
ZOOM1	50Hz 60Hz	0	1	0	285 239	49 43
ZOOM2	50Hz 60Hz	1	1	0	278 234	59 49
BLANK	50Hz 60Hz	1	0	0	Full Blanking	

S1, S2, S3, S4 : S-CORRECTION

0000 (hex 00) : Maximal S-CORRECTION

1111 (hex 0F) : Minimal S-CORRECTION (vertical sawtooth flat)

I²C BUS INFORMATION (continued)**Subaddress 1 (hex 01) : Vertical Sawtooth Amplitude**

MSB						LSB
V6	V5	V4	V3	V2	V1	V0

V6, V5, V4, V3, : V_AMPLITUDE
 V2, V1, V0 : 0000000 (hex 00) : Minimal V_AMPLITUDE (0.46V_{PP} on SENSP/SENSM)
 1111111 (hex 7F) : Maximal V_AMPLITUDE (1.16V_{PP} on SENSP/SENSM)

Subaddress 2 (hex 02) : Vertical Shift & Vertical Position

MSB					LSB	
TEST_MODE	SUB_TITLE	V4	V3	V2	V1	V0

TEST_MODE : 0 : Normal operations
 1 : Reserved for SGS-THOMSON test

SUB_TITLE : DC shift of vertical sawtooth
 0 : Normal operations
 1 : Vertical Sawtooth shifted by 90mV upwards and unsymmetrical vertical
 oversize blanking (if nominal amplitude = V_AMPLITUDE = hex40)

V4, V3, V2, V1, V0 : Vertical position (V_DC)
 00000 (hex 00) : Minimal position (picture shifted down by -65mV on SENSP/SENSM)
 11111 (hex 1F) : Maximal position (picture shifted up by +65mV on SENSP/SENSM)

Subaddress 3 (hex 03) : Horizontal Oversize Blanking & EW-Amplitude

MSB					LSB	
OV_BLK_HOR2	OV_BLK_HOR1	E4	E3	E2	E1	E0

OV_BLK_HOR1, : Horizontal oversize blanking (see Table 2)
 OV_BLK_HOR2

Table 2

TV Mode	OV_BLK_HOR2	OV_BLK_HOR1	Reference is Rising Edge of Positive HFLY-Back (μs)	
			Start of Blanking	End of Blanking
STANDARD 4:3	0	Don't Care	0	11.5
ZOOM1 (14:9)	1	0	-1.7	13.7
ZOOM2 (16:9)	1	1	-3.2	15.2

E4, E3, E2, E1, E0 : EW-AMPLITUDE
 00000 (hex 00) : Maximal parabola amplitude = 0.74V for EW_LOW = 0 ; 0.48V for
 EW_LOW = 1
 11111 (hex 1F) : Minimal parabola amplitude = 0.26V for EW_LOW = 0 ; 0.0V for
 EW_LOW = 1

Subaddress 4 (hex 04) : EW_SHAPE

EW_SHAPE : 0000 (hex 00) : Maximal parabola flattening (flattened corners of parabola)
 1111 (hex 0F) : Minimal parabola flattening (ideal parabola)

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I²C BUS INFORMATION (continued)

Subaddress 5 (hex 05) : EW_Parabola Range Switch & East-West - Tilt Adjustment

MSB						LSB
	EW_LOW	T4	T3	T2	T1	T0

- EW_LOW : Switch for parabola amplitude range
0 : Parabola amplitude from 0.26 to 0.74V
1 : Parabola amplitude from 0 to 0.48V
- T4, T3, T2, T1, T0 : East-west tilt (unsymmetry)
00000 (hex 00) : Minimal position : parabola unsymmetrical, (higher on the top of the picture)
10000 (hex 10) : Parabola symmetrical
11111 (hex 1F) : Maximal position : parabola unsymmetrical, (lower on the top of the picture)

Subaddress 6 (hex 06) : Picture Width (H_WIDTHH)

MSB						LSB
TEST_MODE	W5	W4	W3	W2	W1	W0

- TEST_MODE : 0 : Normal operations
1 : Reserved for SGS-THOMSON test
- W5, W4, W3, W2, W1, W0 : H_WIDTHH (picture width)
000000 (hex 00) : Minimal position : DC_Value of parabola minimal
111111 (hex 3F) : Maximal position : DC_Value of parabola maximal

Output Signals (Read Mode)

MSB				LSB	
PON_RESET	S60/50	VCO_LOCK	VERS_NBR	VERS_EXT	

- PON_RESET : 1 : If Voltage drop has been detected (risk of data loss in latch memory)
- S60/50 : 0 : If VRET frequency = 50Hz
1 : If VRET frequency = 60Hz
- VCO_LOCK : 0 : If PLL FH2 is out of frequency or phase
1 : If PLL FH2 has locked
- VERS_NBR : Number of actual cut (for SGS-THOMSON use)
- VERS_EXT : Number of metal version (for SGS-THOMSON use)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage (pin 5)	9	V
V _{SCL} , V _{SDA}	Separated Protection Structures to these Pins 1 and 2	6	V
V _{SENSP} , V _{SENSM}	No Protection Diodes to V _{CC} in Order to Allow Half Bridge Operation (Pins 15 and 16)	20	V
T _{oper}	Operating Ambient Temperature	0, +70	°C
T _{stg}	Storage Temperature	-55, +150	°C

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THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th (j-a)}	Junction-ambient Thermal Resistance	Max. 70	°C/W

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ELECTRICAL CHARACTERISTICS (V_{CC} = 7.8V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY (Pin 5) (see Note 1)						
P _{max}	Total Power Consumption	Typical power consumption		0.15		W
I _{max}	Current Capability (Pin 4)	Maximum current pulled down by Pin 4			15	mA
	Line Ripple Rejection (see Note 2)	External transistor, Pin 4 connected with 3.3kΩ against Power Supply (e.g. 12V ; recommended current into REG = 1mA), ΔV _{CC} / ΔV _{power}	-35			dB
	Load Regulation (see Note 2)	External transistor, Pin 4 connected with 3.3kΩ against Power Supply (12V), ΔV _{CC} / ΔI _{E(regulation transistor)}			1	mV/mA
V _{NOM}	Regulation Voltage	External regulation transistor, Pin 4 connected via 3.3kΩ resistor against 12V	7.5	7.8	8.2	V

I²C BUS (Pins 1 and 2)

V _{TH}	Input Threshold Voltage		1.5	2.1	2.7	V
I _{BUS}	Input Current	V ₁ and V ₂ = 5V			40	μA
Data	Saturation Voltage	Open collector of pull-down transistor at 5mA			0.5	V
	Pull-down Current	No pull-down capability. Pin 1 can't be pulled down to slow down clock SCL of microprocessor				
f _{Max.}	Maximum Toggle Frequency		200			kHz

TIME BASE GENERATION INTERFACES

HFLY INTERFACE (Pin 10)						
	Polarity of Horizontal Flyback	Preferable heater-winding of EHT-transformer (flyback voltage positive during horizontal flyback)	Positive			
V _{TH}	Threshold Voltage	V _{BE} voltage comparator	0.5	0.7	1.0	V
V _{CLP}	Positive Clamp Voltage	Clamping voltage = V _{TH} + V _{BE}		1.6		V
I _{CLPP}	Maximum Positive Clamping Current	Input voltage exceeds positive clamping voltage			4	mA
V _{CLP}	Negative Clamping Voltage	Clamping voltage = V _{TH} - V _{BE}		0		V
I _{CLPP}	Minimum Negative Clamping Current	Input voltage smaller than negative clamping voltage	-2			mA

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- Notes :**
- Supply voltage is regulated via external series regulator transistor.
 - Parameter is not tested during production, but it is guaranteed by the design and qualified by means of corner lots.

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ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = 7.8V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TIME-BASE GENERATION INTERFACES (continued)						
OVERSIZE BLANKING OUTPUT (Pin 11) (see Note 3)						
I_O	Output Current	V_{OBLK} (Saturation Voltage) < 0.5V			10	mA
V_O	Output Voltage	$I_{OBLK} = 5mA$	0		0.4	V
t_R, t_F	Rise Time / Fall Time	Output Load = 2.2k Ω against V_{CC}		100		ns
HORIZONTAL OVERSIZE BLANKING (Pin 11) (see Figure 1)						
OB_R OB_L	Horizontal Oversize	Bus register $OV_BLK_HOR1,2 = (00)$		-0.3 0.3		μs μs
OB_R OB_L	Horizontal Oversize	Bus register $OV_BLK_HOR1,2 = (01)$	1.45 1.5	1.9 1.7	2.35 1.9	μs μs
OB_R OB_L	Horizontal Oversize	Bus register $OV_BLK_HOR1,2 = (11)$	2.95 2.9	3.4 3.2	3.85 3.6	μs μs
OB_R OB_L	Horizontal Oversize Blanking Unsymmetry	Bus register $OV_BLK_HOR1,2 = (11)$	-0.4	0.2	0.8	μs
FH2 PHASE COMPARATOR (Pin 6)						
I_{OUT}	Output Current			100		μA
ΔI	Current Ratio	Ratio of charging / discharging current (unsymmetry)		1		
VRET INTERFACE (Pin 3)						
	Polarity of VRET	Negative pulse, starts the vertical retrace	Negative			
V_{TH}	Threshold Voltage	$V_{CC} = 7.8V$ (threshold value derived from V_{CC})	2.7	3.0	3.3	V
I_{IN}	Input Current	Input Voltage : $0V < V_{VRET} < 7.8V$	-5		+5	μA

VERTICAL DEFLECTION

VERTICAL LOGIC (countdown circuit for vertical deflection, 50/60Hz recognition and vertical oversize blanking)						
	Free Running Period	No V_Sync pulses (VRET) present		377		lines
	Search Window 60Hz		240		277	lines
VERTICAL OVERSIZE BLANKING (countdown circuit used also for vertical oversize blanking) (Pin 11)						
	Oversize Blanking Disable	$OV_BLK_VERT1,2 = (0,0)$ $SUB_TITLE = 0$; there is no influence of 50 or 60Hz Mode (OBLK always low-level)	No Blanking			
	Vertical Oversize Blanking Subtitle Mode	$SUB_TITLE = 1$; values are the blanked lines Input Frequency $f_{VRET} = 50Hz$ Input Frequency $f_{VRET} = 60Hz$	302 259		67 59	middle of line
	Vertical Oversize Blanking Zoom 1 Mode	$OV_BLK_VERT1,2 = (1,0)$ $SUB_TITLE = 0$; values are the blanked lines Input Frequency $f_{VRET} = 50Hz$ Input Frequency $f_{VRET} = 60Hz$	285 239		49 43	middle of line
	Vertical Oversize Blanking Zoom 2 Mode	$OV_BLK_VERT1,2 = (1,1)$ $SUB_TITLE = 0$; values are the blanked lines Input Frequency $f_{VRET} = 50Hz$ Input Frequency $f_{VRET} = 60Hz$	278 234		59 49	middle of line
	Vertical Oversize Blanking Blank Mode	$OV_BLK_VERT1,2 = (0,1)$ $SUB_TITLE = 0$; there is no influence of 50 or 60Hz Mode (OBLK always high-level)	Full Blanking			

Notes : 3. Open collector output, polarity positive : High (high impedance) : oversize blanking
Low (transistor pulled to Ground) : no blanking

ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = 7.8V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VERTICAL DEFLECTION (continued)						
VERTICAL RAMP GENERATOR (see Figure 2) (see Note 6)						
V_{SAW}	Sawtooth Amplitude	S_CORRECTION = 1111 Register V_AMPLITUDE				
	Min. Value	= minimum (000000) value V_{PP} for 190 lines difference	0.38	0.46	0.55	V
	Max. Value	= maximum (111111) value V_{PP} for 190 lines difference	1.11	1.16	1.21	V
V_{MID}	Sawtooth DC-Level	SUB_TITLE = 0				
	Nom. Value	Register V_DC = (10000) ; (no V-shift)		0		mV
	Min. Value	Register V_DC = (00000) ; (UP-shift)	55	65	75	mV
	Max. Value	Register V_DC = (11111) ; (DOWN-shift)	-75	-65	-55	mV
V_SUBTITLE (see Note 7)						
SUB_TITLE	Vertical DC-Shift for Subtitle Mode	Register SUB_TITLE = 1 (this value affects a vertical UP-shift of about 20 lines)	70	90	110	mV
VERTICAL S-CORRECTION (see Figure 3) (See Notes 4 and 5)						
TF_{MID}	Middle Fix Point	50Hz Mode ; measurement method : difference $SCO_{MAX} - SCO_{MIN}$ is measured at line 160 and 174 ; the middle line TF_{MID} is calculated by linear interpolation (for 60Hz , the middle line shifts to line 140 ; not measured)	157	167	177	line
ΔVF_{UP} ΔVF_{LOW}	Fix-Point Upper at line 72	50Hz Mode Difference $\Delta VF_{UP} = SCO_{MAX} - SCO_{MIN}$ measured at line 72 if V_AMPLITUDE = (111111)		0		
	Lower at line 262	Difference $\Delta VF_{LOW} = SCO_{MAX} - SCO_{MIN}$ measured at line 262 if V_AMPLITUDE = (111111)				
ΔV_{SAWMAX}	Maximum Correction Voltage at line 127	50Hz Mode Difference $\Delta VF_{UP} = SCO_{MAX} - SCO_{MIN}$ measured at line 127 if V_AMPLITUDE = (111111)	20	40	60	mV
	at line 207	Difference $\Delta VF_{LOW} = SCO_{MAX} - SCO_{MIN}$ measured at line 207 if V_AMPLITUDE = (111111)	-60	-40	-20	mV
VERTICAL BREATHING (Pin 9) (Breathing effect $BR = 100\% * (V_{SAW} - V_{SAWB}) / V_{SAW}$) (see Notes 4 and 5) (see Figure 4)						
BR_{Min} BR_{Max}	Breathing Effect			0		%
	Min. Value	$V_9 = 7.8V$		5.3		%
	Max. Value	$V_9 = 1.5V$ measurement at line 72 and 262				%
VERTICAL BRIDGE AND OUTPUT STAGE (see Figure 5)						
	Sense Input Voltage	Input Pins 16 and 15 - Differential input (see Note 2)	10		20	V
	Min. Value	$V_{14} \leq 3V$				V
	Max. Value	$V_{14} \leq 5V$				
	Input Impedance (Pins 15-16)	Resistor value of the internal resistor-bridge		15		k Ω
I_{OUT}	Output Current (Pin 14)	$V_{14} = 3V$, V_{16} and $V_{15} > 10V$		± 100		μA
V_{OUT}	Output Voltage (Pin 14)	$V_{16} > 10V$				
	Min. Value			1		V
	Max. Value			5		V
$\Delta I_{OUT} / \Delta V_{IN}$	Transconductance (Pin 14)	Input voltage ΔV_{IN} = difference voltage between Pin 16 and Pin 15		0.5		mA/V

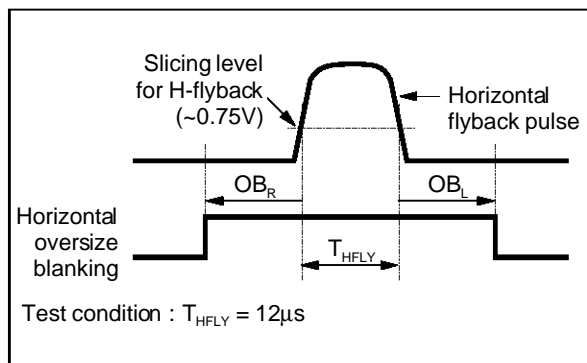
- Notes :**
- Parameter is not tested during production, but it is guaranteed by the design and qualified by means of corner lots.
 - Parameter is measured in EWS, with limits enlarged due to tester accuracy
 - Vertical output signals like vertical sawtooth, breathing and S-correction can only be measured via external test circuit (see Figure 10).
 - Voltage V_{SAW} only indirectly measurable via application circuit in closed loop condition (voltage-drop across R_{SENS}) for all vertical functions : see Note 5.
 - DC-shift of internal sawtooth-voltage; thus maintenance of fix-points for EW-Parabola and S-CORRECTION

ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = 7.8V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VERTICAL DEFLECTION (continued)						
EAST-WEST CORRECTION (Pins 13-12) (See Figure 6)						
	Output-Current			-2.5 to +3		mA
	Output Voltage Range	Application : Output Darlington-Transistor		-0.5 to +2		V
V_{PAR}	Parabola Amplitude EW_LOW = 0 Max. Value Min. Value EW_LOW = 1 Max. Value Min. Value	See Figure 7 H_WIDTH = (000000), EW_TILT = (10000), EW_SHAPE = (11111) EW_AMPLITUDE = (00000) EW_AMPLITUDE = (11111), (Parabola = 1/3) EW_AMPLITUDE = (00000) EW_AMPLITUDE = (11111)	0.63 0.21	0.75 0.27	0.87 0.33	V_{PP} V_{PP}
ΔV_{PAR}	Parabola Amplitude Ratio (EW_LOW = 0)	$\Delta V_{PAR} = V_{PAR} (EW_AMPLITUDE) = (00000) / V_{PAR} (EW_AMPLITUDE) = (11111)$	2.4	3	3.5	
V_{DC-MIN} V_{DC-MAX}	Parabola DC Min. Value Max. Value	EW_TILT = (10000), EW_SHAPE = (1111), EW_LOW = 0, EW_AMPLITUDE = (10000) Register H_WIDTH = (000000) (min. picture width) Register H_WIDTH = (111111) (max. picture width)	2.4 3.65	2.65 3.8	2.9 3.95	V V
TILT	Parabola Unsymmetry (see Figure 8) Max. Value Min. Value	Value is ratio between upper and lower parabola value. $TILT = V_{PARUP} / V_{PARLOW}$ H_WIDTH = (000000), EW_SHAPE = (1111), EW_LOW = 0, EW_AMPLITUDE = (10000) Register EW_TILT = (11111) Register EW_TILT = (00000)		1.83 0.55		
R_{MAX} R_{MIN}	Parabola Shape Deformation (see Figure 9) Max. Value Min. Value	$R = V_{DEF} / V_{PAR}$ H_WIDTH = (000000), EW_TILT = (10000), EW_LOW = 0, EW_AMPLITUDE = (00000) Register EW_SHAPE = (0000) Register EW_SHAPE = (1111) (no parabola deformation), V_AMPLITUDE = (1111111)		0.07 0		

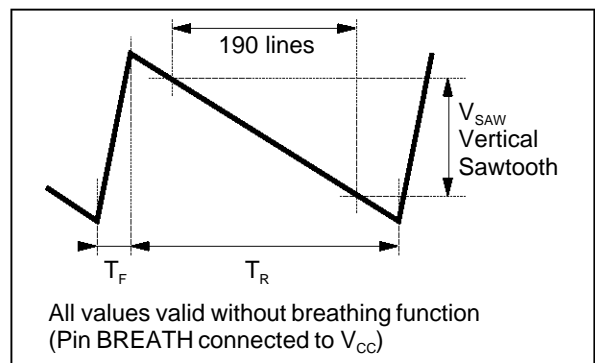
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Figure 1



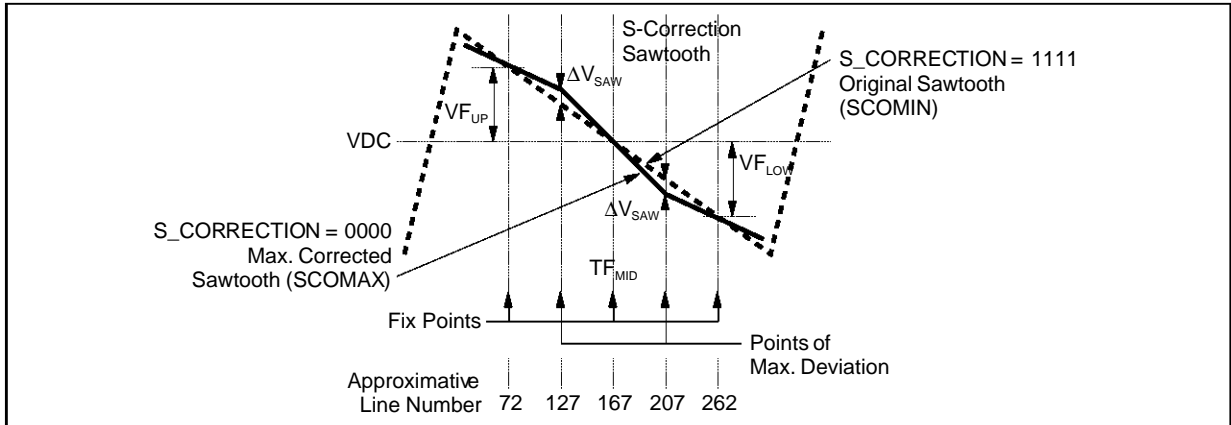
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Figure 2



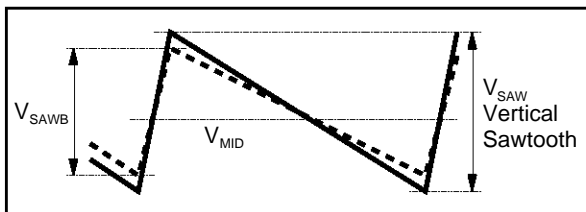
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Figure 3



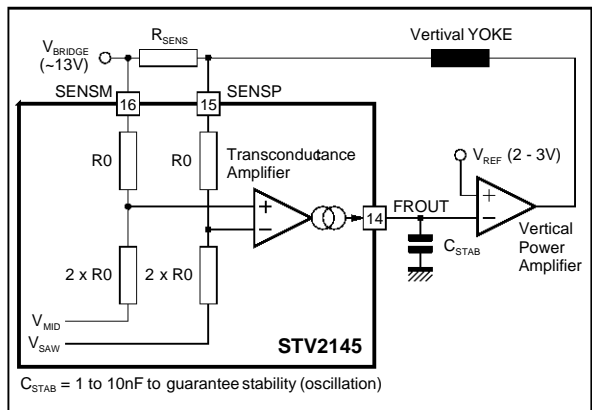
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Figure 4



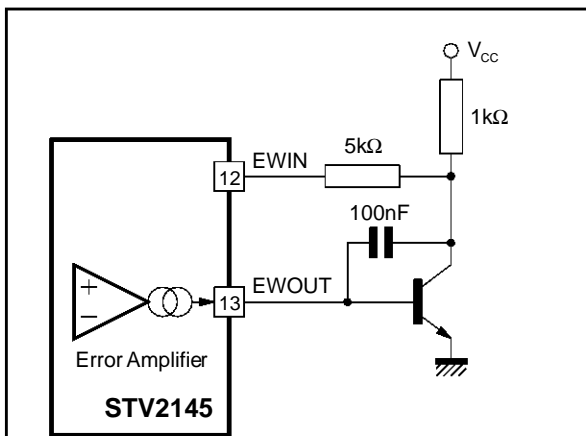
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Figure 5



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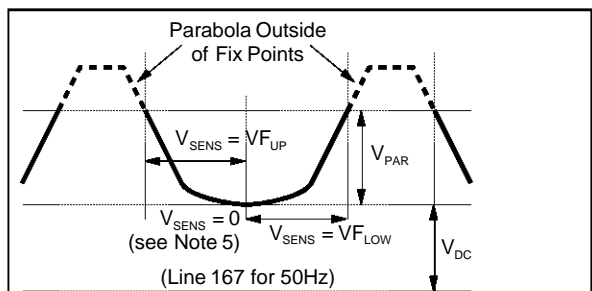
Figure 6



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Test circuit : all measurement values are related to this test circuit, measured at Pin EWIN. All East-West values below are depending on the following settings : $V_AMPLITUDE = (1111111)$ and no breathing (Pin BREATH at V_{CC}).

Figure 7



Amplitude defined for the Fix points $V_{F_{UP}}$ and $V_{F_{LOW}}$ (definition see : vertical ramp generator). Note : valid for all following definitions of parabola amplitude : between $EW_AMPLITUDE = mon.$ and $max.$ there is a linear progression in the amplitude V_{PAR} .

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Figure 8

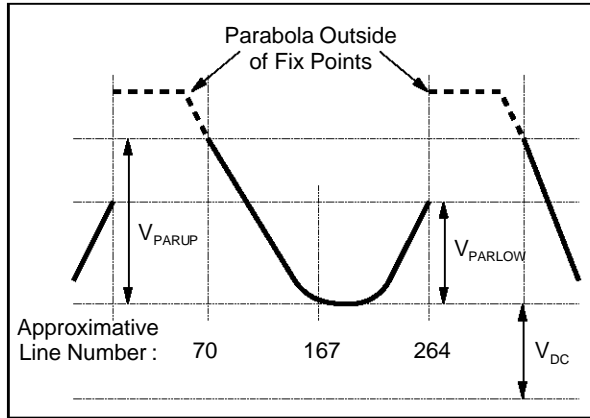


Figure 9

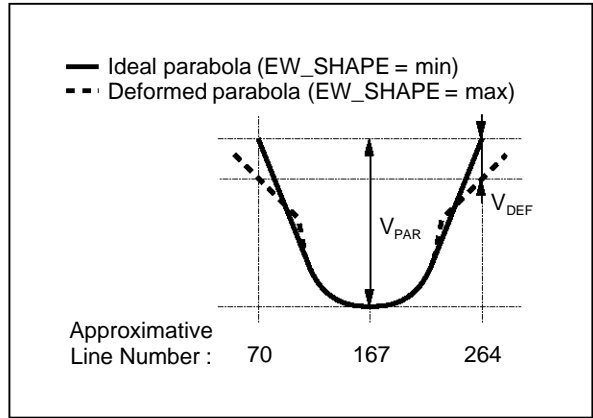
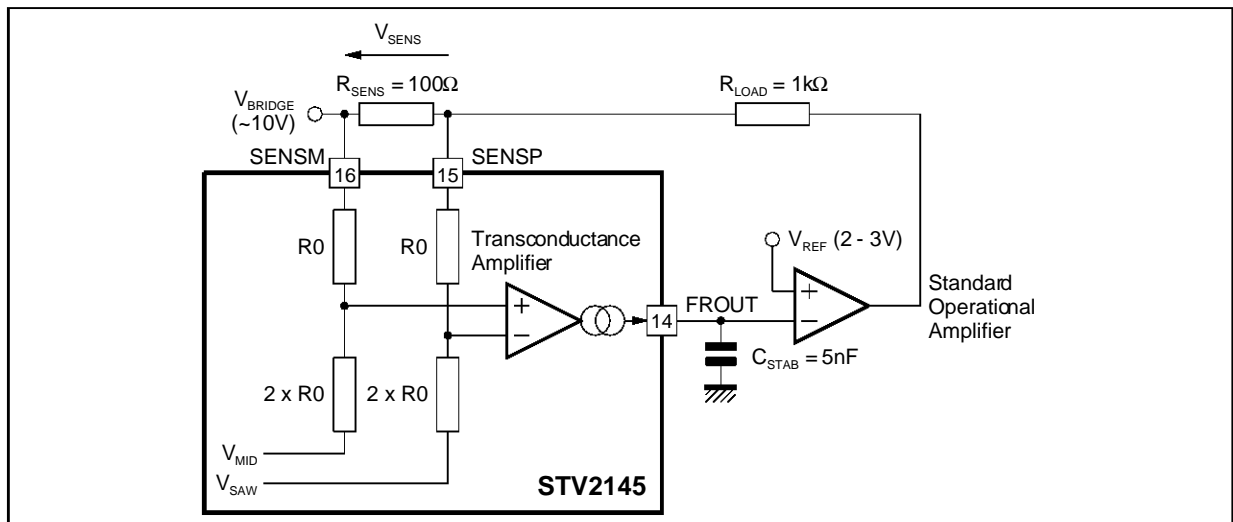
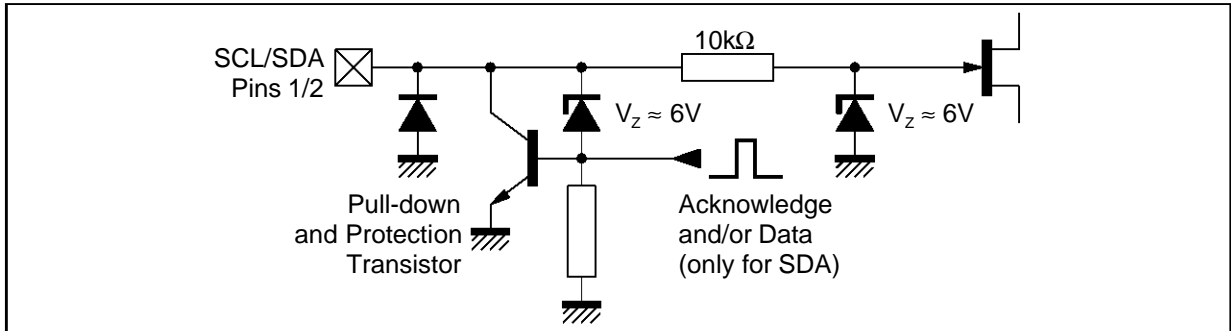


Figure 10



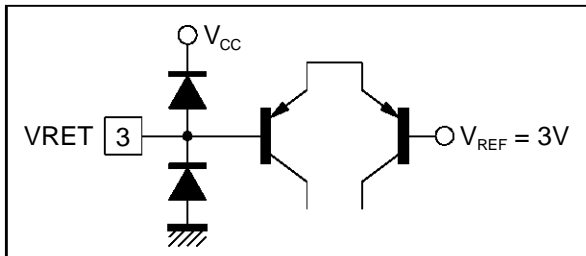
INPUTS/OUTPUTS PIN CONFIGURATION

Figure 11



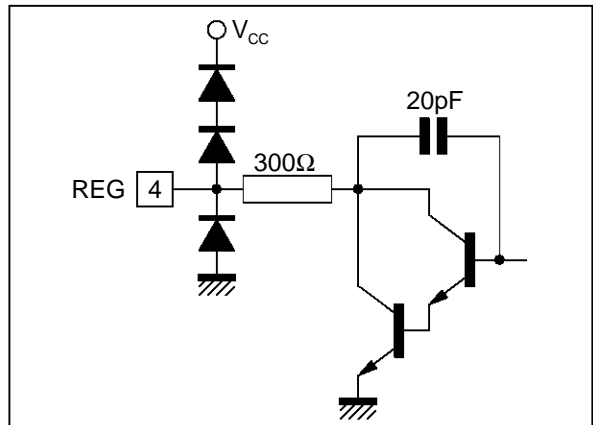
2145-13.EPS

Figure 12



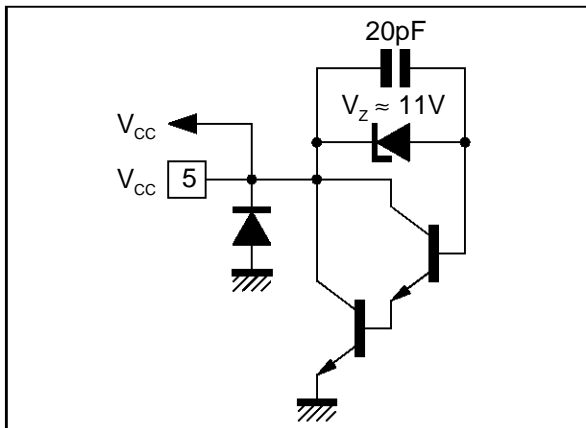
2145-14.EPS

Figure 13



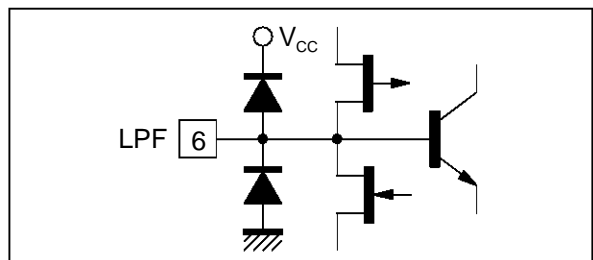
2145-15.EPS

Figure 14



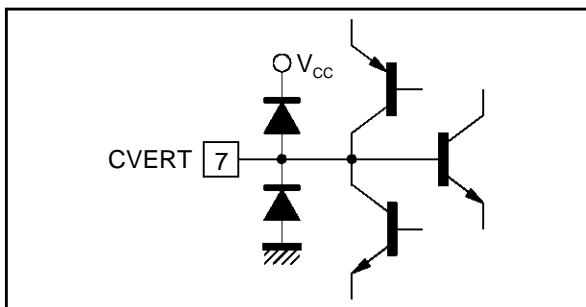
2145-16.EPS

Figure 15



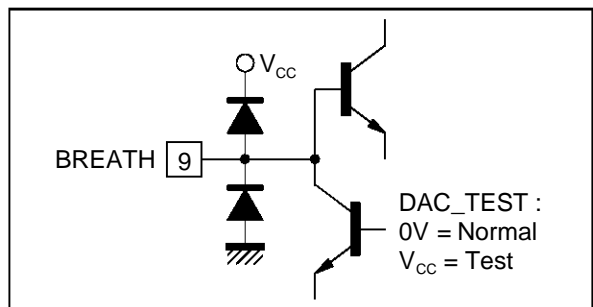
2145-17.EPS

Figure 16



2145-18.EPS

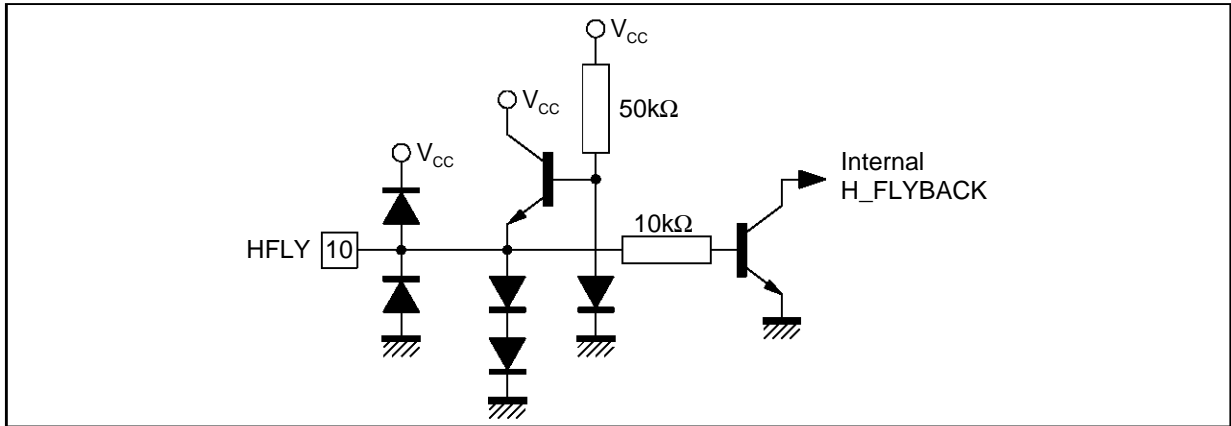
Figure 17



2145-19.EPS

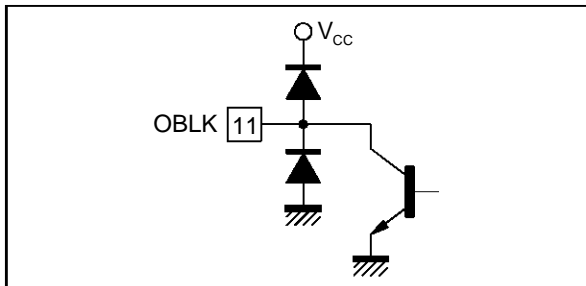
INPUTS/OUTPUTS PIN CONFIGURATION (continued)

Figure 18



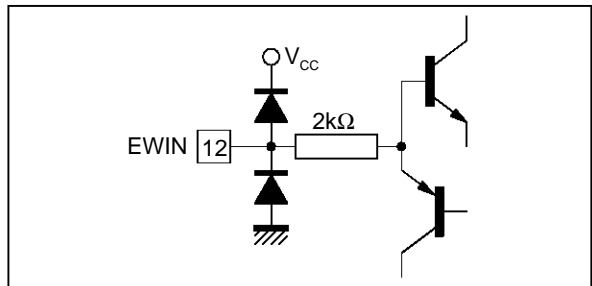
2145-20.EPS

Figure 19



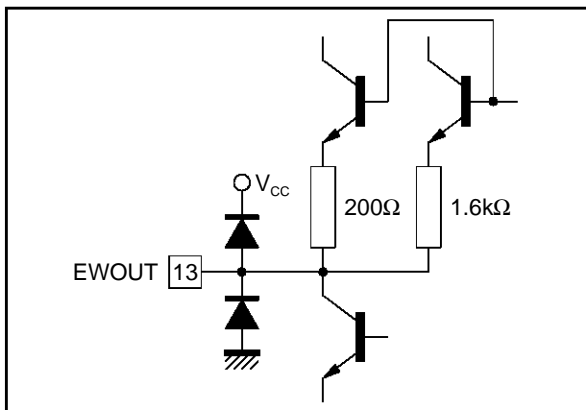
2145-21.EPS

Figure 20



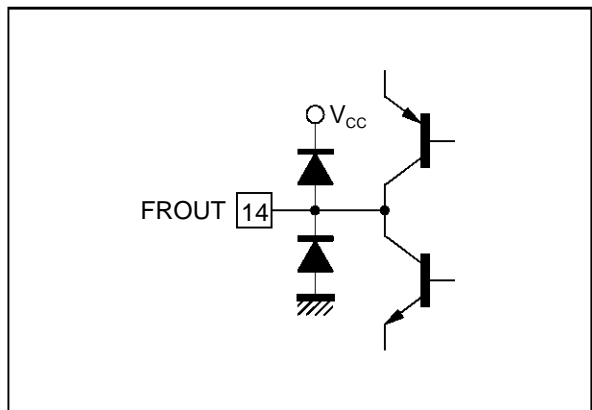
2145-22.EPS

Figure 21



2145-23.EPS

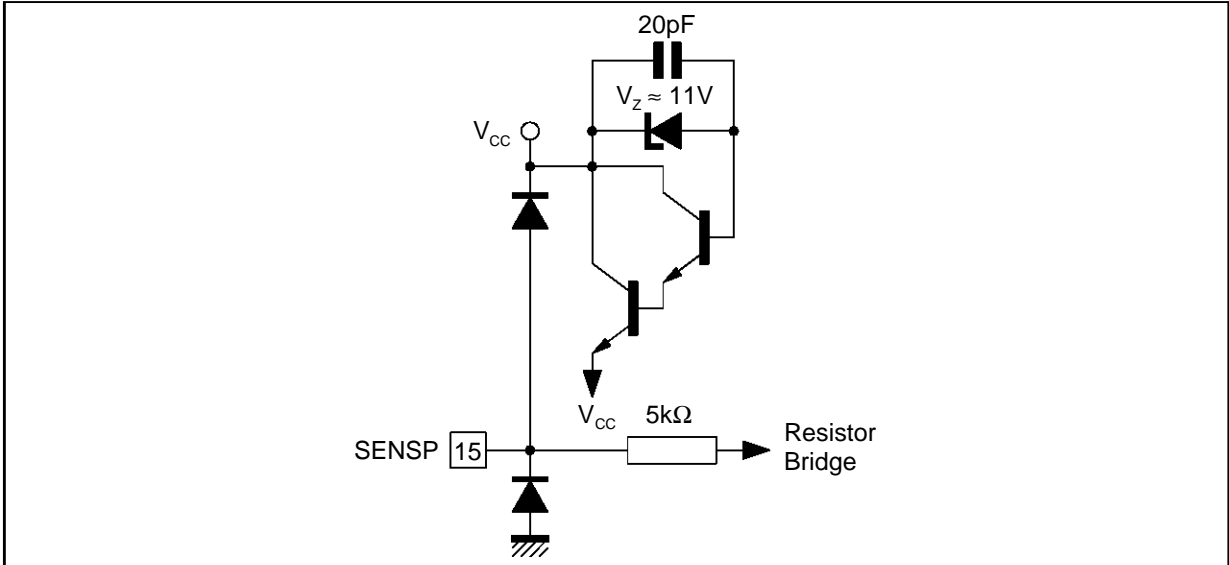
Figure 22



2145-24.EPS

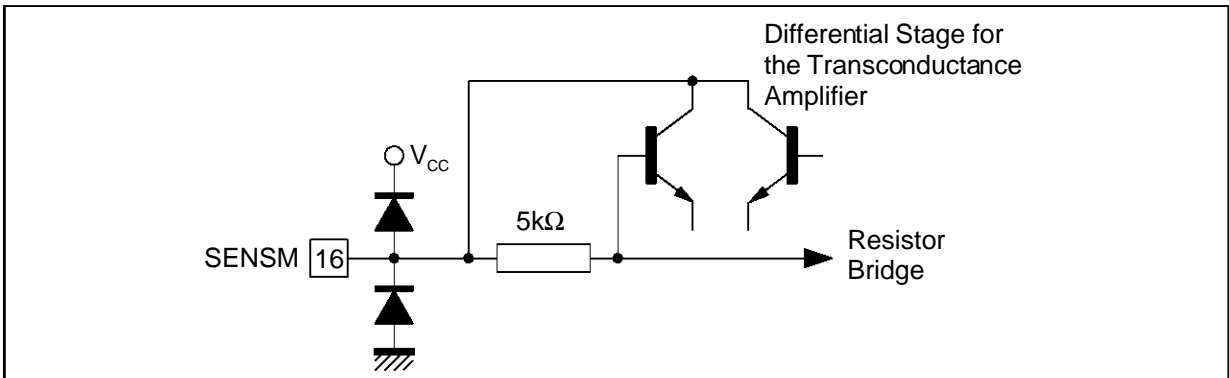
INPUTS/OUTPUTS PIN CONFIGURATION (continued)

Figure 23



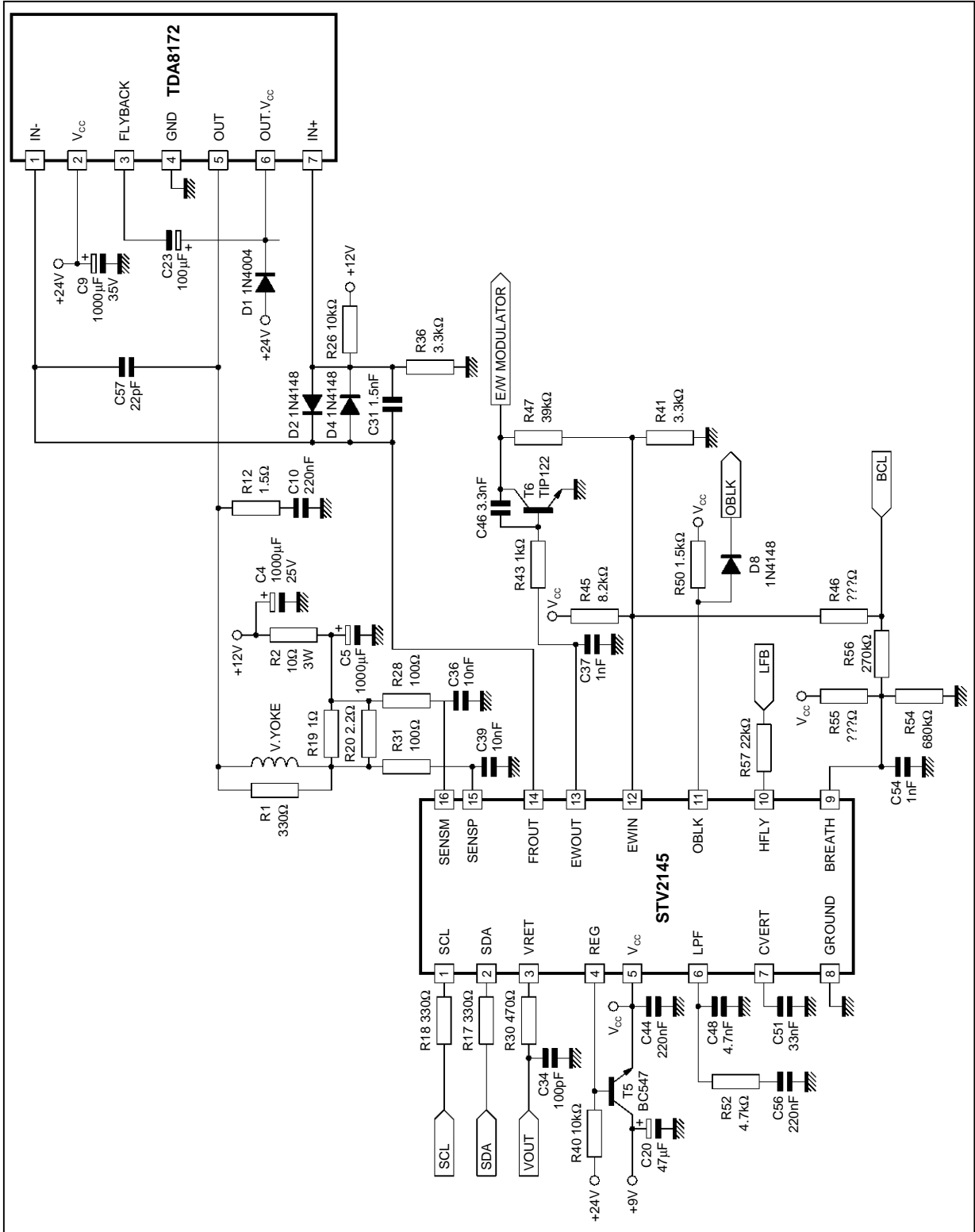
2145-25.EPS

Figure 24



2145-26.EPS

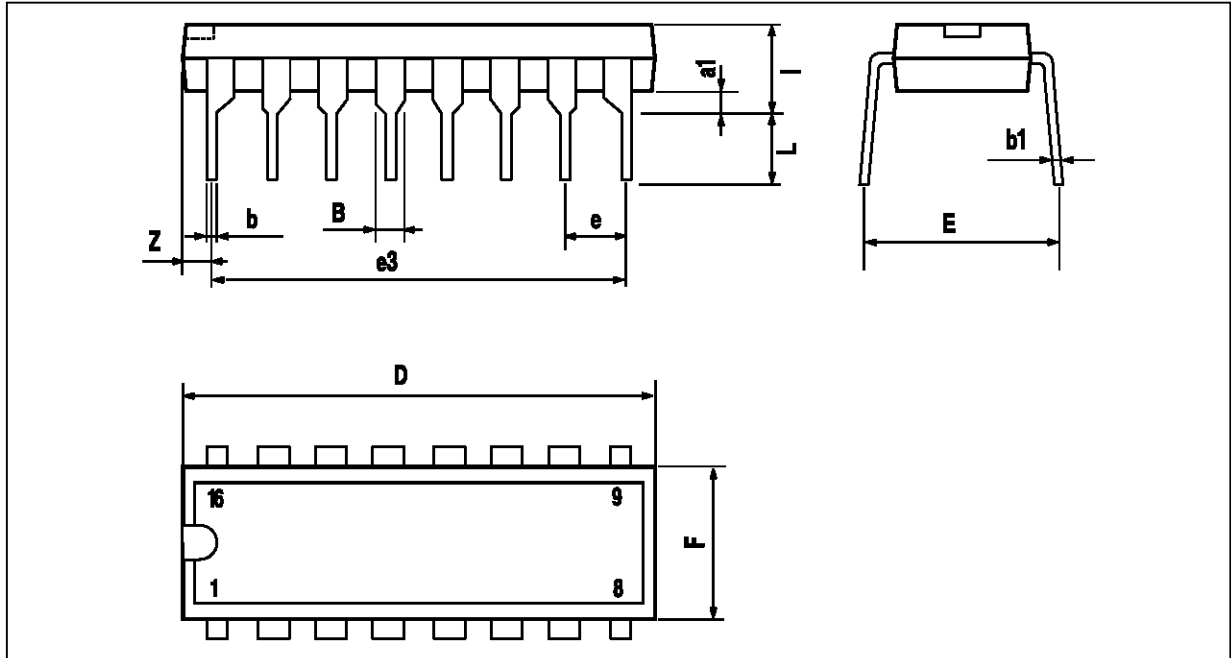
TYPICAL APPLICATION



2145-27-EPS

PACKAGE MECHANICAL DATA

16 PINS - PLASTIC PACKAGE



PM-DIP16.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

DIP16.TBL

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