

FAIRCHILD
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DM74S299 3-STATE 8-Bit Universal Shift/Storage Register

General Description

This Schottky TTL eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, HIGH. This places the 3-STATE outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are ENABLED or OFF.

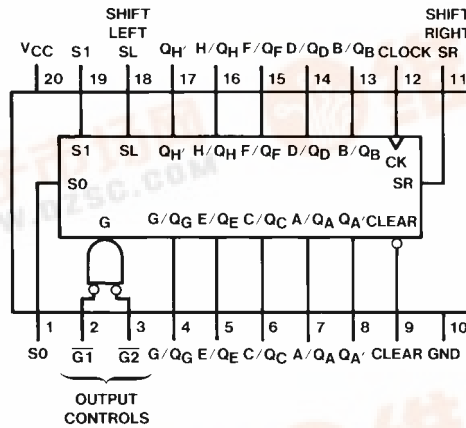
Features

- Multiplexed inputs/outputs provide improved bit density
- Four modes of operation:
 - Hold (Store) Shift Left
 - Shift Right Load Data
- 3-STATE outputs drive bus lines directly
- Can be cascaded for N-bit word lengths
- Operates with outputs enabled or at high Z
- Guaranteed shift (clock) frequency 50 MHz
- Typical power dissipation 700 mW

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| DM74S299N | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Connection Diagram



DM74S299 3-STATE 8-Bit Universal Shift/Storage Register



Function Table

| Mode | Inputs | | | | | | Inputs/Outputs | | | | | | | | Outputs | | | | |
|-------------|--------|--------------------|----------------|----|-------|----------------|----------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|---------------------------------|----|----|
| | Clear | Function Select | Output Control | | Clock | Serial | | A/Q _A | B/Q _B | C/Q _C | D/Q _D | E/Q _E | F/Q _F | G/Q _G | H/Q _H | Q _{A'} | Q _{H'} | | |
| | | | S1 | S0 | | G1 (Note 1) | G2 (Note 1) | | | | | | | | | | | SL | SR |
| | | | L | L | | L | L | | | | | | | | | | | X | X |
| Clear | L | X | L | L | X | X | X | X | L | L | L | L | L | L | L | L | L | | |
| Hold | L | L | X | L | X | X | X | X | L | L | L | L | L | L | L | L | L | | |
| | H | X | X | L | L | L | X | X | Q _{A0} | Q _{B0} | Q _{C0} | Q _{D0} | Q _{E0} | Q _{F0} | Q _{G0} | Q _{H0} | Q _{A0} Q _{H0} | | |
| Shift Right | H | L | H | L | L | ↑ | X | H | H | Q _{An} | Q _{Bn} | Q _{Cn} | Q _{Dn} | Q _{En} | Q _{Fn} | Q _{Gn} | H Q _{Gn} | | |
| | H | L | H | L | L | ↑ | X | L | L | Q _{An} | Q _{Bn} | Q _{Cn} | Q _{Dn} | Q _{En} | Q _{Fn} | Q _{Gn} | L Q _{Gn} | | |
| Shift Left | H | H | L | L | L | ↑ | H | X | Q _{Bn} | Q _{Cn} | Q _{Dn} | Q _{En} | Q _{Fn} | Q _{Gn} | Q _{Hn} | H | Q _{Bn} H | | |
| | H | H | L | L | L | ↑ | L | X | Q _{Bn} | Q _{Cn} | Q _{Dn} | Q _{En} | Q _{Fn} | Q _{Gn} | Q _{Hn} | L | Q _{Bn} L | | |
| Load | H | H | H | X | X | ↑ | X | X | a | b | c | d | e | f | g | h | a h | | |

a...h = The level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

H = HIGH Level

L = LOW Logic Level

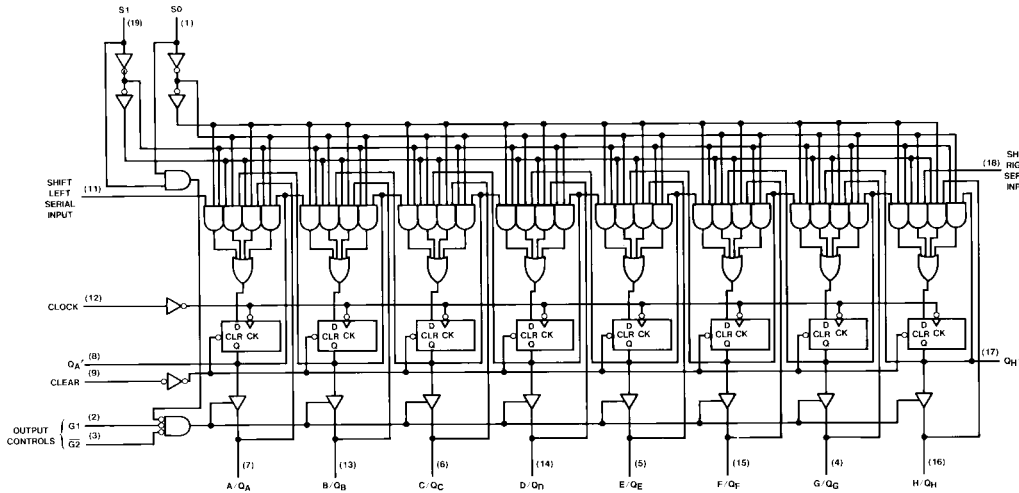
X = Either LOW or HIGH Logic Level

Q_{A0}...Q_{H0} = The output logic level of Q_x before the indicated input conditions were established.

Q_{An}...Q_{Hn} = The output logic level before the active transition (↑) of the clock input.

Note 1: When one or both output controls are HIGH the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected

Logic Diagram



Absolute Maximum Ratings(Note 2)

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 5.5V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|------------------|---|-----------------|-----------------|------|-------|
| V _{CC} | Supply Voltage | 4.75 | 5 | 5.25 | V |
| V _{IH} | HIGH Level Input Voltage | 2 | | | V |
| V _{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I _{OH} | HIGH Level Output Current (Q _A thru Q _H) | | | -6.5 | mA |
| | HIGH Level Output Current (Q _{A'} , Q _{H'}) | | | -0.5 | |
| I _{OL} | LOW Level Output Current (Q _A thru Q _H) | | | 20 | mA |
| | HIGH Level Output Current (Q _{A'} , Q _{H'}) | | | 6 | |
| f _{CLK} | Clock Frequency (Note 3) | 0 | 70 | 50 | MHz |
| f _{CLK} | Clock Frequency (Note 4) | 0 | 60 | 40 | MHz |
| t _W | Pulse Width (Note 5) | Clock HIGH | 10 | | ns |
| | | Clock LOW | 10 | | |
| | | Clear LOW | 10 | | |
| t _{SU} | Setup Time (Note 6)(Note 5)(Note 7) | Select | 15 [↑] | | ns |
| | | Data HIGH | 7 [↑] | | |
| | | Data LOW | 5 [↑] | | |
| t _H | Hold Time (Note 5)(Note 7) | 5 [↑] | | | ns |
| t _{REL} | Clear Release Time (Note 5) | 10 [↑] | | | ns |
| T _A | Free Air Operating Temperature | 0 | | 70 | °C |

Note 3: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 5: T_A = 25°C and V_{CC} = 5V.

Note 6: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 7: Data includes the two serial inputs and the eight input/output data lines.

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 8) | Max | Units | |
|-----------|--|--|---|-----------------|------------|---------------|---------------|
| V_I | Input Clamp Voltage | $V_{CC} = \text{Min}$, $I_I = -18 \text{ mA}$ | | | -1.2 | V | |
| V_{OH} | HIGH Level Output Voltage | $V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$ | Q_A thru Q_H $Q_{A'}$, $Q_{H'}$ | 2.4 3.2 | 3.2 3.4 | V | |
| | LOW Level Output Voltage | $V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$ | | | 0.5 | V | |
| I_I | Input Current @ Max Input Voltage | $V_{CC} = \text{Max}$, $V_I = 5.5 \text{ V}$ | | | 1 | mA | |
| I_{IH} | HIGH Level Input Current | $V_{CC} = \text{Max}$ $V_I = 2.7 \text{ V}$ | A thru H, S0, S1 | | | 100 | μA |
| | | | Any Other | | | 50 | |
| I_{IL} | LOW Level Input Current | $V_{CC} = \text{Max}$ $V_I = 0.5 \text{ V}$ | Clock, Clear | | | -2 | mA |
| | | | S0, S1 | | | -0.5 | |
| | | | Other | | | -0.25 | |
| I_{OZH} | Off-State Output Current with HIGH Level Output Voltage Applied (Q_A thru Q_H) | $V_{CC} = \text{Max}$, $V_O = 2.4 \text{ V}$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$ | | | 100 | μA | |
| I_{OZL} | Off-State Output Current with LOW Level Output Voltage Applied (Q_A thru Q_H) | $V_{CC} = \text{Max}$, $V_O = 0.5 \text{ V}$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$ | | | -250 | μA | |
| I_{OS} | Short Circuit Output Current (Q_A thru Q_H) | $V_{CC} = \text{Max}$ (Note 10) | -40 | | -100 | mA | |
| | Short Circuit Output Current ($Q_{A'}$, $Q_{H'}$) | $V_{CC} = \text{Max}$ (Note 10) | -20 | | -100 | | |
| I_{CC} | Supply Current | $V_{CC} = \text{Max}$ | | 140 | 225 | mA | |

Note 8: $T_A = 25^\circ\text{C}$ and $V_{CC} = 5 \text{ V}$.

Note 9: All typicals are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

Note 10: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

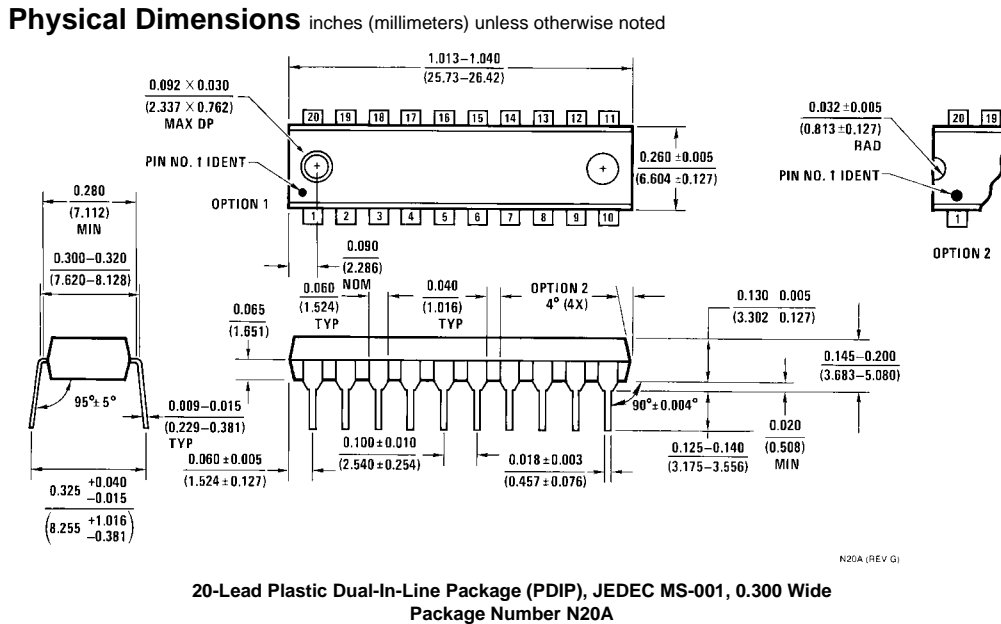
at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $R_L = 280\Omega$ (Note 12) | | | | Units |
|-----------|--|---|-----------------------------|-----|-----------------------|-----|-------|
| | | | $C_L = 15 \text{ pF}$ | | $C_L = 50 \text{ pF}$ | | |
| | | | Min | Max | Min | Max | |
| f_{MAX} | Maximum Clock Frequency | (Note 13) | 50 | | 40 | | MHz |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output (Note 12) | Clock to $Q_{A'}$ or $Q_{H'}$ | | 20 | | 22 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output (Note 12) | Clock to Q_A or Q_H | | 20 | | 23 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Clock to Q_A thru Q_H | | | | 21 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Clock to Q_A thru Q_H | | | | 21 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output (Note 12) | Clear to $Q_{A'}$ or $Q_{H'}$ | | 21 | | 24 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Clear to Q_A thru Q_H | | | | 24 | ns |
| t_{PZH} | Output Enable Time to HIGH Level Output | $\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H | | | | 18 | ns |
| t_{PZL} | Output Enable Time to LOW Level Output | $\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H | | | | 18 | ns |
| t_{PHZ} | Output Disable Time to HIGH Level Output (Note 11) | $\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H | | 12 | | | ns |
| t_{PLZ} | Output Disable Time to LOW Level Output (Note 11) | $\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H | | 12 | | | ns |

Note 11: $C_L = 5 \text{ pF}$.

Note 12: $R_L = 1 \text{ K}\Omega$ for delays measured to $Q_{A'}$ and $Q_{H'}$.

Note 13: For testing f_{MAX} all outputs are loaded simultaneously.



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