

**FAIRCHILD**  
SEMICONDUCTOR™

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## DM74S280 9-Bit Parity Generator/Checker

### General Description

These universal, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry, and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is easily expanded by cascading.

The DM74S280 can be used to upgrade the performance of most systems utilizing the DM74180 parity generator/checker. Although the DM74S280 is implemented without expander inputs, the corresponding function is provided by the availability of all input at pin 4, and no internal connection at pin 3. This permits the DM74S280 to be substituted for the 180 in existing designs to produce an identical function, even if DM74S280's are mixed with existing 180's.

Input buffers are provided so that each input represents only one normal 74S load, and full fan-out to 10 normal Series 74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normal Series 74S loads is provided at high logic levels, to facilitate connection of unused inputs to used inputs.

### Features

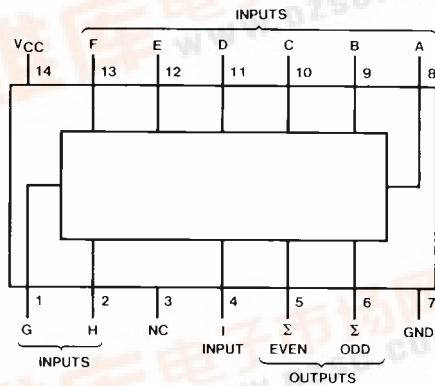
- Generates either odd or even parity for nine data lines
- Cascadable for N-bits
- Can be used to upgrade existing systems using MSI parity circuits
- Typical data-to-output delay—14 ns

### Ordering Code:

Order Number	Package Number	Package Description
DM74S280M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74S280N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



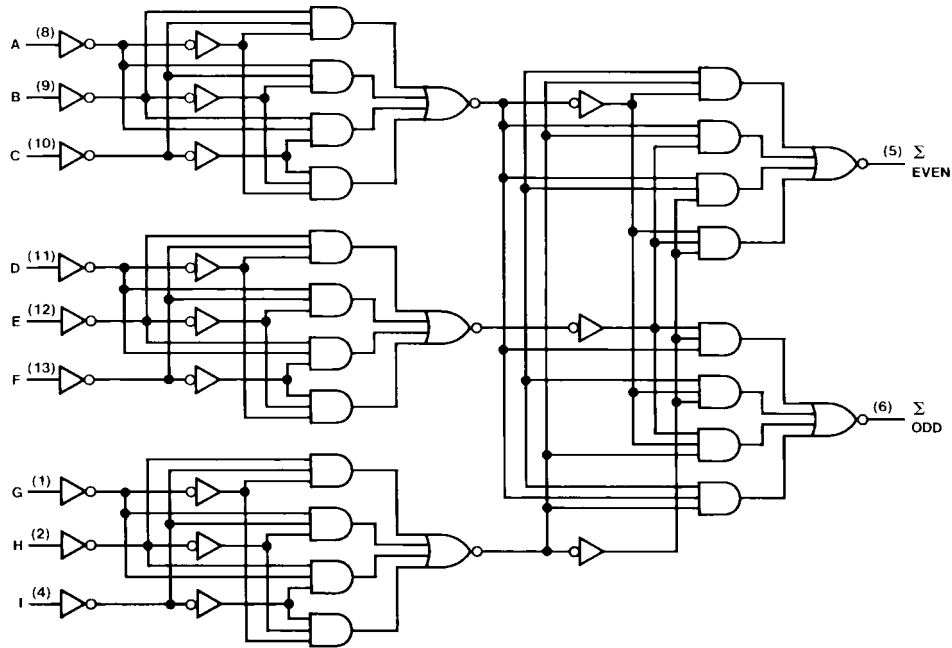
### Function Table

Number of Inputs (A Thru I) that are HIGH	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

DM74S280 9-Bit Parity Generator/Checker



### Logic Diagram



### Typical Applications

Three DM74S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 25 ns. (See Figure 1.)

Longer word lengths can be implemented by cascading DM74S280's. As shown in Figure 2, parity can be generated for word lengths up to 81 bits in typically 25 ns.

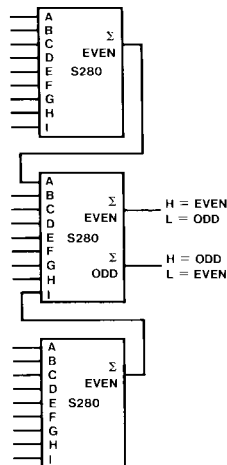


FIGURE 1. 25-Line Parity/Generator Checker

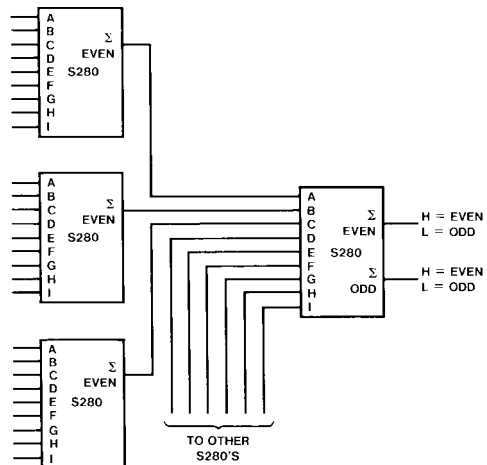


FIGURE 2. 81-Line Parity/Generator Checker

**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
I <sub>OH</sub>	HIGH Level Output Current			-1	mA
I <sub>OL</sub>	LOW Level Output Current			20	mA
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>	HIGH Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.7	3.4		V
V <sub>OL</sub>	LOW Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max			0.5	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	HIGH Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			50	μA
I <sub>IL</sub>	LOW Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.5V			-2	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 3)	-40		-100	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> Max (Note 4)		67	105	mA

**Note 2:** All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

**Note 3:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 4:** I<sub>CC</sub> is measured with all inputs grounded and all outputs OPEN.

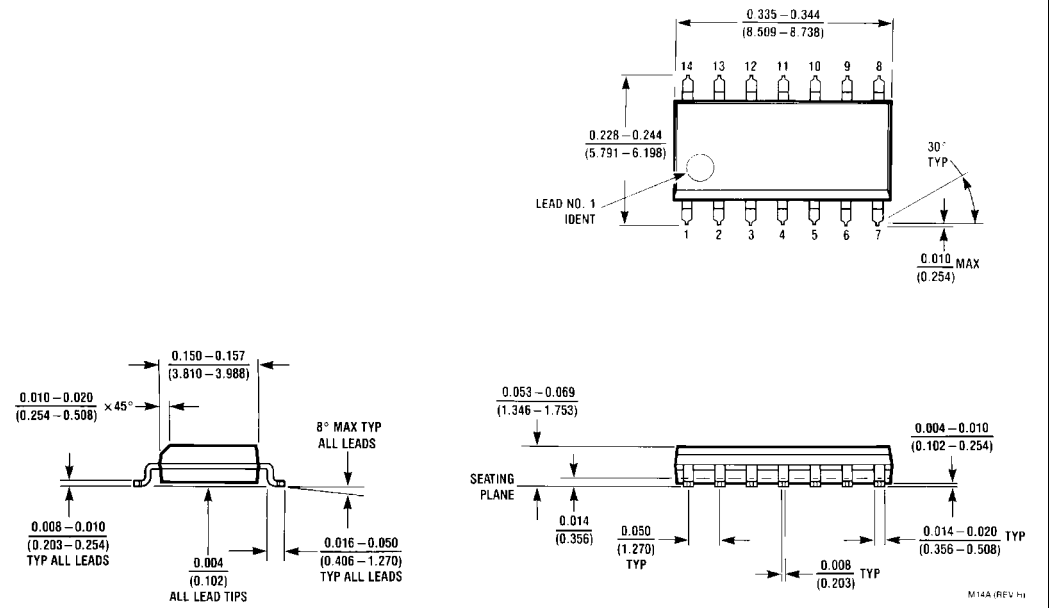
**Switching Characteristics**

at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C

Symbol	Parameter	From (Input) To (Output)	R <sub>L</sub> = 280Ω C <sub>L</sub> = 15 pF		R <sub>L</sub> = 280Ω C <sub>L</sub> = 50 pF		Units
			Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Data to Σ Even		21		24	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	Data to Σ Even		18		21	ns
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Data to Σ Odd		21		24	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	Data to Σ Odd		18		21	ns

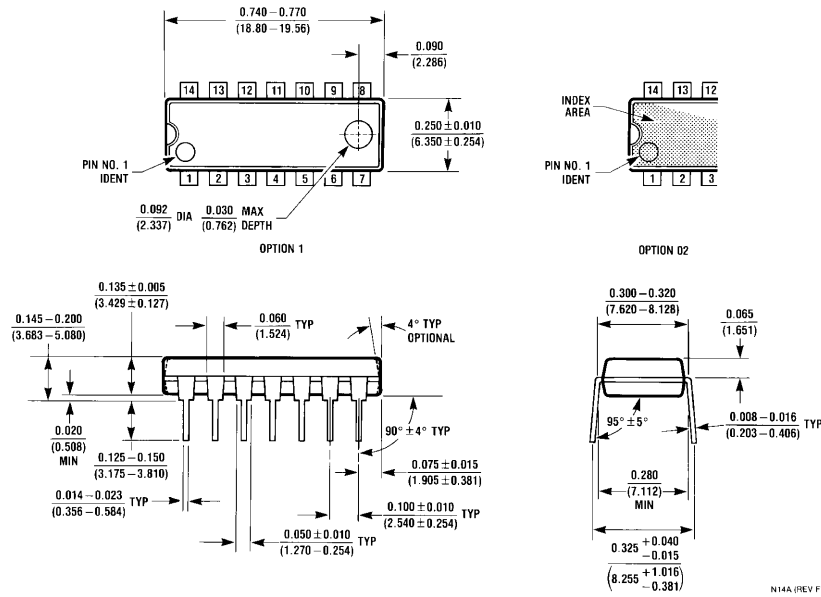
DM74S280

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A**

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