



August 1986  
Revised March 2000

## DM74LS74A

### Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

#### General Description

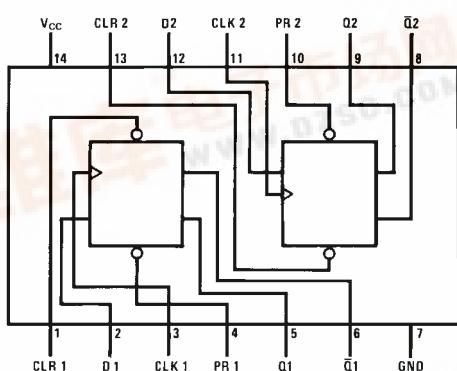
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is LOW or HIGH without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

#### Ordering Code:

Order Number	Package Number	Package Description
DM74LS74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS85ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram



#### Function Table

PR	CLR	CLK	D	Inputs		Outputs	
				Q	$\bar{Q}$	Q	$\bar{Q}$
L	H	X	X	H	L		
H	L	X	X	L	H		
L	L	X	X	H (Note 1)		H (Note 1)	
H	H	$\uparrow$	H			H	L
H	H	$\uparrow$	L	L	H		
H	H	L	X	$Q_0$	$\bar{Q}_0$		

H = HIGH Logic Level

X = Either LOW or HIGH Logic Level

L = LOW Logic Level

$\uparrow$  = Positive-going Transition

$Q_0$  = The output logic level of Q before the indicated input conditions were established.

**Note 1:** This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

## Absolute Maximum Ratings<sup>(Note 2)</sup>

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			-0.4	mA
$I_{OL}$	LOW Level Output Current			8	mA
$f_{CLK}$	Clock Frequency (Note 3)	0		25	MHz
$f_{CLK}$	Clock Frequency (Note 4)	0		20	MHz
$t_W$	Pulse Width (Note 3)	Clock HIGH	18		ns
		Preset LOW	15		
		Clear LOW	15		
$t_W$	Pulse Width (Note 4)	Clock HIGH	25		ns
		Preset LOW	20		
		Clear LOW	20		
$t_{SU}$	Setup Time (Note 3)(Note 5)	20 $\uparrow$			ns
$t_{SU}$	Setup Time (Note 4)(Note 5)	25 $\uparrow$			ns
$t_H$	Hold Time (Note 5)(Note 6)	0 $\uparrow$			ns
$T_A$	Free Air Operating Temperature	0		70	°C

**Note 3:**  $C_L = 15 \text{ pF}$ ,  $R_L = 2 \text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ , and  $V_{CC} = 5\text{V}$ .

**Note 4:**  $C_L = 50 \text{ pF}$ ,  $R_L = 2 \text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ , and  $V_{CC} = 5\text{V}$ .

**Note 5:** The symbol ( $\uparrow$ ) indicates the rising edge of the clock pulse is used for reference.

**Note 6:**  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 7)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -18 \text{ mA}$			-1.5	V
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$	2.7	3.4		V
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = \text{Max}$ $V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$ $I_{OL} = 4 \text{ mA}$ , $V_{CC} = \text{Min}$		0.35	0.5	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ $V_I = 7V$	Data		0.1	mA
			Clock		0.1	
			Preset		0.2	
			Clear		0.2	
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7V$	Data		20	$\mu\text{A}$
			Clock		20	
			Clear		40	
			Preset		40	
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4V$	Data		-0.4	mA
			Clock		-0.4	
			Preset		-0.8	
			Clear		-0.8	
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 8)	-20		-100	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 9)		4	8	mA

Note 7: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ\text{C}$ .

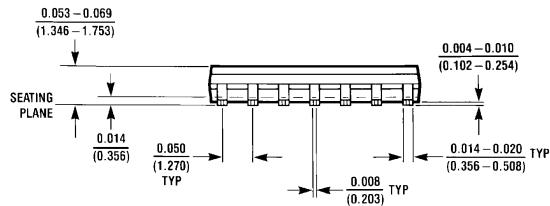
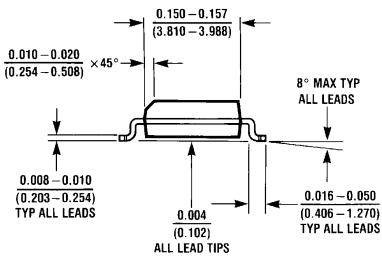
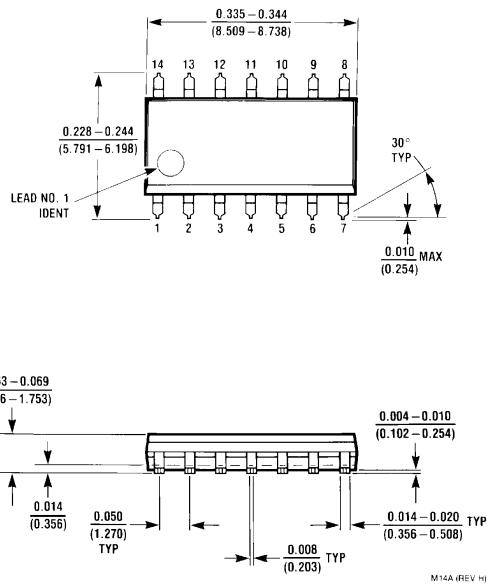
Note 8: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where  $V_O = 2.125V$  with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 9: With all outputs OPEN,  $I_{CC}$  is measured with CLOCK grounded after setting the Q and  $\bar{Q}$  outputs HIGH in turn.

## Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ\text{C}$

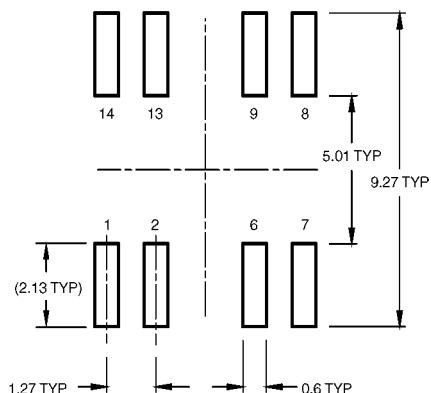
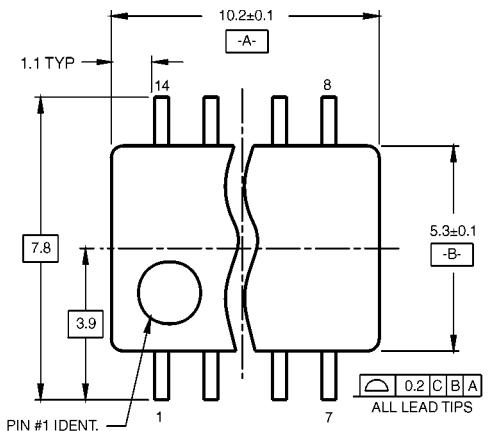
Symbol	Parameter	From (Input) To (Output)	$R_L = 2 \text{ k}\Omega$				Units	
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$			
			Min	Max	Min	Max		
$f_{MAX}$	Maximum Clock Frequency		25		20		MHz	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\bar{Q}$		25		35	ns	
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\bar{Q}$		30		35	ns	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25		35	ns	
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\bar{Q}$		30		35	ns	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\bar{Q}$		25		35	ns	
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		30		35	ns	

**Physical Dimensions** inches (millimeters) unless otherwise noted

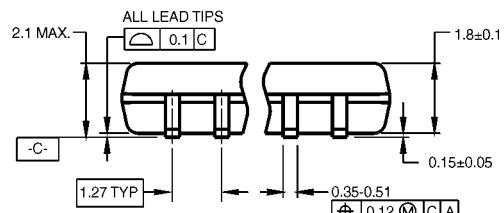
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow  
Package Number M14A

M14A (REV H)

## **Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



#### LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

## NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

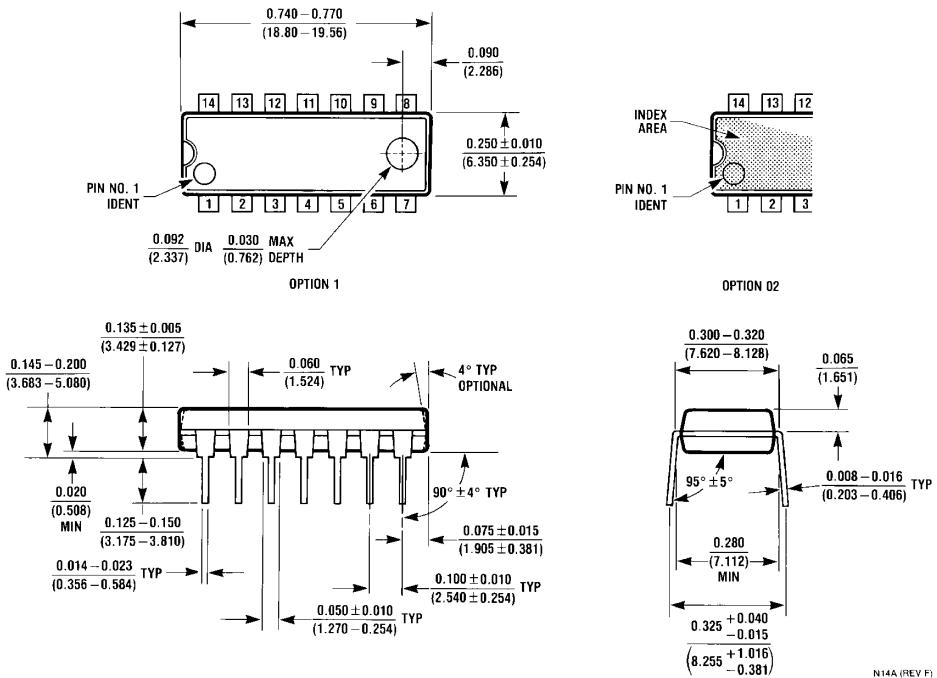
M14DRevB1

The diagram shows a cross-section of a stepped component. A horizontal dashed line represents the GAGE PLANE. A horizontal solid line represents the SEATING PLANE. The top surface has a vertical height of 0.60 ± 0.15. The top surface is labeled with a dimension of 1.25. A vertical dimension of 0.25 is shown from the seating plane to the top of the upper step. A note indicates a slope of 0°-8° TYP for the top surface. A note indicates a slope of 7° TYP for the transition between the two steps. Arrows point to the GAGE PLANE, SEATING PLANE, and the 0.25 dimension.

**DETAIL A**

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)