

**FAIRCHILD**  
SEMICONDUCTOR™

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## DM74S174 • DM74S175 Hex/Quad D Flip-Flop with Clear

### General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (DM74S175) versions feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect at the output.

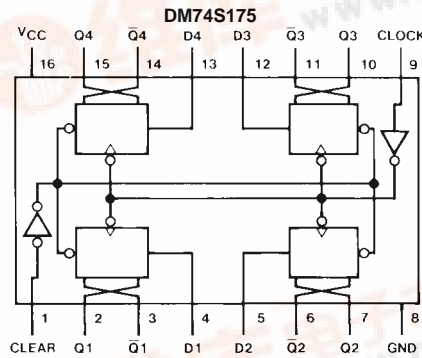
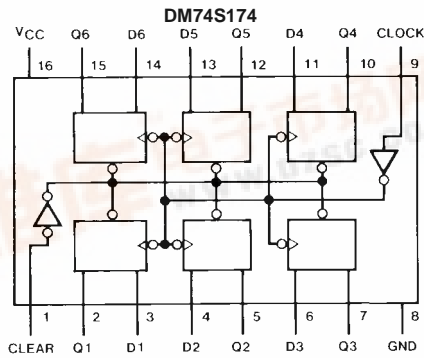
### Features

- DM74S174 contain six flip-flops with single-rail outputs.
- DM74S175 contain four flip-flops with double-rail outputs.
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 110 MHz
- Typical power dissipation per flip-flop 75mW

### Ordering Code:

Order Number	Package Number	Package Description
DM74S174N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74S175N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

### Connection Diagrams



DM74S174 • DM74S175 Hex/Quad D Flip-Flop with Clear

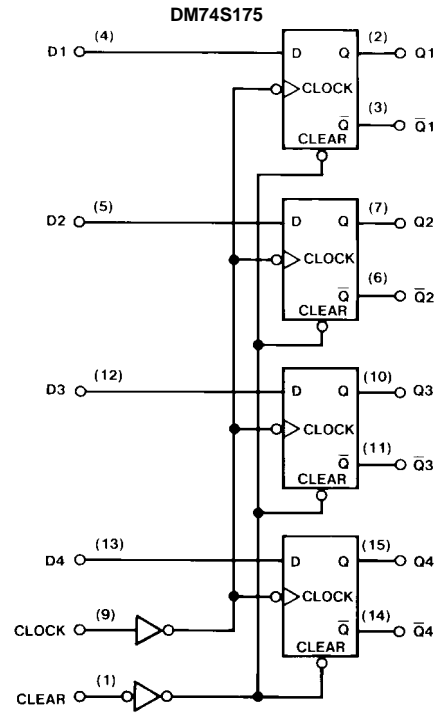
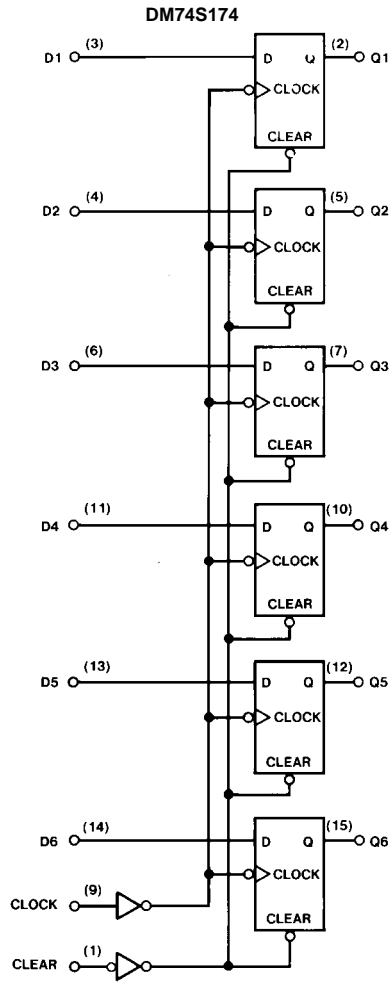


### Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	Q̄ (Note 1)
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

H = HIGH Level (steady state)  
 L = LOW Level (steady state)  
 X = Don't Care  
 ↑ = Transition from LOW-to-HIGH level  
 Q<sub>0</sub> = The level of Q before the indicated steady-state input conditions were established.  
**Note 1:** DM74S175 only.

### Logic Diagrams



**Absolute Maximum Ratings**(Note 2)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
I <sub>OH</sub>	HIGH Level Output Current			-1	mA
I <sub>OL</sub>	LOW Level Output Current			20	mA
f <sub>CLK</sub>	Clock Frequency (Note 3)	0	110	75	MHz
f <sub>CLK</sub>	Clock Frequency (Note 4)	0	90	65	MHz
t <sub>w</sub>	Pulse Width (Note 3)	Clock	7		ns
		Clear	10		
	Pulse Width (Note 4)	Clock	9		
		Clear	12		
t <sub>SU</sub>	Data Setup Time (Note 3)	5		ns	
	Data Setup Time (Note 4)	7			
t <sub>H</sub>	Data Hold Time (Note 3)	3		ns	
	Data Hold Time (Note 4)	5			
t <sub>REL</sub>	Clear Release Time (Note 3)	5		ns	
	Clear Release Time (Note 4)	7			
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

**Note 3:** C<sub>L</sub> = 15 pF, R<sub>L</sub> = 280Ω, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

**Note 4:** C<sub>L</sub> = 50 pF, R<sub>L</sub> = 280Ω, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	2.7	3.4		V
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$			0.5	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7 \text{ V}$			50	$\mu\text{A}$
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}, V_I = 0.5 \text{ V}$			-2	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 6)	-40		-100	mA
$I_{CC}$	Supply Current (DM74S174)	$V_{CC} = \text{Max}$ (Note 7)		90	144	mA
$I_{CC}$	Supply Current (DM74S175)	$V_{CC} = \text{Max}$ (Note 7)		60	96	mA

**Note 5:** All typicals are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

**Note 6:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

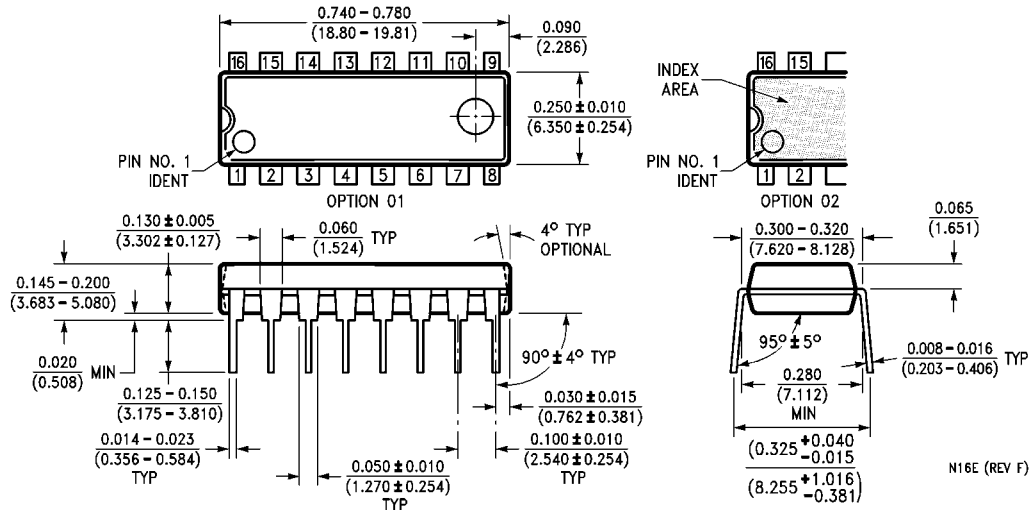
**Note 7:** With all outputs OPEN and 4.5V applied to all DATA and CLEAR inputs,  $I_{CC}$  is measured after a momentary ground, then 4.5V applied to the CLOCK input.

## Switching Characteristics

at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
			Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency		75		65		MHz
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Output		12		15	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Output		17		21	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output (DM74S175 Only)	Clear to $\bar{Q}$		15		18	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		22		23	ns

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E**

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