# NCP5209

*Product Preview*

## 4-In-1 PWM Buck and Tri-Linear DDR Power Controller

ON Semiconductor®

http://onsemi.com

The NCP5209 4−In−1 PWM Buck and Tri−Linear Power Controller is a complete ACPI compliant power solution for MCH and DDR memory. This IC combines the high efficiency of a PWM controller for the VDDQ supply with the simplicity of linear regulator for the VTT termination voltage as well as the MCH core supply voltage.

This IC contains a synchronous PWM buck controller for driving two external NFETs to form the DDR memory supply voltage (VDDQ). The DDR memory termination regulator (VTT) is designed to track at the half of reference voltage while sourcing and sinking current. The two linear regulator controllers driving two external NFETs are cascaded to produce the MCH core voltage (VMCH).

Protective features include, soft−start circuitry, under−voltage monitoring of 5VDUAL, 5VATX and 12VATX, and thermal shutdown. The IC is packaged in a QFN−20.

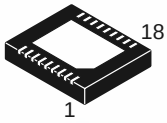
### Features

- Synchronous PWM Buck Controller for VDDQ
- Integrated Power FETs with VTT Regulator Sourcing/Sinking up to 1.8 A
- Two Linear Regulator Drivers for VMCH
- All External Power MOSFETs are N−Channel
- Adjustable VDDQ and VMCH by External Dividers
- VTT Tracks at Half the Reference Voltage or can be Adjusted Externally
- Fixed Switching Frequency of 250 kHz for DDQ Regulator in Normal Mode Doubled switching frequency (500 kHz) for DDQ Regulator in Standby Mode
- Soft−Start Protection for all Regulators
- Under−Voltage Monitoring of Supply Voltages
- Over−Current Protection for DDQ and VTT Regulators
- Fully Complies with ACPI Power Sequencing Specifications
- Protects against Reverse DIMM Insertion
- Thermal Shutdown
- Housed in QFN−20

### Applications

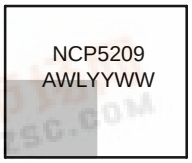
- DDR I and DDR II Memory and MCH Power Supply

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



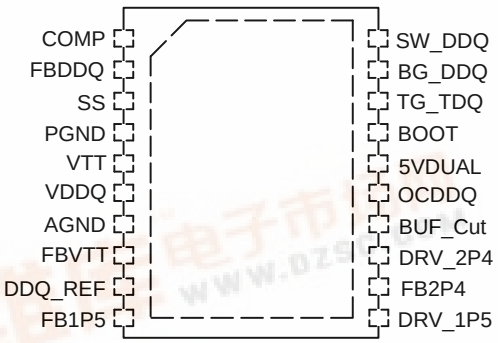

**20−LEAD QFN**
**MN SUFFIX**
**CASE 505**

**MARKING DIAGRAM**




NCP5209 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

**PIN CONNECTIONS**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NCP5209MN | 20−Lead QFN* | Rail |
| NCP5209MNR2 | 20−Lead QFN* | Tape and Reel |

*5 x 6 mm

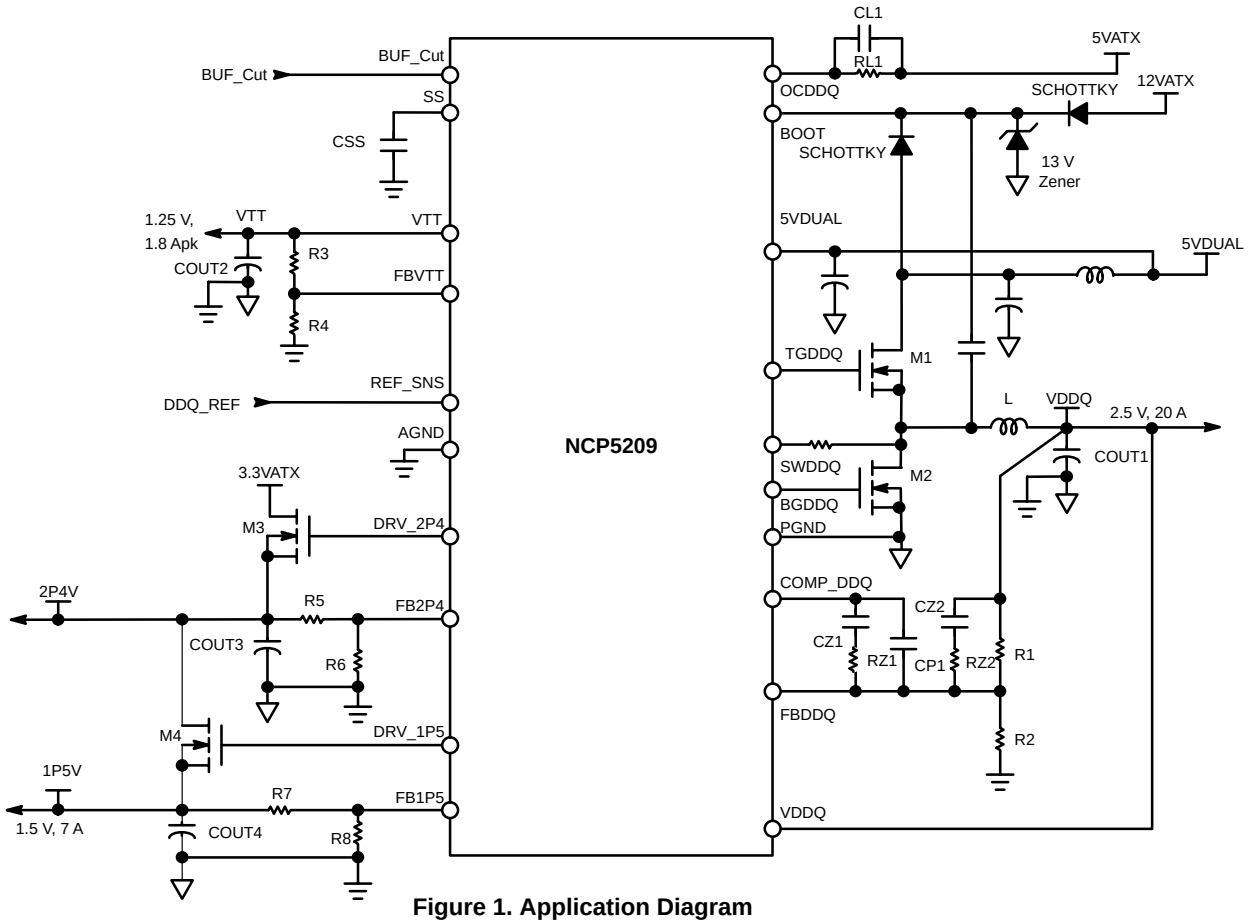



**Figure 1. Application Diagram**

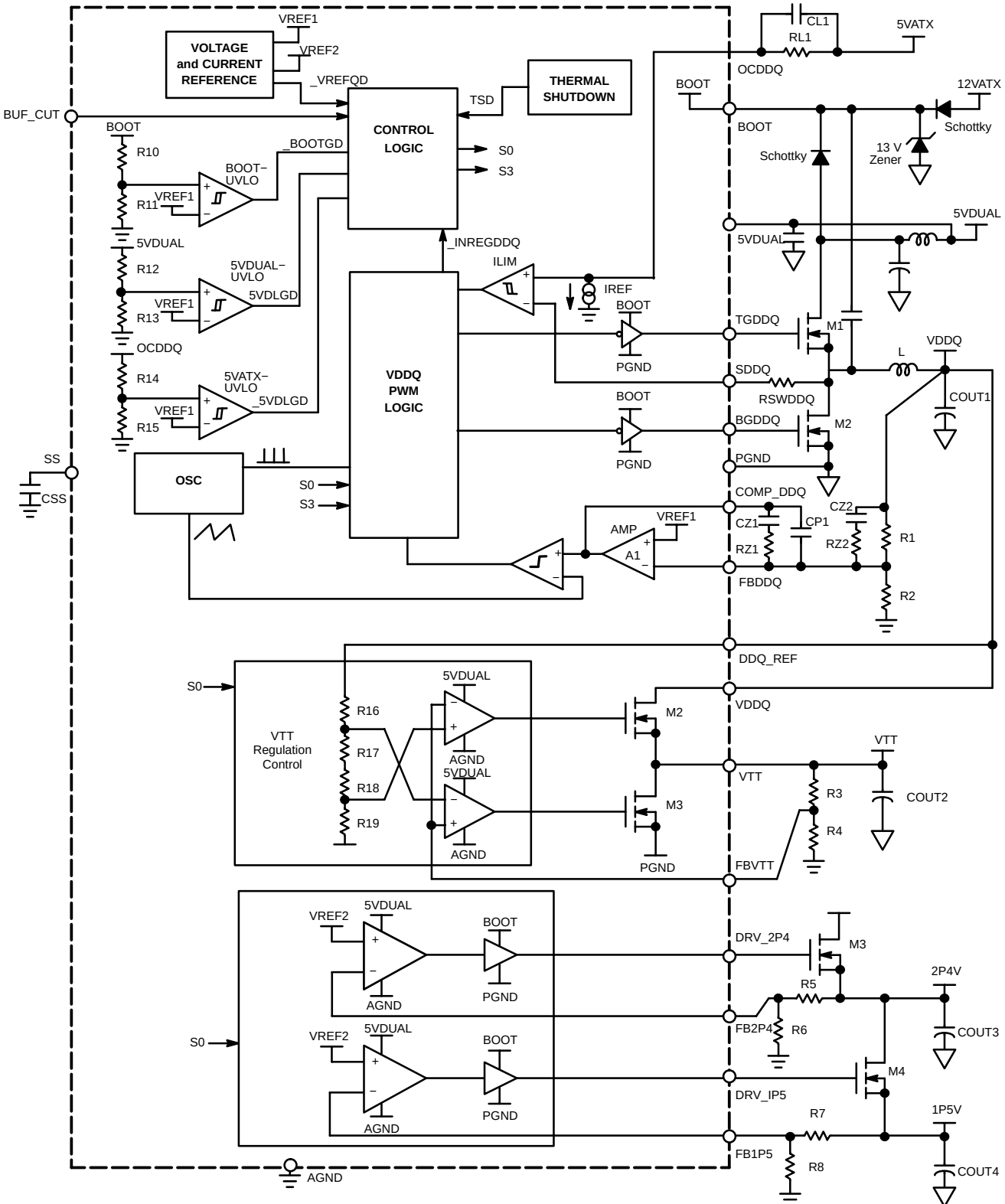



**Figure 2. Internal Block Diagram.**

## PIN DESCRIPTION

| Pin | Symbol | Descriptions |
|---|---|---|
| 1 | COMP | VDDQ Error Amplifier Compensation Node. |
| 2 | FBDDQ | VDDQ Regulator Feedback Pin for Closed Loop Regulation. |
| 3 | SS | Soft Start Capacitor Connection to Ground. |
| 4 | PGND | Power Ground |
| 5 | VTT | VTT Regulator Output |
| 6 | VDDQ | Power Input for VTT Linear Regulator |
| 7 | AGND | Analog Ground Connection and Remote Ground Sense. |
| 8 | FBVTT | VTT Linear Regulator Feedback pin for Closed Loop Regulation. |
| 9 | DDQ_REF | VDDQ Reference Voltage Input of VTT Regulator. |
| 10 | FB1P5 | 2nd Linear Regulator Feedback Pin for Closed Loop Regulation. |
| 11 | DRV_1P5 | 2nd Linear Regulator Gate Driver Output for N−Channel Power FET. |
| 12 | FB2P4 | 1st Linear Regulator Feedback Pin for Closed Loop Regulation. |
| 13 | DRV_2P4 | 1st Linear Regulator Gate Driver Output for N−Channel Power FET. |
| 14 | BUF_CUT | Active High Control Signal to Activate S3 Sleep State. |
| 15 | OCDDQ | Over−current Sense and Program Input for the VDDQ High Side FET. |
| 16 | 5VDUAL | 5 V Dual Supply Input |
| 17 | BOOT | Gate Driver Input Supply. A Boost Capacitor is Connected between SWDDQ and BOOT. |
| 18 | TGDDQ | Gate Driver Output for VDDQ Regulator High Side N−Channel Power FET. |
| 19 | BGDDQ | Gate Driver Output for VDDQ Regulator Low Side N−Channel Power FET. |
| 20 | SWDDQ | DDQ Regulator Current Limit Sense Input. A Protection Resistor Should be Connected between the Inductor Driven Node and SWDDQ. |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage (Pin 16) to AGND (Pin 7) | 5VDUAL | −0.3, 6.0 | V |
| Gate Drive Voltage (Pin 11, 13, 17−19) to AGND (PIN 7) | $V_{CC}$, $V_g$ | −0.3, 14 | V |
| Input / Output Pins to AGND (Pin 7)<br>Pin 1−6, 8−10, 12, 14−15, 20 | $V_{IO}$ | −0.3, 6.0 | V |
| Thermal Characteristics<br>QFN−20 Plastic Package<br>Thermal Resistance Junction−to−Air | $R_{\theta JA\_Q}$ | 68 | °C/W |
| Operating Junction Temperature Range | $T_J$ | 0 to + 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | 0 to + 70 | °C |
| Storage Temperature Range | $T_{stg}$ | − 55 to +150 | °C |
| Moisture Sensitivity Level | MSL | | |

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ≤ 2.0 kV per JEDEC standard: JESD22–A114.
   Machine Model (MM) ≤ 200 V per JEDEC standard: JESD22–A115.
2. Latch–up Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78.

## ELECTRICAL CHARACTERISTICS

(5VDUAL = 5 V, BOOT = 12 V, 5VATX = 5 V, DDQ_REF = 2.5 V, $T_A$ = 0 to 70°C, L = 1.7 μH, COUT1 = 3770 μF, COUT2 = 470 μF, COUT3 = 680 μF, COUT4 = 3300 μF, CSS = 33 nF, RL1 = 50 kΩ, R1 = 2.2 kΩ, R2 = 2 kΩ, R3 = 0 Ω, R4 = 1 kΩ, R5 = 10 kΩ, R6 = 5 kΩ, R7 = 6.8 Ω, R8 = 7.5 kΩ, RSWDDQ = 1 kΩ, RZ1 = 20 kΩ, RZ2 = 8 Ω, CP1 = 10 nF, CZ1 = 6.8 nF, CZ2 = 100 nF, for min/max values unless otherwise noted.)

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | | |
| 5VDUAL Operating Voltage | | V5VDUAL | 4.5 | 5.0 | 5.5 | V |
| OCDDQ Operating Voltage | | VOCDDQ | 4.5 | 5.0 | 5.5 | V |
| BOOT Operating Voltage | | VBOOT | | 12.0 | 13.2 | V |
| **Supply Current** | | | | | | |
| S0 mode Supply Current from 5VDUAL | BUF_CUT = LOW, BOOT = 12 V, 5VATX = 5 V | I5VDL_S0 | | | 7 | mA |
| S3 mode Supply Current from 5VDUAL | BUF_CUT = HIGH, 5VATX = 0 V | I5VDL_S3 | | | 5 | mA |
| S5 mode Supply Current from 5VDUAL | BUF_CUT = LOW, 5VATX = 0 V | I5VDL_S5 | | | 1 | mA |
| S0 mode Supply Current from BOOT | BUF_CUT = LOW, BOOT=12 V, 5VATX = 5 V, TGDDQ, BGDDQ, DRV_2P4 and DRV_1P5 Open | IBOOT_S0 | | | 40 | mA |
| S3 mode Supply Current from BOOT | BUF_CUT = HIGH, 5VATX=0 V, TGDDQ, BGDDQ, DRV_2P4 and DRV_1P5 Open | IBOOT_S3 | | | 10 | mA |
| **Under−Voltage−Monitor** | | | | | | |
| 5VDUAL UVLO Upper Threshold | | V5VDLUV+ | | | 4.4 | V |
| 5VDUAL UVLO Hysteresis | | V5VDLhys | | 300 | | mV |
| BOOT UVLO Upper Threshold | | VBOOTUV+ | | | 10.2 | V |
| BOOT UVLO Hysteresis | | VBOOThys | | 1.0 | | V |
| OCDDQ UVLO Upper Threshold | | OCDDQUV+ | | | 1.25 | V |
| OCDDQ UVLO Hysteresis | | OCDDQhys | | 200 | | mV |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown | | Tsd | | 140 | | °C |
| Thermal Shutdown Hysteresis | | Tsdhys | | 25 | | °C |
| **DDQ Switching Regulator** | | | | | | |
| FBDDQ Feedback Voltage, Control Loop in Regulation | $T_A$ = 25°C<br>$T_A$ = 0 to 70°C | VFBQ | 1.178<br>1.166 | 1.190<br>1.190 | 1.202<br>1.214 | V |
| Feedback Input Current | V(FBDDQ) = 1.190 V | IDDQfb | | | 1 | μA |
| Oscillator Frequency in S0 Mode | | FDDQS0 | 225 | 250 | 275 | kHz |
| Oscillator Frequency in S3 Mode | | FDDQS3 | 450 | 500 | 550 | kHz |
| OCDDQ pin Current Sink | V(OCDDQ) = 3 V | IOCDDQ | 28 | 40 | 52 | μA |
| Current Limit Blanking Time in S0 Mode | | TDDQbk | 400 | | | ns |
| Minimum Duty Cycle in S0 Mode | | DS0min | 0 | | | % |
| Maximum Duty Cycle in S0 Mode | | DS0max | | | 100 | % |
| **DDQ Switching Regulator** | | | | | | |
| Minimum Duty Cycle in S3 Mode | | DS3min | 0 | | | % |
| Maximum Duty Cycle in S3 Mode | | DS3max | | | 90 | % |
| Soft−Start Timing | | Tss1 | | 10 | | ms |
| **DDQ ERROR AMPLIFIER** | | | | | | |
| DC Gain | | GAINDDQ | | 70 | | dB |

## ELECTRICAL CHARACTERISTICS

(5VDUAL = 5 V, BOOT = 12 V, 5VATX = 5 V, DDQ_REF = 2.5 V, $T_A$ = 0 to 70°C, L = 1.7 μH, COUT1 = 3770 μF, COUT2 = 470 μF, COUT3 = 680 μF, COUT4 = 3300 μF, CSS = 33 nF, RL1 = 50 kΩ, R1 = 2.2 kΩ, R2 = 2 kΩ, R3 = 0 Ω, R4 = 1 kΩ, R5 = 10 kΩ, R6 = 5 kΩ, R7 = 6.8 Ω, R8 = 7.5 kΩ, RSWDDQ = 1 kΩ, RZ1 = 20 kΩ, RZ2 = 8 Ω, CP1 = 10 nF, CZ1 = 6.8 nF, CZ2 = 100 nF, for min/max values unless otherwise noted.)

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DDQ ERROR AMPLIFIER** | | | | | | |
| Gain−Bandwidth Product | COMP_DDQ = 220 nF, 1 Ω in Series | GBWDDQ | | TBD | | MHz |
| Slew Rate | COMP_DDQ = 10 pF | SRDDQ | | 8 | | V/μs |
| **VTT Active Termination Regulator** | | | | | | |
| VTT tracking REF_SNS/2 at S0 mode | IOUT= 0 to 1.8 A (Sink Current)<br>IOUT= 0 to –1.8 A (Source Current) | adVTTS0 | −30 | | 30 | mV |
| VTT Source Current Limit | | ILIMVTsrc | | 2.4 | | A |
| VTT Sink Current Limit | | ILIMVTsnk | | 2.4 | | A |
| DDQ_REF Input Resistance | | RDDQ_REF | | 50 | | Ω |
| **Dual Linear Regulator Controller** | | | | | | |
| 1st Regulator Feedback Voltage, Control Loop in Regulation | $T_A$ = 0°C to 70°C | VFB2P4 | 0.784 | 0.800 | 0.816 | V |
| 1st Regulator Feedback Input Current | | IFB2P4 | | | 1 | μA |
| 1st Regulator DC Gain | | GAIN2P4 | | 66 | | dB |
| 2nd Regulator Feedback Voltage, Control Loop in Regulation | $T_A$ = 0°C to 70°C | VFB1P5 | 0.784 | 0.800 | 0.816 | V |
| 2nd Regulator Feedback Input Current | | IFB1P5 | | | 1 | μA |
| 2nd Regulator DC Gain | | GAIN1P5 | | 66 | | dB |
| Internal Soft−Start Timing | | Tss2 | | 1.5 | | ms |
| **Control Section** | | | | | | |
| BUF_CUT Input Logic HIGH | | Logic_H | 2.0 | | | V |
| BUF_CUT Input Logic LOW | | Logic_L | | | 0.8 | V |
| BUF_CUT Input Current | | ILogic | | | 1 | μA |
| **Gate Drivers** | | | | | | |
| TGDDQ Gate Pull−HIGH Resistance | BOOT = 12 V, V(TGDDQ) = 11.9 V | RH_TG | | 3.5 | | Ω |
| TGDDQ Gate Pull−LOW Resistance | BOOT = 12 V, V(TGDDQ) = 0.1 V | RL_TG | | 2.5 | | Ω |
| BGDDQ Gate Pull−HIGH Resistance | BOOT = 12 V, V(BGDDQ) = 11.9 V | RH_BG | | 3.5 | | Ω |
| BGDDQ Gate Pull−LOW Resistance | BOOT = 12 V, V(BGDDQ) = 0.1 V | RL_BG | | 1.3 | | Ω |
| DRV_2P4 Gate Pull−HIGH Voltage | BOOT = 12 V | VH2P4 | | 9.0 | | V |
| DRV_2P4 Gate Pull−LOW Voltage | BOOT = 12 V | VL2P4 | | 0.8 | | V |
| DRV_2P4 Gate Source Current | BOOT = 12 V | IH2P4 | | 10 | | mA |
| DRV_2P4 Gate Sink Current | BOOT = 12 V | IL2P4 | | 10 | | mA |
| DRV_1P5 Gate Pull−HIGH Voltage | BOOT = 12 V | VH1P5 | | 9.0 | | V |
| DRV_1P5 Gate Pull−LOW Voltage | BOOT = 12 V | VL1P5 | | 0.8 | | V |
| DRV_1P5 Gate Source Current | BOOT = 12 V | IH1P5 | | 10 | | mA |
| DRV_1P5 Gate Sink Current | BOOT = 12 V | IL1P5 | | 10 | | mA |

## DETAILED OPERATION DESCRIPTIONS

### General

The NCP5209 4−In−1 PWM Buck and Tri−Linear DDR Power Controller contains a high efficiency PWM controller, an integrated two−quadrant linear regulator and two linear regulator controllers.

The VDDQ supply is generated by a PWM controller driving two external NFETs. The VTT termination voltage is tracked by an integrated linear regulator with sourcing and sinking current capability. The dual linear controllers driving two external NFETs can either be cascaded to create the MCH core voltage or work independently to produced two regulated output voltages. All regulator outputs are adjustable.

The inclusion of soft−start, supply under−voltage monitors, over−current protection and thermal shutdown, makes this device a complete power solution for the MCH and DDR memory system. This device is packaged in QFN−20.

### ACPI Control Logic

The ACPI control logic is powered by the 5VDUAL supply input. The BUF_CUT input and the three supply voltage monitoring signals from the internal UVLOs are used to decode the operating mode in accordance with the state transition diagram shown in Figure 5. The 5VDUAL supply must come up before the other supplies.

The UVLOs monitor the motherboard supplies 5VDUAL, 12VATX and 5VATX through the 5VDUAL, BOOT and OCDDQ pins respectively. Three control signals, _5VDUALGD, _BOOTGD and _OCDDQGD, are asserted when the supply voltages are in good condition.

When the device is first powered up, it is in S5 shutdown mode to minimize the power consumption. When all three supplies are good and BUF_CUT is LOW the device enters S0 normal operating mode, in which, all regulators are running.

The transition of BUF_CUT from LOW to HIGH in S0 mode triggers the device into the S3 sleep mode. In S3 mode, the external 12VATX and 5VATX supplies collapse and only the VDDQ regulator is working.

During S3 mode, the transition of BUF_CUT from HIGH to LOW triggers the device back to S0 mode providing 12ATX and 5VATX are good. The IC can re−enter S5 mode from S0 mode by removing one of the supplies. Transitions from S3 to S5 or vice versa are not allowed. A timing diagram is shown in Figure 4.

Table 1 summarizes the operating states of all regulators and the conditions of the output pins.

### S5−To−S0 Mode Power Up Sequence

An internal bandgap reference is generated whenever 5VDUAL exceeds 2.7 V. Once this bandgap reference is in regulation, an internal signal _VREFGD is asserted to wake up the ACPI logic.

The assertion of VREFGD enables the ACPI control logic. Once the ACPI control is activated, the power up sequence starts by waking up the 5VDUAL voltage monitor block and reference current generator first. After 5VDUAL is within the preset level, the BOOT and OCDDQ under voltage monitor blocks are enabled to detect the presence of the 12VATX and 5VATX supplies. When the three supplies are in regulation and BUFCUT is LOW the device enters S0 mode by activating the soft−start of VDDQ switching regulator.

After the VDDQ regulator is in regulation and the soft−start interval is completed, the _INREGDDQ signal is asserted to wake up the VTT regulator and the dual linear controllers.

**Table 1. Mode, Operation and Output Pin Condition**

| MODE | OPERATING CONDITIONS | | | OUTPUT PIN CONDITIONS | | | |
|---|---|---|---|---|---|---|---|
| | DDQ | VTT | Dual Linear | TGDDQ | BGDDQ | DRV_2P4 | DRV_1P5 |
| S0 | Normal | Normal | Normal | Normal | Normal | Normal | Normal |
| S3 | Standby | H−Z | H−Z | Standby | Standby | Low | Low |
| S5 | H−Z | H−Z | H−Z | Low | Low | Low | Low |

### VDDQ Switching Regulator

The VDDQ regulator in S0 mode is a synchronous buck controller that drives two external power NFETs to supply up to 25 A. It employs the voltage mode fixed frequency PWM control scheme with external compensation switching at 250 kHz ± 10%. As shown in Figure 2, the VDDQ output voltage is divided down and fed back to the inverting input of an amplifier through the FBDDQ pin to close the loop at VDDQ = VFBQ × (1 + R2/R1). This amplifier compares the feedback voltage with an internal VREF1 (=1.190 V) to generate an error signal for the PWM comparator. This error signal is further compared with a fixed frequency RAMP waveform to generate a PWM signal. This PWM signal drives the external NFETs via the TG_DDQ and BG_DDQ pins. External inductor L and capacitor COUT1 filter the output voltage. When the NCP5209 leaves S5 mode, the VDDQ output voltage ramps up at a rate controlled by the capacitor at the SS pin. When VDDQ is regulating in S0 mode, a signal _INREGDDQ goes HIGH.

In S3 standby mode, the switching frequency is doubled to reduce the conduction loss in the external NFETs.

### Tolerance of VDDQ

Both the tolerance of VFBDDQ and the ratio of external resistor divider R2/R1 impact the precision of VDDQ. When the control loop is in regulation, VDDQ = VFBQ × (1 + R2/R1). With a worst case (for all valid operating conditions) VFBDDQ tolerance of ±2.0%, a worst case range of ±2.5% for VDDQ can be assured if the ratio R2/R1 is specified as 1.10 ±1%.

### Fault Protection of VDDQ Regulator

In S0 mode, an external resistor (RL1) connecting the 5VATX supply to the OCDDQ pin sets the current limit for the high−side switch. An internal 40 μA current sink at the OCDDQ pin establishes a voltage drop across this resistor. The inductor node voltage is sensed at the SWDDQ pin through a resistor (RSWDDQ). The voltage at the OCDDQ pin is compared to the voltage at the SWDDQ pin when the high−side FET is turned on after a fixed period of blanking time thus avoiding false current limit triggering. If the voltage at SW_DDQ is lower than that at OCDDQ, an over−current condition occurs, during which, all regulators are latched off to protect against over−current. The IC can be powered up again only if any one of supply voltages (5VDUAL, 12VATX or 5VATX) is recycled or the SS pin is discharged to ground externally.

Since the OCDDQ pin is also used for detecting the 5VATX power supply, the upper threshold of the 5VATX UVLO is set to 1.25 V. Therefore, RL1 must be selected in such a way that the voltage at the OCDDQ pin must be higher than this threshold to avoid false triggering of the UVLO.

In S3 mode, this over−current protection feature is disabled.

### Feedback Compensation of VDDQ Regulator

The compensation network is shown in Figure 2.

### VTT Active Terminator

The VTT active terminator is a two quadrant linear regulator with two internal NFETs to provide current sink and source capability up to 1.8 A. It is active only when the VDDQ regulator is in regulation in S0 mode. It draws power from VDDQ with the internal gate drive power derived from 5VDUAL. While the VTT output is directly connected to the FBVTT pin, the VTT voltage is designed to automatically track at the half of the DDQ_REF voltage. This VTT voltage can be adjusted by using an external resistor divider in the feedback loop. This regulator is stable with any value of output capacitor greater than 470 μF, and is insensitive to ESR ranging from 1 mΩ to 400 mΩ.

### Fault Protection of VTT Active Terminator

To provide protection for the internal FETs, a bi−directional current limit set to 2.4 A is implemented. This current limit is also used as a constant current source during VTT startup.

### Dual Linear Regulators

The dual linear regulators are formed by two high−gain controllers driving external NFETs. They are activated after the DDQ regulator is in regulation in S0 mode. The output voltage of each regulator is fed back through an external resistor divider. The feedback voltage is compared to an internal reference voltage VREF2 (=0.800 V) to achieve voltage regulation.

Both linear regulators use a common soft−start ramp voltage set to 1.5 ms. Once they are activated, hiccup mode is employed during the soft−start period to protect them against short circuit or power failure conditions. In the soft−start interval, the feedback voltages of both regulators are compared with the soft−start ramping voltage. If either one of feedback voltages is 100 mV below the SS ramping voltage, a short circuit or power failure condition is detected,

causing both regulators to be reset and initiate the soft start sequence again, as depicted in Figure 3. This hiccup mode feature is disabled once after both outputs are in regulation.

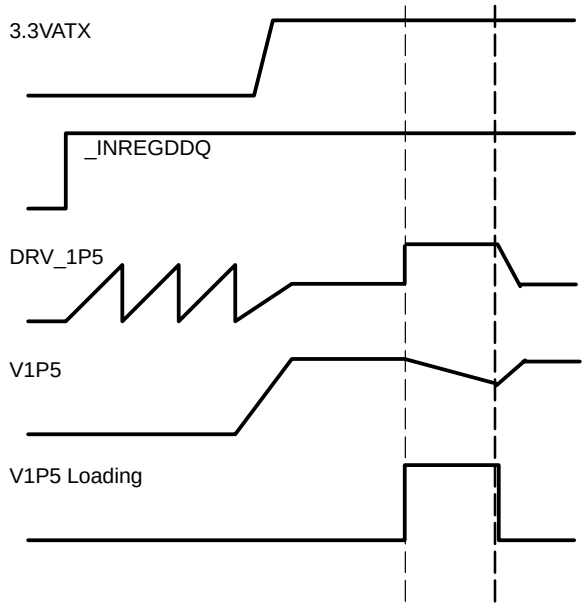



**Figure 3. Hiccup Mode Soft−start of Dual Linear Regulators**

These two linear regulators can be cascaded to generate the 1.5 V MCH core voltage with 2.4 V as the intermediate voltage. By using the 3.3 V ATX as the power supply for the external NFETs, up to 7 A can be delivered.

If only one linear regulator is used, it is recommended to pull the feedback pin of the unused regulator to 5VDUAL to reduce the internal power consumption as well as to avoid soft−start issues.

### Fault Protection of Dual Linear Regulators

Internal soft−start is built−in to limit the in−rush current.

### BOOT Pin Supply Voltage

In a typical application, a flying capacitor is connected between the inductor LX node and the BOOT pin. In S0 mode, the 12VATX supply is tied to the BOOT pin through a Schottky diode. A 13 V zener diode must be put as close to the BOOT pin as possible to clamp the boot strapping voltage produced by the flying capacitor.

In S3 mode the 12VATX supply is collapsed. The BOOT voltage is created by the Schottky diode between 5VDUAL and BOOT pins and the flying capacitor.

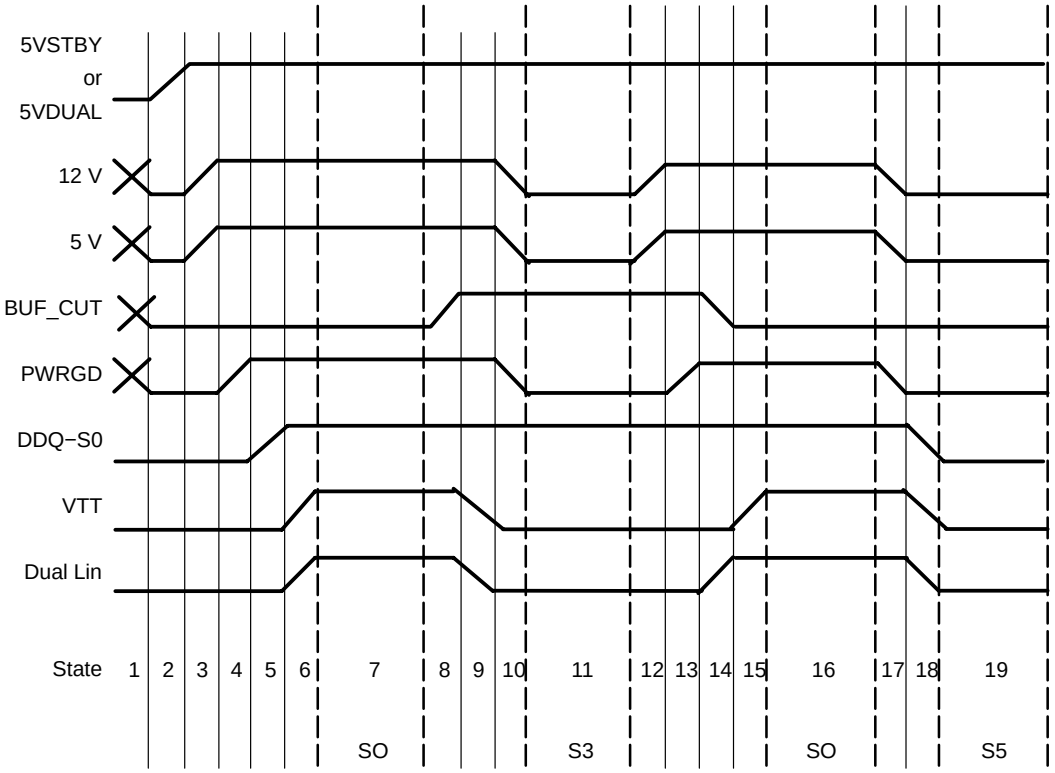
### Thermal Consideration

Assuming an ambient temperature of 50°C, the maximum allowed dissipated power of the QFN−20 package is 1.45 W. Thus a maximum of 0.8 A of DC current can be handled by the VTT regulator in S0 mode. To take full advantage of the thermal capability of this package, the exposed pad underneath must be soldered directly onto a PCB metal substrate to allow good thermal contact.

### Thermal Shutdown

The device will enter S5 mode from any operating mode if the junction temperature of the NCP5209 exceeds 140°C. It will resume normal operation (from S5 to S0 mode) when the junction temperature falls below 115°C.

## Power Up and Power Down Timing




1 5VSTBY or 5VSTB is ultimate chip enable. This supply has to be up first to ensure gates are in known state.
3 12 V and 5 V Supplies can Ramp in Either Order
4 PWRGD asserts to indicate 5VDUAL has switched to 5VCC
5 DDQ ramps up with timing set by the SS pin
6 MCH and VTT both ramp once DDQ SS is completed and DDQ is within 90% of regulated voltage
7 SO Operation
8 Prepare S3 Mode −− BUF_CUT = H
9 VTT and MCH will be turned off
10 12V and 5V ramp down to 0 volts, so as PWRGD
11 Standard S3 State
12 12V and 5V ramp back to regulation
13 PWRGD ramps up to indicate that 5VDUAL has switched to 5VCC
14 DDQ switches back to 250kHz and MCH ramps up
15 VTT ramps up after BUF_CUT goes LOW
16 SO Operation
17 S5 mode −− BUF_CUT = L and (12VUVLO = L or 5VUVLO = L )
18 DDQ, VTT and MCH turned off
19 S5 Mode

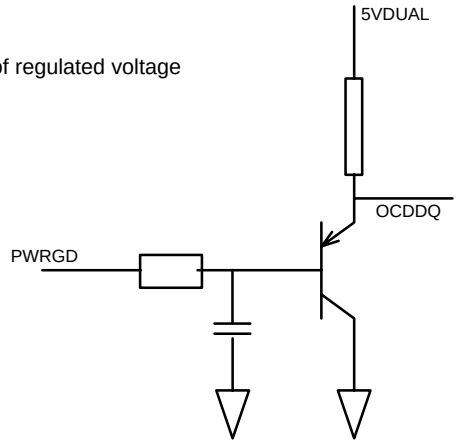
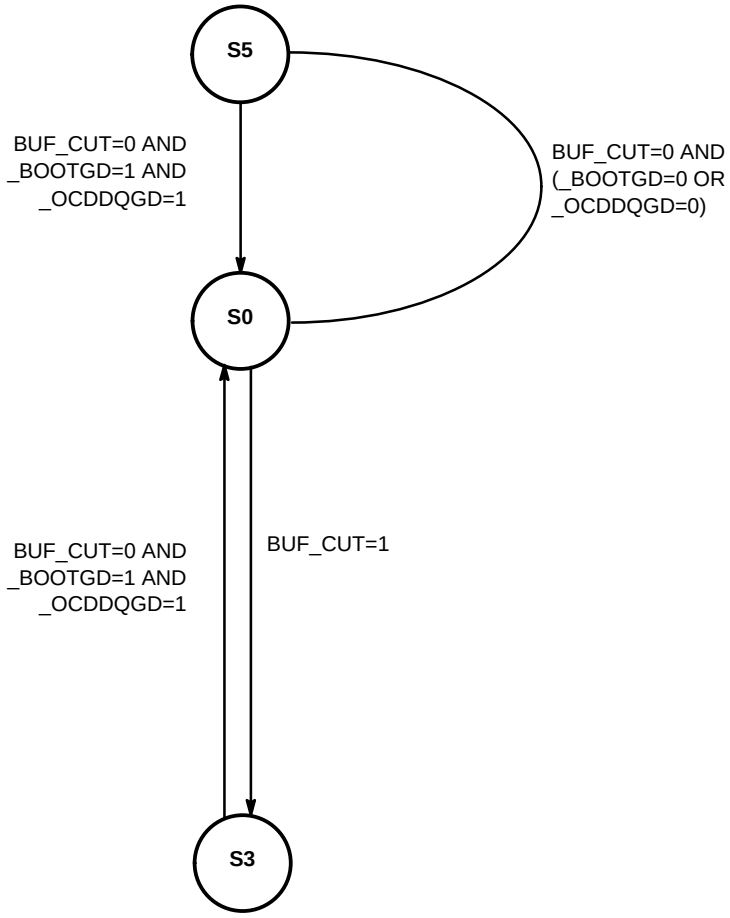



**Figure 4. Timing Diagram**

### State Transition Diagram




NOTES: Note: 5VDUAL is assumed to be in good conditions in any mode.
All possible state transitions are shown.
All unspecified inputs do not cause any state change.

**Figure 5. State Transition Diagram.**

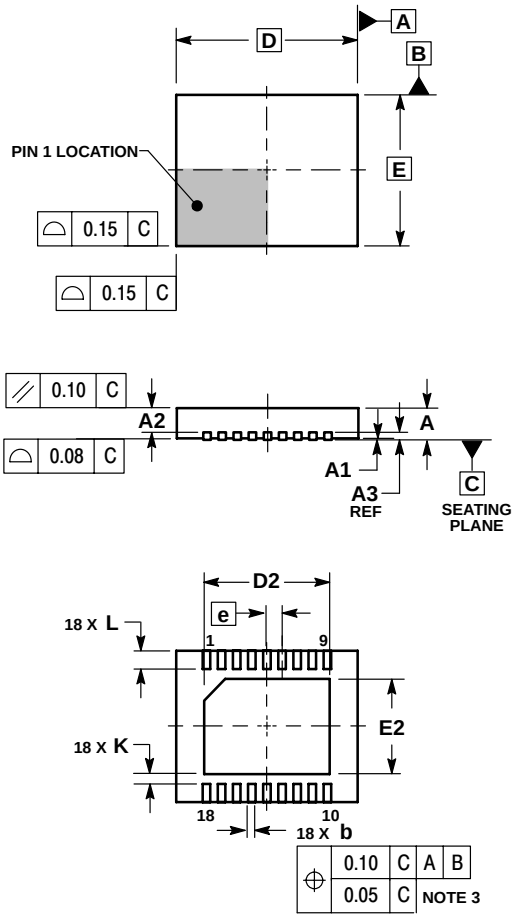
### Applications Information

In some systems, the switching of 5VDUAL from 5VSTBY to 5VATX or vice versa does not automatically occur during mode transitions. To avoid overloading the 5VSTBY supply, a PWRGD signal, which is asserted only when 5VDUAL has been switched over to 5VATX, is created. This PWRGD signal is then used for controlling one of the UVLOs of this device so that the device can only enter S0 after the 5VDUAL has been switched over to 5VATX.

# NCP5209

## PACKAGE DIMENSIONS

**[Package Designation]**
**MN SUFFIX**
CASE 505−01
ISSUE A




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A2 | 0.65 | 0.75 |
| A3 | 0.20 REF | |
| b | 0.23 | 0.28 |
| D | 6.00 BSC | |
| D2 | 3.98 | 4.28 |
| E | 5.00 BSC | |
| E2 | 2.98 | 3.28 |
| e | 0.50 BSC | |
| K | 0.20 | −−− |
| L | 0.50 | 0.60 |



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