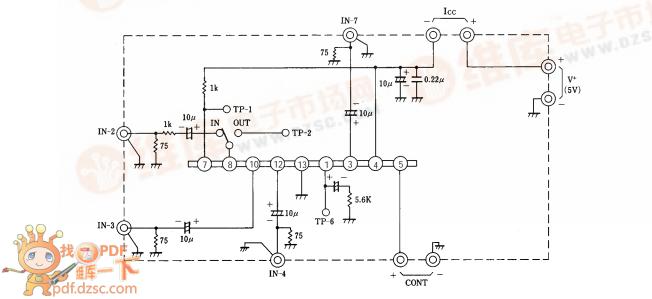


TEST CIRCUIT



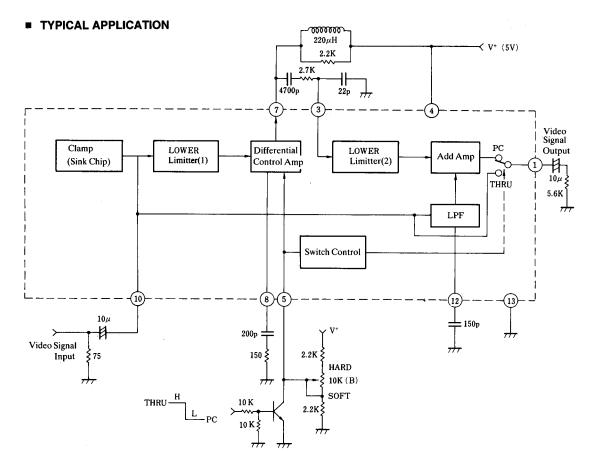
ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RAT	(Ta=25°C		
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V*	8	v
Power Dissipation	PD	(DMP8) 300	mW
Operating Temperature Range	Topr	-20~+75	τ
Storage Temperature Range	Tstg	-40~+125	°C

ELECTRICAL CHARACTERISTICS

(V⁺=5V, Ta=25°C, Refer to Test Circuit))

PARAMETER		SYMBOL	SIGNAL PIN	TEST PIN	CONT. VOLTAGE	TEST CONDITION	MIN.	ТҮР.	MAX.	UNIT
Operating Current		Icc			2.8V	No Input Signal	_	7.5	10	mA
Limitter Level (1)		LIMI	3	2		SYNC level>0.35V,Input Video Signal	0.23	0.27	0.31	v
Limitter Level (2)		LIM2	7	6	—	f=100kHz, 1V _{P-P} Sine Wave Input	0.21	0.25	0.29	v
Control Amp Gain	н	Gн	2	1	2.8V	f=100kHz,0.1Vrms.Sine Wave Input G=20 $\log_{10}V_{out}/V_{1N}$ (dB)	-2	-0.9	0	dB
	м	Gм	2	1	1.3V		-12	-10	-8	dB
	L	GL	2	1	0.45V			_	-28	dB
Add	3pin input	G7	.7	6	2.8V	$f=100kHz, 200mV_{PP} \text{ Sine Wave}$ G=20 log ₁₀ V _{OUT} /V _{IN} (dB)	-1.6	-0.6	0.4	dB
	₁₀ pin input	G3	3	6	2.8V	I V _{P-P} Video Signal Input G=20Log 10 V _{OUT} /V _{IN} (dB)	-1	0	+1	dB
Switch Cross Talk		Csw	4	6	2.8→0V	f=2MHz, $1V_{P-P}$ Sine Wave C _{SW} =20 log ₁₀ V(0V)/V(2.8V) (dB)	_	-50	_	dB
Through Gain		GT	3	6	0V	$V_{P,P}$ Video Signal Input $G_T = 20 \log_{10} V_{OUT}/V_{IN}$ (dB)	-1	0	1	dB
Switch Control Threshold Voltage		V _{TH}	4	6		f=100kHz, 1V _{p-p} Sine Wave Input -40dB=20log ₁₀ V _{OUT} /V _{IN}	0.2	0.3	0.4	v
Differential Gain(Note 1)		DG _{PC}	3	6	2.8V	DGDP Tester	_	1	3	%
Differential Gain(Note 2)		DGT	3	6	0V	Video Signal 1V _{p-p} (Stair Step)		0	3	%
1 PIN Voltage(Note 1)		V _{6PC}		6	2.8V			1.8	_	v
1 PIN Voltage(Note 2)		V _{6T}		6	0V		—	2.0	-	v



PRINCIPLES OF OPERATION, BI BLOCK DIAGRAM

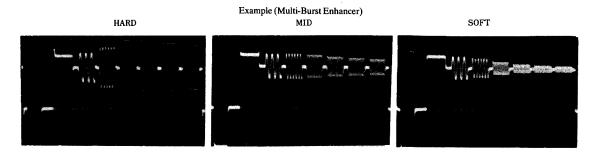
The NJM2209 is a video signal IC which converts an input video signal to a compensated video signal of the picture outline by adding an input signal through a differential amplifier to the original input signal.

The compensating (enhanced) ratio is decided by pin 5 voltage and so the original signal comes when pin 5 voltage is zero.

A peaking frequency compensation of the internal

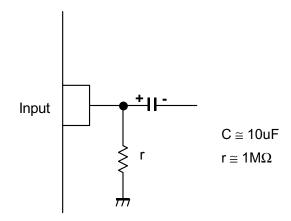
differential amplifier is changed by C,R attached to pin 8 and L,R to pin 7.

The compensation signal and the original video signal are delayed the phase by low pass filter. These are done by a capacitor attached to pin12. The compensated ratio is originally settled by the coupling condenser between pin7 and pin 3.



This IC requires $1M\Omega$ resistance between INPUT and GND pin for clamp type input since the minute causes an unstable pin voltage.

New Japan Radio Co., Ltd.



[CAUTION] The specifications on this databook given for information , without any gu as regards either mistakes or omission as regards enter initiatates to offination application circuits in this databook a described only to show representativ of the product and not intended for th guarantee or permission of any right the industrial rights.