

## MOS Memories

# FUJITSU

### ■ MBM27C256A-20-W MBM27C256A-25-W

CMOS 32,768 x 8-Bit UV Erasable  
and Electrically Programmable  
Read Only Memory

#### Description

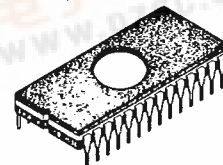
The Fujitsu MBM27C256A-W is a high speed 262,144-bits UV erasable and electrically reprogrammable read only memory (EPROM) with CMOS technology. It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-pad Leadless Chip Carrier (LCC) are used to package the MBM27C256A-W. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

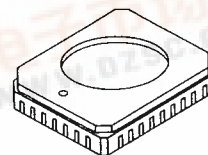
The MBM27C256A-W is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

#### Features

- Wide temperature range: -55°C to +125°C
- CMOS Power Consumption: 550  $\mu$ W max. (Standby) 41 mW/MHz (Active)
- 32,768 words by 8-bits organization, fully decoded
- Simple programming requirements
- Single location programming
- High speed programming algorithm (typically two 1 ms pulses)
- No clock required (fully static operation)
- Programming voltage: 12.5V
- Single +5V supply,  $\pm 10\%$
- TTL compatible inputs and outputs
- 3-state output with OR-tie capability
- Output Enable ( $\overline{OE}$ ) pin for simplified memory expansion
- Fast access time: MBM27C256A-20-W 200 ns max. MBM27C256A-25-W 250 ns max.
- Single +5V operation
- Standard 28-pin DIP package/32-pad LCC



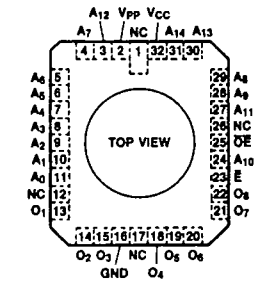
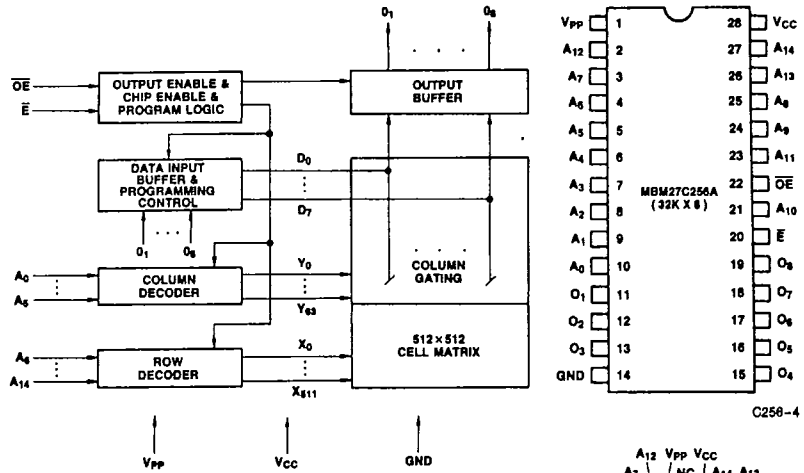
Ceramic Package  
DIP-28C-C01



Leadless Chip Carrier  
LCC-32C-A01

**MBM27C256A-20-W**  
**MBM27C256A-25-W**

**MBM27C256A Block Diagram and Pin Assignments**



**Absolute Maximum Ratings**  
 (See Note)

Parameter	Symbol	Value	Unit
Temperature under bias	T <sub>BIAS</sub>	-65 to +125	°C
Storage temperature	T <sub>STG</sub>	-65 to +150	°C
Inputs/outputs with respect to GND	V <sub>IN</sub> , V <sub>OUT</sub>	-0.6 to +7	V
Voltage on A <sub>9</sub> with respect to GND	V <sub>A9</sub>	-0.6 to +13.5	V
V <sub>PP</sub> with respect to GND	V <sub>PP</sub>	-0.6 to +14	V
V <sub>CC</sub> with respect to GND	V <sub>CC</sub>	-0.6 to +7	V

**Note:**  
 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

**MBM27C256A-20-W**  
**MBM27C256A-25-W**

**Functions and Pin Connections**

Function (Pin No.)	Address Input (2~10, 21, 23~27)	A <sub>0</sub> (24)	Data I/O (11~13, 15~19)	$\bar{E}$ (20)	$\bar{OE}$ (22)	V <sub>CC</sub> (28)	V <sub>PP</sub> (1)	GND (14)
Mode								
Read	A <sub>IN</sub>	A <sub>IN</sub>	OUT	V <sub>IL</sub>	V <sub>IL</sub>	+5V	+5V	GND
Output disable	A <sub>IN</sub>	A <sub>IN</sub>	High Z	V <sub>IL</sub>	V <sub>IH</sub>	+5V	+5V	GND
Stand by	Don't care	Don't care	High Z	V <sub>IH</sub>	Don't care	+5V	+5V	GND
Program	A <sub>IN</sub>	A <sub>IN</sub>	IN	V <sub>IL</sub>	V <sub>IH</sub>	+6V	+12.5V	GND
Program verify	A <sub>IN</sub>	A <sub>IN</sub>	OUT	V <sub>IL</sub>	V <sub>IL</sub>	+6V	+12.5V	GND
Program inhibit	Don't care	Don't care	High Z	V <sub>IH</sub>	Don't care	+6V	+12.5V	GND
Electronic signature	A <sub>IN</sub>	+12V	Code	V <sub>IL</sub>	V <sub>IL</sub>	+5V	+5V	GND

**Recommended Operating Conditions**  
 (Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V <sub>CC</sub> supply voltage (1)	V <sub>CC</sub>	4.5	5.0	5.5	V	-55°C to +125°C
V <sub>PP</sub> supply voltage	V <sub>PP</sub>	V <sub>CC</sub> -0.6		V <sub>CC</sub> +0.6	V	
Input high voltage	V <sub>IH</sub>	2.0		V <sub>CC</sub> +0.3	V	
Input low voltage	V <sub>IL</sub>	-0.1		0.8	V	

**Note:**

1. V<sub>CC</sub> must be applied either before or coincident with V<sub>PP</sub> and removed either after or coincident with V<sub>PP</sub>.

**Capacitance**  
 (T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance (V <sub>IN</sub> = 0V)	C <sub>IN</sub>		4	6	pF
Output capacitance (V <sub>OUT</sub> = 0V)	C <sub>OUT</sub>		8	12	pF

**DC Characteristics**  
 (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input load current (V <sub>IN</sub> = 5.5V)	I <sub>LI</sub>			10	μA
Output leakage current (V <sub>OUT</sub> = 5.5V)	I <sub>LO</sub>			10	μA
V <sub>PP</sub> supply current	I <sub>PP</sub>		1	100	μA
V <sub>CC</sub> standby current ( $\bar{E}$ = V <sub>IH</sub> )	I <sub>SB1</sub>			1	mA
V <sub>CC</sub> standby current ( $\bar{E}$ = V <sub>CC</sub> -0.3V to V <sub>CC</sub> +0.3V, I <sub>OUT</sub> = 0 mA)	I <sub>SB2</sub>		1	100	μA
V <sub>CC</sub> active current ( $\bar{E}$ = V <sub>IL</sub> )	I <sub>CC1</sub>			30	mA
V <sub>CC</sub> operation current (f = 4 MHz, I <sub>OUT</sub> = 0 mA)	I <sub>CC2</sub>			30	mA
Output low voltage (I <sub>OL</sub> = 2.1 mA)	V <sub>OL</sub>			0.45	V
Output high voltage (I <sub>OH</sub> = -400 μA)	V <sub>OH1</sub>	2.4			V
Output high voltage (I <sub>OH</sub> = -100 μA)	V <sub>OH2</sub>	V <sub>CC</sub> -0.7			V

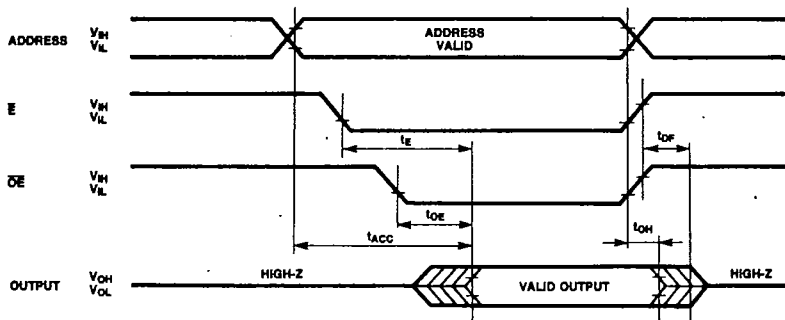
**MBM27C256A-20-W**  
**MBM27C256A-25-W**

**AC Characteristics**  
 (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM27C256A-20		MBM27C256A-25		Unit
		Min	Max	Min	Max	
Address access time (1) ( $\bar{E} = \bar{OE} = V_{IL}$ )	$t_{ACC}$		200		250	ns
$\bar{E}$ to output valid ( $\bar{OE} = V_{IL}$ )	$t_E$		200		250	ns
$\bar{OE}$ to output valid ( $\bar{E} = V_{IL}$ ) (1)	$t_{OE}$		75		100	ns
$\bar{OE}, \bar{E}$ high to output float (2,3)	$t_{DF}$	0	60	0	60	ns
Address to output hold (3)	$t_{OH}$	0		0		ns

- Notes:**
- $\bar{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the following edge of  $\bar{E}$  without impact on  $t_{ACC}$ .
  - $t_{DF}$  is specified from  $\bar{OE}, \bar{E}$ , whichever occurs first. Output float is defined as the point where data is no longer driven.
  - Sampling, not 100% tested.

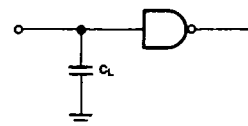
**Operation Timing Diagram**



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**AC Test Conditions**  
 (Including programming)

Input Pulse Levels: ..... 0.45V to 2.4V  
 Input Rise and Fall Time: .....  $\leq 20$  ns  
 Timing Measurement Reference Levels: 1.0V and 2.0V for inputs  
 0.8V and 2.0V for outputs  
 Output Load: ..... 1 TTL gate and  $C_L = 100$  pF



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**MBM27C256A-20-W**  
**MBM27C256A-25-W**

**Programming/Erasing Information**

**Memory Cell Description**

The MBM27C256A-W is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate as shown in Memory Cell diagram. The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold as shown in Memory Cell Threshold Shift diagram. In the initial state, the cell has a low threshold ( $V_{TH1}$ ) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level ( $V_{TH0}$ ), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold ( $V_{THS}$ ), as indicated by the dotted line as shown in Memory Cell Threshold Shift diagram.

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C256A-W has all 262,144-bits in the "1", or high, state. "0's" are loaded into the MBM27C256A-W through the procedure of programming.

The MBM27C256A-W is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to the  $V_{PP}$  pin and  $V_{CC}$  pin respectively, and  $\bar{E}$  and  $\bar{OE}$  are at  $V_{IH}$ . A 0.1  $\mu$ F capacitor between  $V_{PP}$  and GND is needed to prevent excessive voltage transients, which could damage the de-

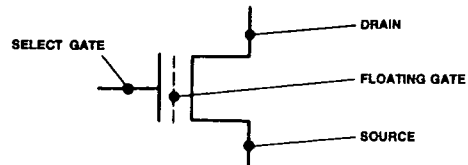
vice. The address to be programmed is applied to the proper address pins. The 8-bit pattern is placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a sequence of single TTL low-level pulses are applied to the  $\bar{E}$  pin followed by an additional pulse to the  $\bar{E}$  pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flow chart.)

- 1) Input the start address (start address = G).
- 2) Set  $V_{CC} = 6V$ ,  $V_{PP} = 12.5V$  and  $\bar{E} = V_{IH}$ .
- 3) Clear the programming pulse counter ( $X \leftarrow 0$ ).
- 4) Input data to respective pins.
- 5) Apply ONE programming pulse ( $t_{PW} = 1 \text{ ms Typ.}$ ) to  $\bar{E}$ .
- 6) Increment the counter ( $X \leftarrow X + 1$ ).
- 7) Compare the number ( $= X$ ) of applied programming pulse with 25 and then verify the programmed data. If the programmed data is verified, go to the next step regardless of X value. If  $X = 25$  and programmed data is not verified, the device fails.
- 8) Apply one additional wide programming pulse to  $\bar{E}$  (3X ms).
- 9) Compare the address with an end address ( $= N$ ). If the programmed address is the end address, proceed to the next step. If not, increment the address ( $G \leftarrow G + 1$ ) and then go to the step 3) for the next address.
- 10) Set  $V_{CC} = V_{PP} = 5V$ .
- 11) Verify all the data. If the programmed data is not the same as the input data, the part failed. If it is the same, the program is completed.

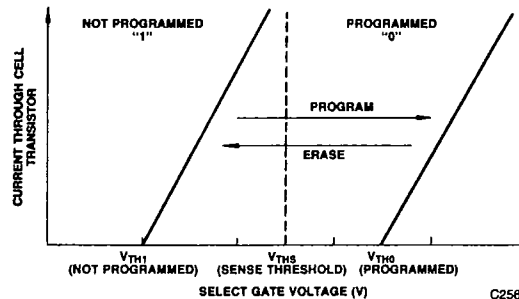
A continuous TTL low level should not apply to  $\bar{CE}$  input pin during the program mode ( $V_{PP} = 12.5V$ ,  $V_{CC} = 6V$  and  $\bar{OE} = V_{IH}$ ) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

**Memory Cell**



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**Memory Cell Threshold Shift**



C256-9

Quick Pro™ is a trademark of Fujitsu Limited.

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**MBM27C256A-20-W**  
**MBM27C256A-25-W****Programming/Erasing Information (Continued)****Erasure**

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C256A-W to an ultraviolet light source. A dosage of 15W-seconds/cm<sup>2</sup> is required to completely erase an MBM27C256A-W. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of

12,000 μW/cm<sup>2</sup> for 15 to 20 minutes. The MBM27C256A-W should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C256A-W and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although

erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C256A-W and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

**AC Characteristics**

(T<sub>A</sub> = 25°C ± 5°C,  
V<sub>CC</sub> = 6V ± 0.25V,  
V<sub>pp</sub> = 12.5V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t <sub>AS</sub>	2			μs
Chip enable setup time	t <sub>CES</sub>	2			μs
Output enable setup time	t <sub>OES</sub>	2			μs
Data setup time	t <sub>DS</sub>	2			μs
V <sub>pp</sub> setup time	t <sub>VS</sub>	2			μs
Address hold time	t <sub>AH</sub>	2			μs
Output enable hold time (1)	t <sub>OEH</sub>	2			μs
Data hold time	t <sub>DH</sub>	2			μs
Output enable recovery time (1)	t <sub>OR</sub>	2			μs
Chip enable to data valid	t <sub>DV</sub>			1	μs
Output disable to output float delay	t <sub>DF</sub>			105	ns
Programming pulse width	t <sub>PW</sub>	0.95	1	1.05	ms
Additional programming pulse width	t <sub>APW</sub>	2.85		78.75	ms
Programming pulse number	X	1		25	times

**Note:**

1. t<sub>OEH</sub> + t<sub>OR</sub> ≥ 50 μs.

**Electronic Signature**

The MBM27C256A-W has electronic signature mode which is intended to be used with programming equipment for the purpose of automatically matching the device to be programmed with its cor-

responding programming algorithm.

The electronic signature is activated when +12V is applied to address line A<sub>9</sub> (pin 24) of the MBM27C256A-W. Two identifier bytes are read out

from the outputs by toggling address line A<sub>0</sub> (pin 10) from V<sub>IL</sub> to V<sub>IH</sub>. The address lines from A<sub>1</sub> and A<sub>13</sub> must be held at V<sub>IL</sub> to keep the electronic signature mode. See the table below.

A <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	Definition
V <sub>IL</sub>	0	0	1	0	0	0	0	0	Manufacture
V <sub>IH</sub>	0	1	0	0	0	1	1	0	Device

**Notes:**

A<sub>9</sub> = 12V ± 0.5V.

A<sub>1</sub> thru A<sub>8</sub> = A<sub>10</sub> thru A<sub>13</sub> = CE = OE = V<sub>IL</sub>.

A<sub>14</sub> = Either V<sub>IL</sub> or V<sub>IH</sub>.

**MBM27C256A-20-W**  
**MBM27C256A-25-W**

**Programming/Erasing Information (Continued)**

**DC Characteristics**

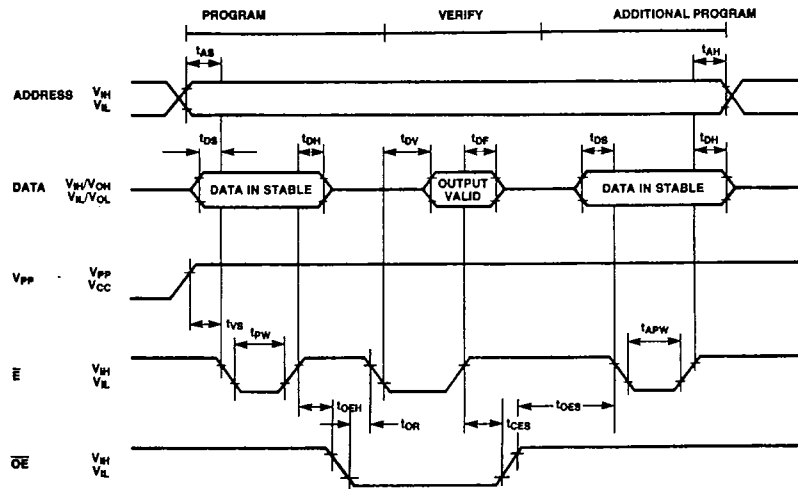
( $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ ,  
 $V_{CC} = 6\text{V} \pm 0.25\text{V}$ ,  
 $V_{PP} = 21\text{V} \pm 0.5\text{V}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current ( $V_{IN} = 5.25\text{V}/0.45\text{V}$ )	$I_{LI}$			10	$\mu\text{A}$
$V_{PP}$ supply current during programming pulse ( $\bar{E} = V_{IL}$ )	$I_{PP}$			40	$\text{mA}$
$V_{CC}$ supply current	$I_{CC}$			30	$\text{mA}$
Input low level	$V_{IL}$	-0.1		0.8	V
Input high level	$V_{IH}$	2.0		$V_{CC} + 0.3$	V
Output low voltage during verify ( $I_{OL} = 2.1\text{mA}$ )	$V_{OL}$			0.45	V
Output high voltage during verify ( $I_{OH} = -400\mu\text{A}$ )	$V_{OH}$	2.4			V

**Notes:**

$V_{CC}$  must be applied either coincident with or before  $V_{PP}$  and removed either coincident with or after  $V_{PP}$ .  
 $V_{PP}$  must not be greater than 21.5V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with  $V_{PP} = 21\text{V}$ . Also, during  $\bar{E} = V_{IL}$ ,  $V_{PP}$  must not be switched from 5V to 21V or vice-versa.

**Programming Waveform**



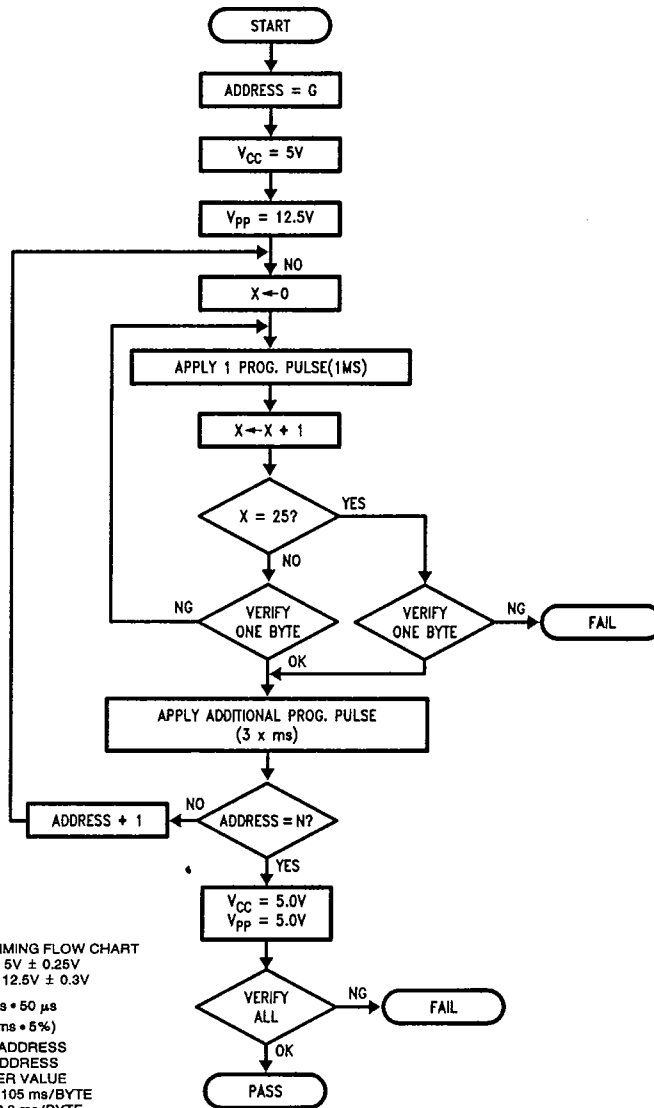
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**MBM27C256A-20-W**  
**MBM27C256A-25-W**

**Programming/Erasing**  
**Information (Continued)**

**Quick Program Flow Chart**



PROGRAMMING FLOW CHART  
 $V_{CC} = 5V \pm 0.25V$   
 $V_{PP} = 12.5V \pm 0.3V$   
 $TPW = 1ms + 50\mu s$   
 (\*Xms + 5%)  
 G: START ADDRESS  
 N: STOP ADDRESS  
 X: COUNTER VALUE  
 MAXIMUM 105 ms/BYTE  
 MINIMUM 3.8 ms/BYTE

C256-11



