

PRELIMINARY

VFD CONTROLLER DRIVER

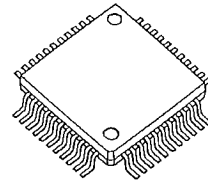
■ GENERAL DESCRIPTION

The **NJU3423** is a VFD (Vacuum Fluorescent Display) Controller Driver with key function.

It contains display data RAM, address counter, command register, high voltage drivers, and serial interface circuit.

The display data, the command data and the key scanning data can be transmitted with the serial interface, and VFD driving voltage is up to 45V. The **NJU3423** is useful for car audio, VCR and other VFD application items.

■ PACKAGE OUTLINE



NJU3423F

■ FEATURES

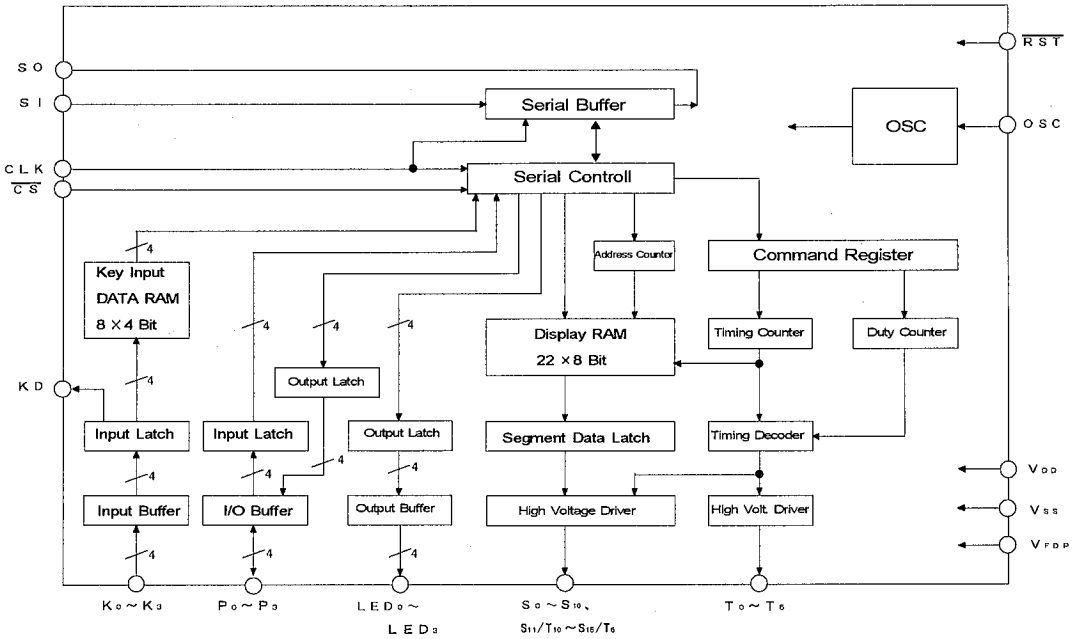
- VFD Driving Voltage | $V_{DD}-V_{FDP}$ | =45V
- Display Mode 11 Segments Display × 11 Digits
16 Segments Display × 6 Digits
- Display ON/OFF Function
- Display Scan Function (Digit Signal)
- Display Data RAM 22 × 8 Bits
- Key Input Data RAM 8 × 4 Bits
- Key Scan Function 8 × 4 Key max.
- I/O Port (4 Ports)
- LED Driving Port(4 Ports)
- CR Oscillation Circuit on-chip (fosc=5.5MHz Typ)
- External CLK Terminal
- Serial Interface (8 Bit)
- Power On Initialization
- Operating Voltage 5V ± 10%
- Low Operating Current
- C-MOS Technology
- Package Outline QFP 44

■ VERSION

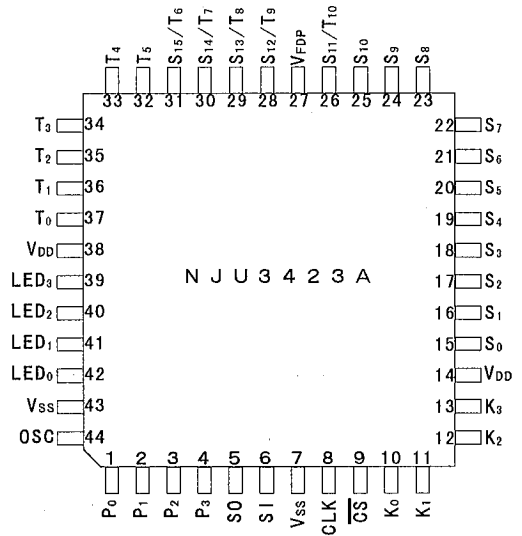
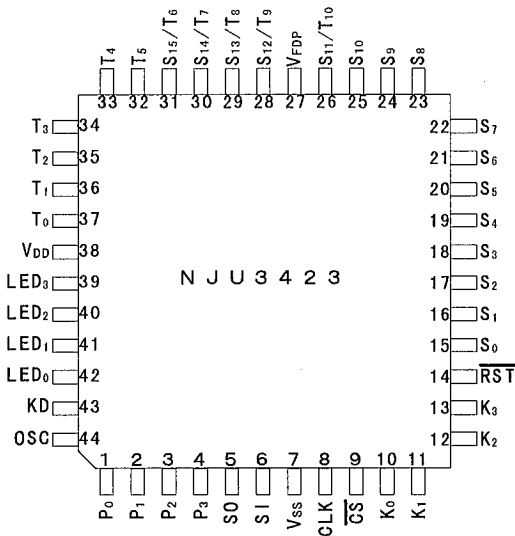
| VERSION | RESET TERMINAL | KEY INPUT DETECT TERMINAL |
|----------|----------------|------------------------------|
| NJU3423 | HAVE | HAVE |
| NJU3423A | NO | NO |

NOTE: Refer to the Pin Configuration

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

| NO. | | SYMBOL | FUNCTION |
|-------------|-------------|--|--|
| NJU3423 | NJU3423A | | |
| 38 | 14,38 | V _{DD} | POWER SOURCE 5 V |
| 7 | 7,43 | V _{SS} | GND 0 V |
| 27 | 27 | V _{FDP} | VFD Driving Voltage V _{DD} -45V |
| 44 | 44 | OSC | External CLK Terminal.(Normally Open) |
| 10~13 | 10~13 | K ₀ ~K ₃ | Key Input Terminals.(Pull-Down Resistance) |
| 43 | — | KD | Key Input Detection Terminal. When Key is input, "H" level is output from this terminal. |
| 15~25 | 15~25 | S ₀ ~S ₁₀ | Segment Output Terminals. (Pull-Down Resistance) |
| 26 28~31 | 26 28~31 | S ₁₁ /T ₁₀ S ₁₂ /T ₉ ~ S ₁₅ /T ₆ | Segment/Timing Output Terminals.(Pull-Down Resistance) |
| 32~37 | 32~37 | T ₅ ~T ₀ | Timing Output Terminals.(Pull-Down Resistance) |
| 14 | — | RST | Reset Terminal(Pull-Up Resistance) RESET operation requires "L" level over than 10 μ S |
| 1~4 | 1~4 | P ₀ ~P ₃ | I/O Ports(Pull-Up Resistance) |
| 5 | 5 | S0 | Serial Data Output Terminal.(8-Bit / Word) Keyscan data (Port,Key data)are output from this terminal. |
| 6 | 6 | SI | Serial Data Input Terminal.(8-Bit / Word) Address, I/O Ports, Command, Display |
| 8 | 8 | CLK | Shift Clock Input Terminal. |
| 9 | 9 | \overline{CS} | Chip Select Input Terminal. Active "L". |
| 39~42 | 39~42 | LED ₃ ~LED ₀ | Output Port Terminal. It can drive LED directly. |

■ TABLE OF INSTRUCTIONS

| INSTRUCTIONS | C O D E | | | | | | | | D E S C R I P T I O N |
|--|---------|-----|-----|-----|------|------|------|------|---|
| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| Reset | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | Resets the system excepting for RAM. |
| Address Set | 0 | 0 | 0 | AD4 | AD3 | AD2 | AD1 | AD0 | Sets DD RAM address. The data(15H to 00H) into address (AD4 to AD0). |
| Write Data to DDRAM | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | Sets Display Data. The data must be set continuously after the address set. |
| Function Set | 1 | DT2 | DT1 | DT0 | DSP | TM2 | TM1 | TM0 | Sets Duty Ratio(DT2~0), Disp.ON/OFF(DSP) and Display Digit(TM2~TM0). |
| Write Data and Input Control to I/O Port | 0 | 1 | 0 | 0 | D3 | D2 | D1 | D0 | Sets I/O Output Data. When the output data selected "H",Input port can use active "L". |
| Write Data to LED Port | 0 | 1 | 1 | 0 | LED3 | LED2 | LED1 | LED0 | Output Control of LED ₀ to LED ₃ . |
| Read Data from I/O Port and Key Input Data | P3 | P2 | P1 | P0 | K3 | K2 | K1 | K0 | When the I/O port data selected "H". Upper 4bit:Port data Lower 4bit:Key data |

■ DESCRIPTION OF EACH INSTRUCTIONS

(1) Reset Circuit

"Reset" operates the initialization by the following instruction and the condition of control logic circuits in the IC is kept during "CS" is low.

| RESET | | | | | | | |
|-------|----|----|----|----|----|----|----|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |

Reset by RST terminal and Power on reset are operated as same as the instruction reset. The condition of output terminals and registers are shown in bellow after reset operation.

· Initialization

- ① Display Off
- ② Display Mode:16-Segment/6-Character
- ③ Duty Ratio :2/16
- ④ Clear the Key Input Latch
- ⑤ Clear the I/O Port Latch
- ⑥ All I/O Port Output:"H"
- ⑦ All LED Port Output:"H"
- ⑧ Clear the serial buffer
- ⑨ Clear the Address Counter
- ⑩ Clear the Timing Counter
- ⑪ Clear the Duty Counter
- ⑫ Clear the Command Register

NOTE) DD RAM and Key Input RAM are not cleared.

(2) Address Counter

The address counter addresses the area of display data RAM to store the display data from the serial interface.

When the first word of the serial data is recognized as the address of the display data RAM (The upper three bits of a byte must be "0"), the lower 5bits are set into the address counter.

The display data, which are input sequentially after the address code are set into the addressed area of display data RAM and the address counter is incremented automatically for next data.

Though the address counter consists of the 5-bit counter, the effective range is from "00000"(00H) to "10101"(15H) and the invalid range is from "10110"(16H) to "11111"(1FH).

The next address of "10101"(15H) is "00000"(00H) with automatic increment operation.

The Address Data

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | AD4 | AD3 | AD2 | AD1 | AD0 |

The mapping of the display data RAM

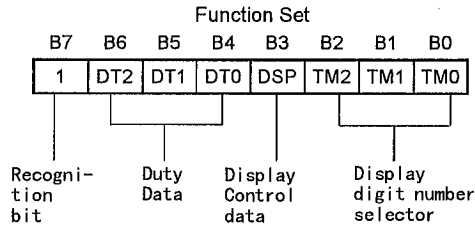
| B7 B6 B5 B4 B3 B2 B1 B0 | | | | | | | | B7 B6 B5 B4 B3 B2 B1 B0 | | | | | | | | | | |
|-------------------------|----|----|----|----|----|----|----|-------------------------|--|-----|-----|-----|-----|-----|-----|-----|----|--|
| 00H | | | | | | | | 01H | | | | | | | | T0 | | |
| 02H | | | | | | | | 03H | | | | | | | | T1 | | |
| 04H | | | | | | | | 05H | | | | | | | | T2 | | |
| 06H | | | | | | | | 07H | | | | | | | | T3 | | |
| 08H | | | | | | | | 09H | | | | | | | | T4 | | |
| 0AH | | | | | | | | 0BH | | | | | | | | T5 | | |
| 0CH | | | | | | | | 0DH | | | | | | | | T6 | | |
| 0EH | | | | | | | | 0FH | | | | | | | | T7 | | |
| 10H | | | | | | | | 11H | | | | | | | | T8 | | |
| 12H | | | | | | | | 13H | | | | | | | | T9 | | |
| 14H | | | | | | | | 15H | | | | | | | | T10 | | |
| | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | | S15 | S14 | S13 | S12 | S11 | S10 | S9 | S8 | |

(3) COMMAND REGISTER

The Command Register is the register for function set of Display Duty, DisplayDigit Number and Display ON/OFF.

When the first word of serial transmitted data is "1", the lower 7bits are set into the commandregister. The Display digit number selector effective range is from "000"(00H) to "101"(05H) and the invalid range is from "110"(06H) and "111"(07H).

The default condition of the display mode is display-off by the power on initialization.



(2-1) Duty set

| DT2 | DT1 | DT0 | Timing signal Duty |
|-----|-----|-----|-----------------------|
| 0 | 0 | 0 | 2/16 |
| 0 | 0 | 1 | 4/16 |
| 0 | 1 | 0 | 6/16 |
| 0 | 1 | 1 | 8/16 |
| 1 | 0 | 0 | 10/16 |
| 1 | 0 | 1 | 12/16 |
| 1 | 1 | 0 | 14/16 |
| 1 | 1 | 1 | 15/16 |

(2-2) Display control set

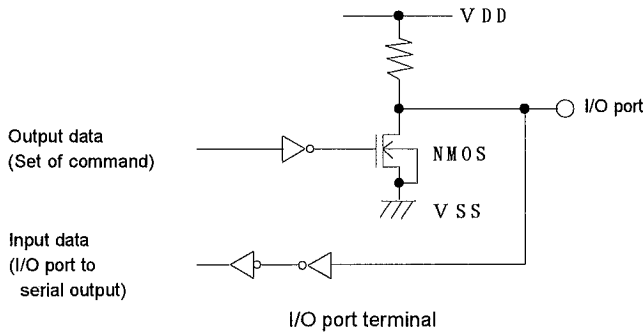
| DSP | Display |
|-----|---------|
| 0 | OFF |
| 1 | ON |

(2-3) Display digit number set

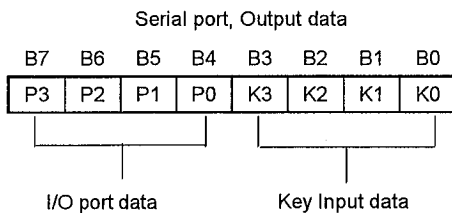
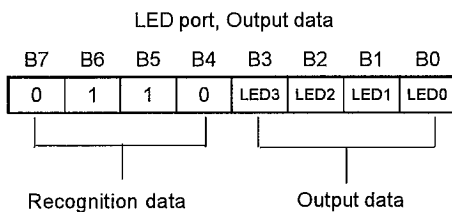
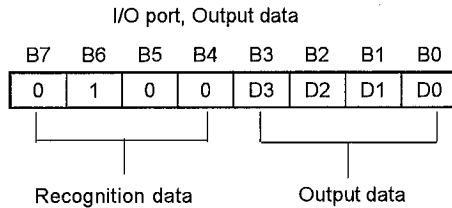
| TM2 | TM1 | TM0 | Digits |
|-----|-----|-----|--------|
| 0 | 0 | 0 | 6 |
| 0 | 0 | 1 | 7 |
| 0 | 1 | 0 | 8 |
| 0 | 1 | 1 | 9 |
| 1 | 0 | 0 | 10 |
| 1 | 0 | 1 | 11 |
| 1 | 1 | 0 | No use |
| 1 | 1 | 1 | No use |

(4) I/O Port, LED Driving Port

The NJU3423 incorporates four I/O ports and four LED driver ports. I/O ports are constructed by the N-channel open-drain type FET with the pull-up resistor. When the output data is set into D3 ~ D0, these I/O ports can be used as the output terminal. In case of input mode "H" level must be set into D3 ~ D0, then these I/O ports can be used as the input terminal with pull-up resistor. The P3 ~ P0 data of input or output is transferred to the MPU with Key Input Data (K3 ~ K0), by the serial interface. When the power supply is turned on, the output data is "H". And the data is hold until the next data is transferred.

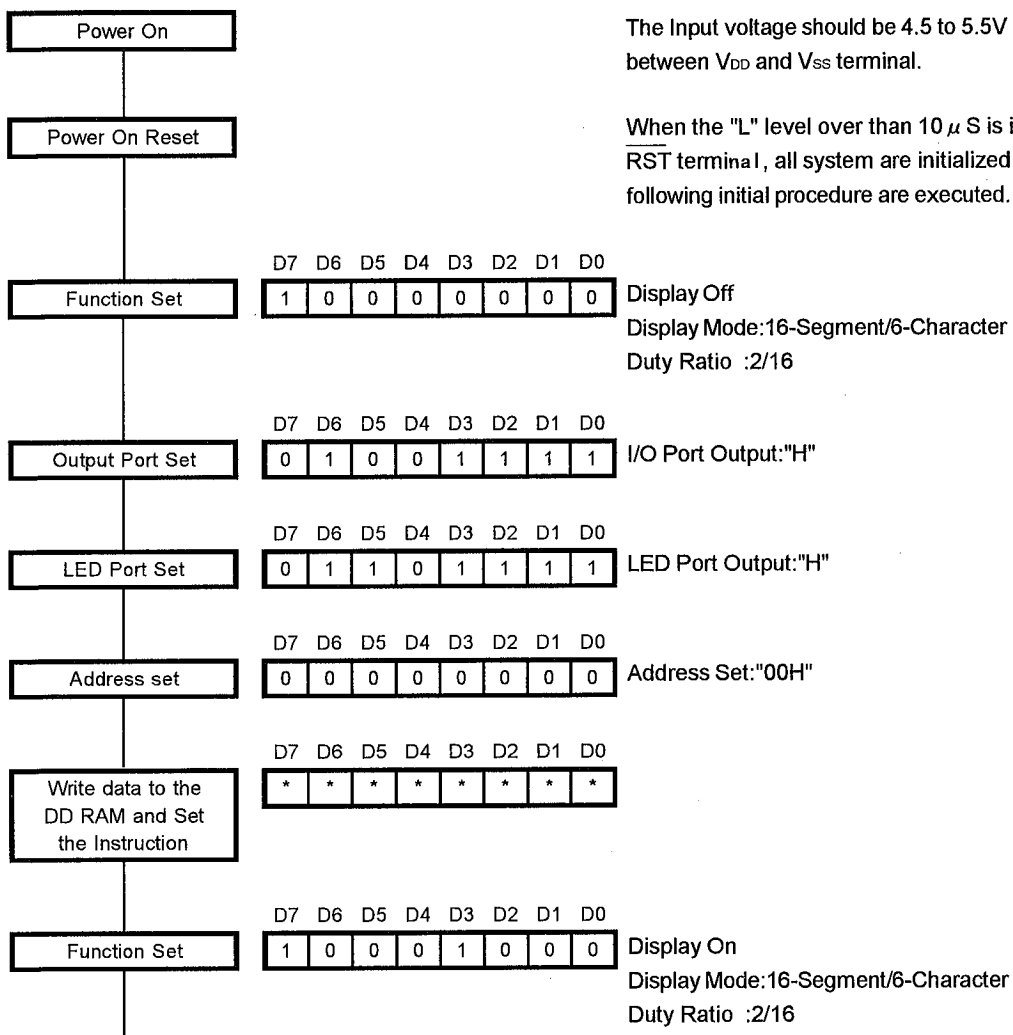


Each Terminals Instructions is shown below.

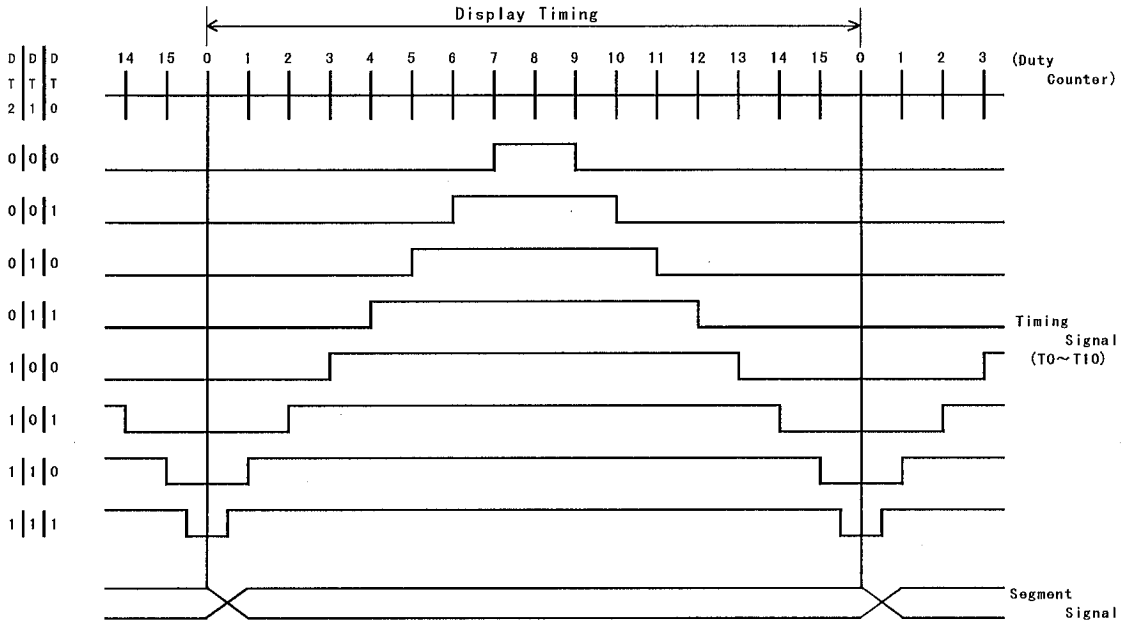


(4-1) INITIALIZATION

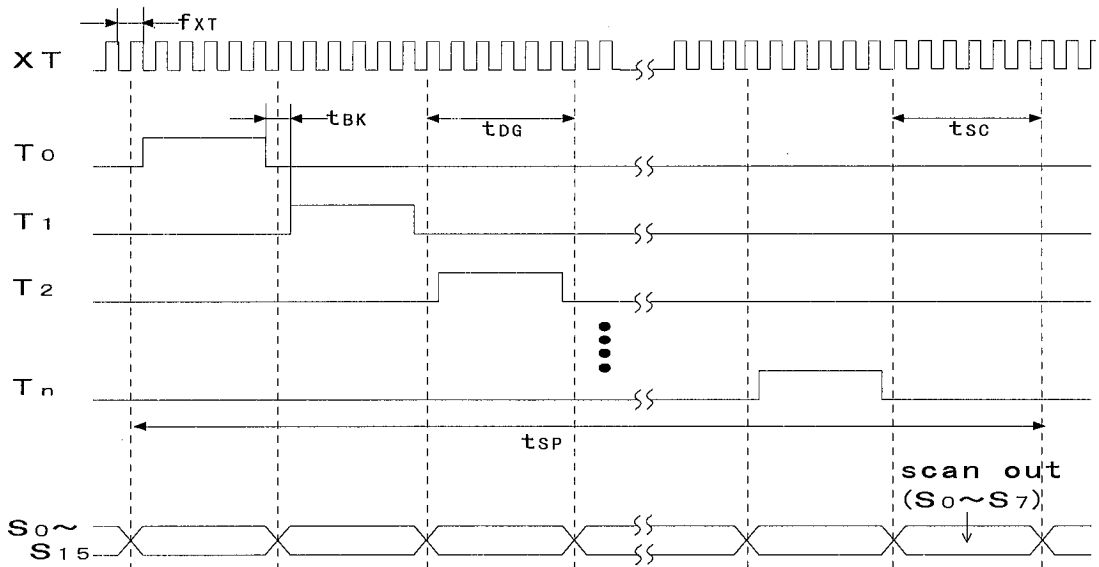
Initialization flow is shown below:



TIMING SIGNAL / DUTY CHANGE WAVEFORM



DISPLAY TIMING CHART



| | |
|------------------------------------|--|
| Oscillation frequency | : f_{XT} |
| Minimum blanking time (Duty 15/16) | : $t_{BK} = (1/f_{XT}) \times 96$ |
| 1 character display time | : $t_{DG} = t_{BK} \times 16$ |
| Key scanning time | : $t_{sc} = t_{DG}$ |
| 1 cycle display time | : $t_{SP} = t_{DG} \times \text{character} + t_{sc}$ |

(5) KEY INPUT CIRCUIT

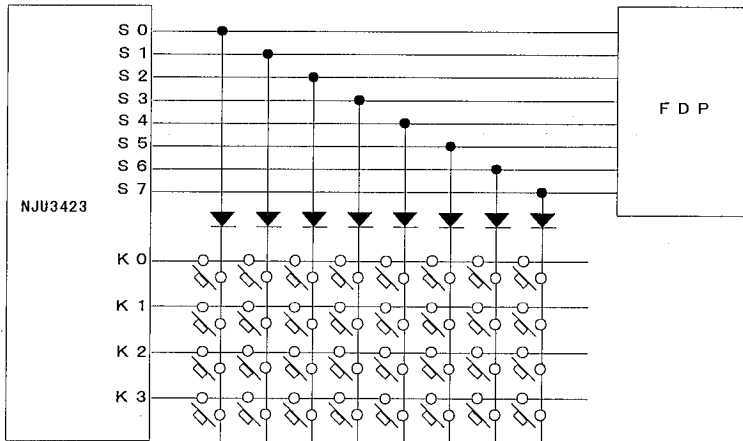
The key input circuit uses 8 terminals of the display segment output for key scanning and the key data are read from 4 input terminals (K0 ~ K3) on the each scanning timing. Then the key data are stored into the key input data RAM, and transmitted to MPU in serial transmission.

The condition of key input terminals are normally "L" and they go to "H" is the key on.

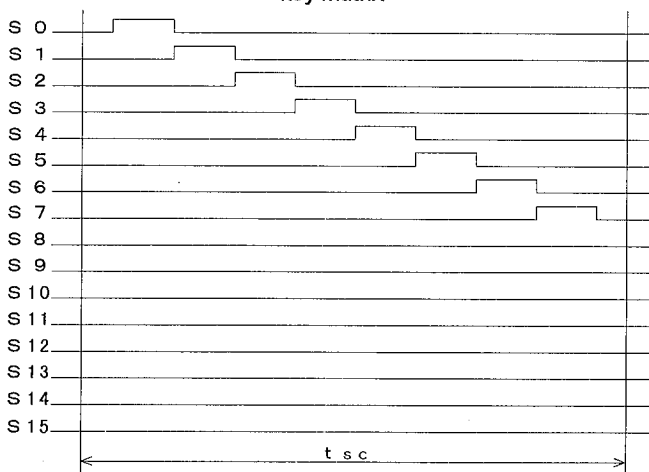
The key input detector function outputs "H" level during key is on at key scan.

(5-1) key condition vs key input terminal level

| key condition | input level |
|----------------|-------------|
| key pushed | "H" |
| not key pushed | "L" |



key matrix



key scan wave form

(6) SERIAL DATA TRANSMISSION

The NJU3423 provides the serial interface to communicate with external circuit. This interface circuit requires the external shift clock input and can operate the bi-directional (input/output) transmission synchronizing with clock.

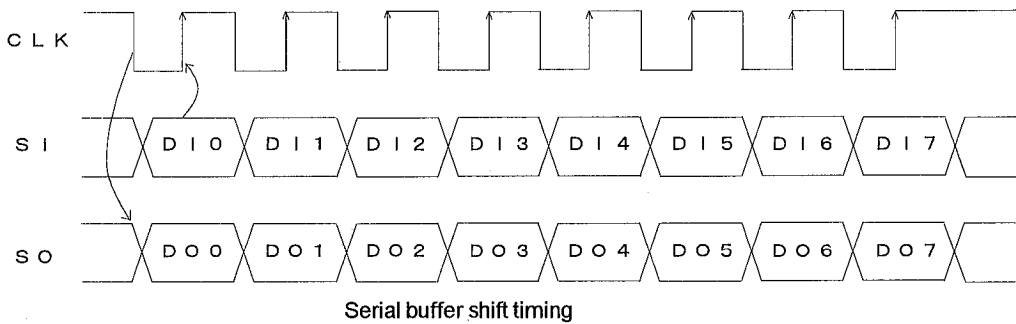
The serial data are grouped as a word which equals to byte(8 bits)for this device. The serial interface circuit is activated when the CS terminal is set to "L" level. While the CS is "L", the words of the serial data can be transmitted synchronizing the shift Clock (the CLK terminal) with the serial data input or output(the SI or SO terminal).

On the data input mode, the first transmitted word must be the address,the command or the I/O port output data. When the first word is the address data, the next words are the display data. When the first word is the command or I/O port output data, the next words are ineffective.

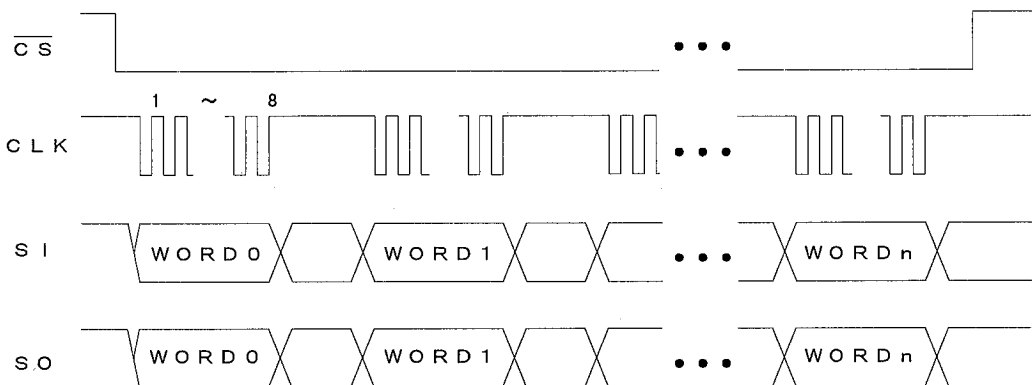
On the data output mode, the transmitted word consists of the key data in the lower 4 bits and the I/O port input data in the upper 4 bits (The MSB is invalid). The key data of the first word is the data by S0 scanning, the second word is the data by S1,--- finally scanning, the 8th word means the data by S7 scanning. The I/O port input data means the last status data.For getting all key matrix data(8 X 4 max.),the data transmission of the 8 words is required.

When the key data transmission is stopped at less than 8 words, the new key data transmission is start to read from the first (S0 scanning) word.

■ CLK and SI/SO TIMING CHART



■ SERIAL TRANSMISSION FORMAT



(6-1) SERIAL INPUT DATA

WORD 0

The address data

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | AD4 | AD3 | AD2 | AD1 | AD0 |

The I/O port output data

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 0 | D3 | D2 | D1 | D0 |

The LED port output data

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|----|----|------|------|------|------|
| 0 | 1 | 1 | 0 | LED3 | LED2 | LED1 | LED0 |

The command data

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|-----|-----|-----|-----|-----|-----|-----|
| 1 | DT2 | DT1 | DT0 | DSP | TM2 | TM1 | TMO |

The RESET data

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|----|----|----|----|----|----|
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |

WORD 1 ~ n Display data are required when WORD 0 = address data
 Any data are become ineffective when WORD 0 = not address data

(6-2) SERIAL OUTPUT DATA

WORD 0 ~ 7 (Key scan data)

Serial output data

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----|----|----|----|----|----|----|----|
| P3 | P2 | P1 | P0 | K3 | K2 | K1 | K0 |

WORD 8 ~ n Ineffectivedata

| | | | | |
|-----------------------------------|------------------|-----------------------------|-------------|---|
| Operating Voltage | V_{DD} | $-0.3 \sim +7.0$ | V | |
| Input Voltage | V_{IN} | $-0.3 \sim V_{DD}+0.3$ | V | |
| Output Voltage | V_{OUT} | $-0.3 \sim V_{DD}+0.3$ | V | |
| VFD Driving Voltage | V_{FDP} | $V_{DD}-40 \sim V_{DD}+0.3$ | V | Specified as V_{DD} . |
| "H"level Output Current | I_{OH} | -5 | mA | For a terminal except the display terminals |
| | I_{ODH1} | -15 | mA | For a terminal, $S_0 \sim S_7$ terminals only |
| | I_{ODH2} | -35 | mA | For a terminal, $T_0 \sim T_5$, $T_6/S_{15} \sim T_{10}/S_{11}$ Terminals only |
| "H" level Total Output Current | ΣI_{OH} | -40 | mA | Sum of the output terminal except the display Terminals |
| | ΣI_{ODH} | -100 | mA | Sum of the display Terminals |
| "L"level Output Current | I_{OLC} | 20 | mA | For a terminal, $LED_0 \sim LED_3$ Terminals |
| "L"level Total Output Current | ΣI_{OL} | 100 | mA | Sum of the Output Terminals |
| Operating Temperature Range | T_{opr} | $-30 \sim +80$ | $^{\circ}C$ | |
| Storage Temperature Range | T_{stg} | $-55 \sim +125$ | $^{\circ}C$ | |
| Power Dissipation | P_D | 400 | mW | QFP-44 Package |

Note) Decoupling capacitor should be connected between V_{DD} and V_{SS} , V_{FDP} and V_{SS} .

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{SS}=0V)

| PARAMETER | SYM. | CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
|---------------------------|------------------|--|---|------|---------------------|------|----|
| Operating Voltage | V _{DD} | V _{DD} Terminal | 4.5 | - | 5.5 | V | |
| "H" level Input Voltage | V _{IH1} | OSC, \overline{RST} , \overline{CS} , CLK, S ₁ , P ₀ ~ P ₃ Term. | 0.8V _{DD} | | | V | |
| | V _{IH2} | K ₀ ~ K ₃ Terminal | 0.4V _{DD} | | | V | |
| "L" level Input Voltage | V _{IL1} | OSC, \overline{RST} , \overline{CS} , CLK, S ₁ , P ₀ ~ P ₃ Term. | | | 0.2V _{DD} | V | |
| | V _{IL2} | K ₀ ~ K ₃ Terminal | | | 0.16V _{DD} | V | |
| "H" level Output Voltage | V _{OH1} | KD, S ₀ Terminal | V _{DD} =4.5V, I _{OH1} =-0.5mA | 4.0 | | V | |
| | V _{OH2} | | V _{DD} =4.5V, I _{OH2} =-1.2mA | 3.5 | | V | |
| "L" level Output Voltage | V _{OL1} | KD, S ₀ , P ₀ ~ P ₃ Terminal | V _{DD} =4.5V, I _{OL1} = 1.8mA | | 0.4 | V | |
| | V _{OL2} | | V _{DD} =4.5V, I _{OL2} = 3.6mA | | 0.6 | V | |
| | V _{OL3} | LED ₀ ~ LED ₃ Term. | V _{DD} =4.5V, I _{OL3} = 10mA | | 0.4 | V | |
| Input Off Leak Current | I _{Iz} | \overline{CS} , CLK, S ₁ Term. | V _{DD} =5.5V, V _I =0 or 5.5V | | ±1 | μA | |
| Display Output Current | I _{OH1} | S ₀ ~ S ₁₀ Term. | V _{DD} =4.5V, V _{OH} =V _{DD} -2.5V | | -7 | mA | |
| | I _{OH2} | S ₁₁ /T ₁₀ ~ S ₁₅ /T ₆ , T ₀ ~ T ₅ Terminal | | | -15 | mA | |
| Pull-up resistance | R _{UR} | \overline{RST} Terminal | V _{DD} =5.0V, V _I =V _{SS} | 140 | 260 | KΩ | |
| | R _{UP} | LED ₀ ~ LED ₃ , P ₀ ~ P ₃ Terminal | V _{DD} =5.0V, V _I =V _{SS} | 10 | 20 | KΩ | |
| Pull-Down resistance | R _{DK} | K ₀ ~ K ₃ Terminal | V _{DD} =5.0V, V _I =V _{DD} | 20 | 50 | KΩ | |
| | R _{DST} | S ₁₁ /T ₁₀ ~ S ₁₅ /T ₆ , T ₀ ~ T ₅ , S ₀ ~ S ₁₀ Terminal | V _{DD} =5.0V, V _O =V _{DD} , V _{FDP} =V _{DD} -40V | 70 | 200 | KΩ | |
| Logic Operating Current | I _{DD1} | V _{SS} Terminal | V _{DD} =5.0V, CR Oscillation, Output Open, K ₀ ~ K ₃ , P ₀ ~ P ₃ \overline{RST} Term. Open, All Segment or Timing Output is OFF | | 2 | 4 | mA |
| Display Operating Current | I _{DD2} | V _{FDP} Terminal | V _{DD} =5.0V, V _{FDP} =V _{DD} -40V Output Open except S ₁₁ /T ₁₀ ~ S ₁₅ /T ₆ , T ₀ ~ T ₅ , S ₀ ~ S ₁₀ , All Segment or Timing Output is ON | | 7 | 10 | mA |

■ AC Characteristics

(Ta=25°C, V_{DD}=4.5V ~ 5.5V, V_{SS}=0V)

| PARAMETER | SYM. | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|--------------------------------------|--|------|------|--------------------|------|
| Oscillation Frequency External Frequency | f _{CR} | Fig.1 | 3 | 5.5 | 8 | MHz |
| External Clock Rise / Fall Time | t _{CLH} t _{CLL} | Fig.1 | | | 20 | ns |
| Serial Input Setup Time | t _{SIS} | Fig.2 | 60 | | | ns |
| Serial Input Hold Time | t _{SIH} | Fig.2 | 10 | | | ns |
| Serial Output Delay Time | t _{SOD} | Fig.2 Load=50pF | | | 120 | ns |
| Shift Clock Frequency | f _{CLK} | Fig.3 | | | f _{CR} /3 | MHz |
| Shift Clock Interval Time | t _{CLKI} | Fig.3 | 10 | | | μs |
| Minimum Blanking Time | t _{BK} | Fig.4 @f _{CR} =4MHz | 20 | | 30 | μs |
| "L" level Time | t _{KSL} | Fig.5 @f _{CR} =4MHz, Key scan | 20 | | | μs |
| "H" level Time | t _{KST} | Fig.5 @f _{CR} =4MHz, Key scan | 20 | | 30 | μs |
| Reset Pulse Width | t _{RST} | | 10 | | | μs |
| Power Rise Time | t _R | Fig.6 | 0.05 | | 50 | ms |

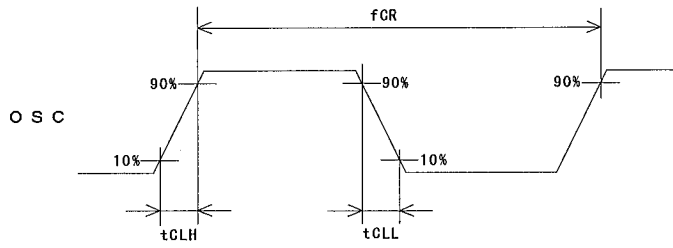


Fig.1

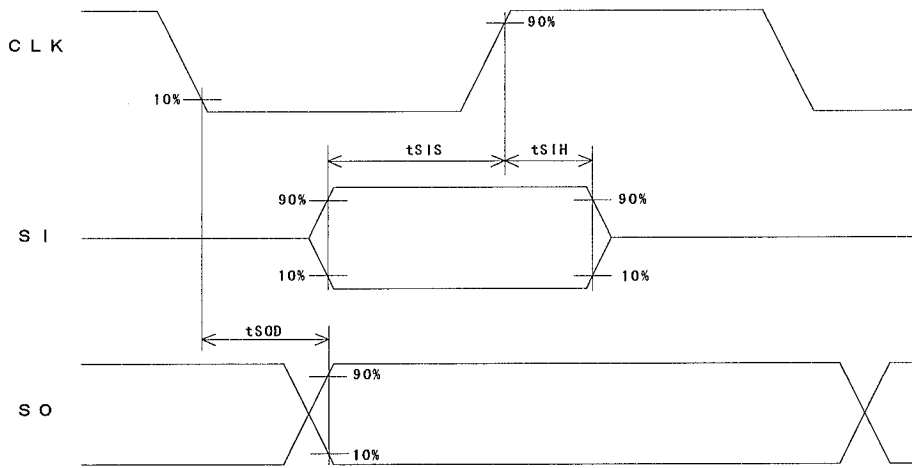


Fig.2

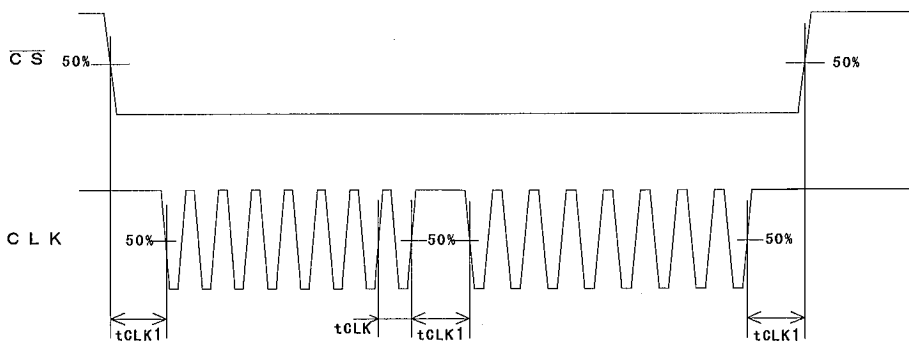


Fig.3

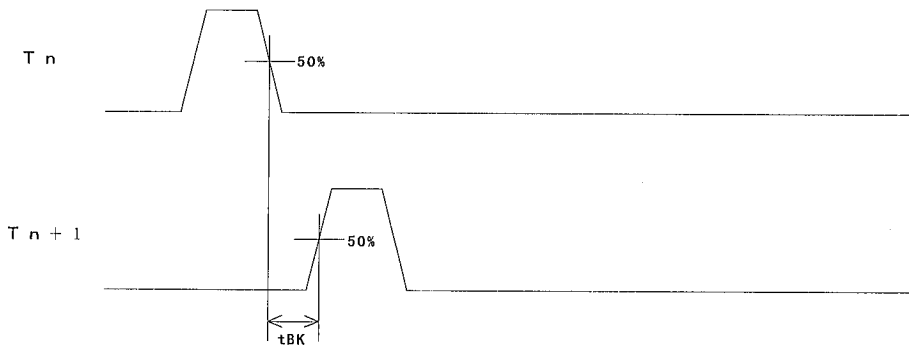


Fig.4

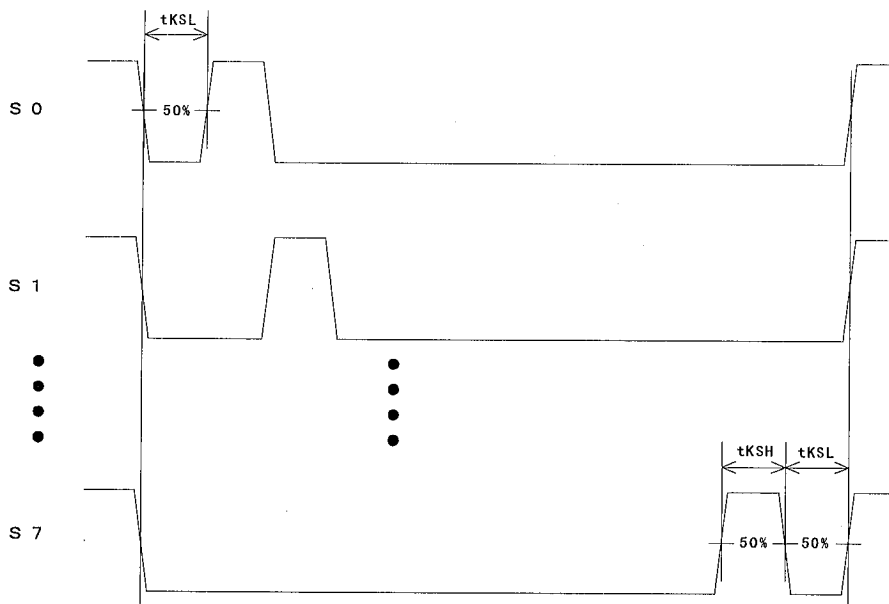


Fig.5

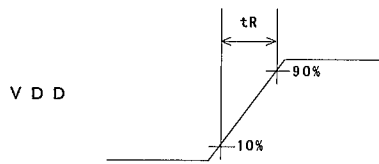
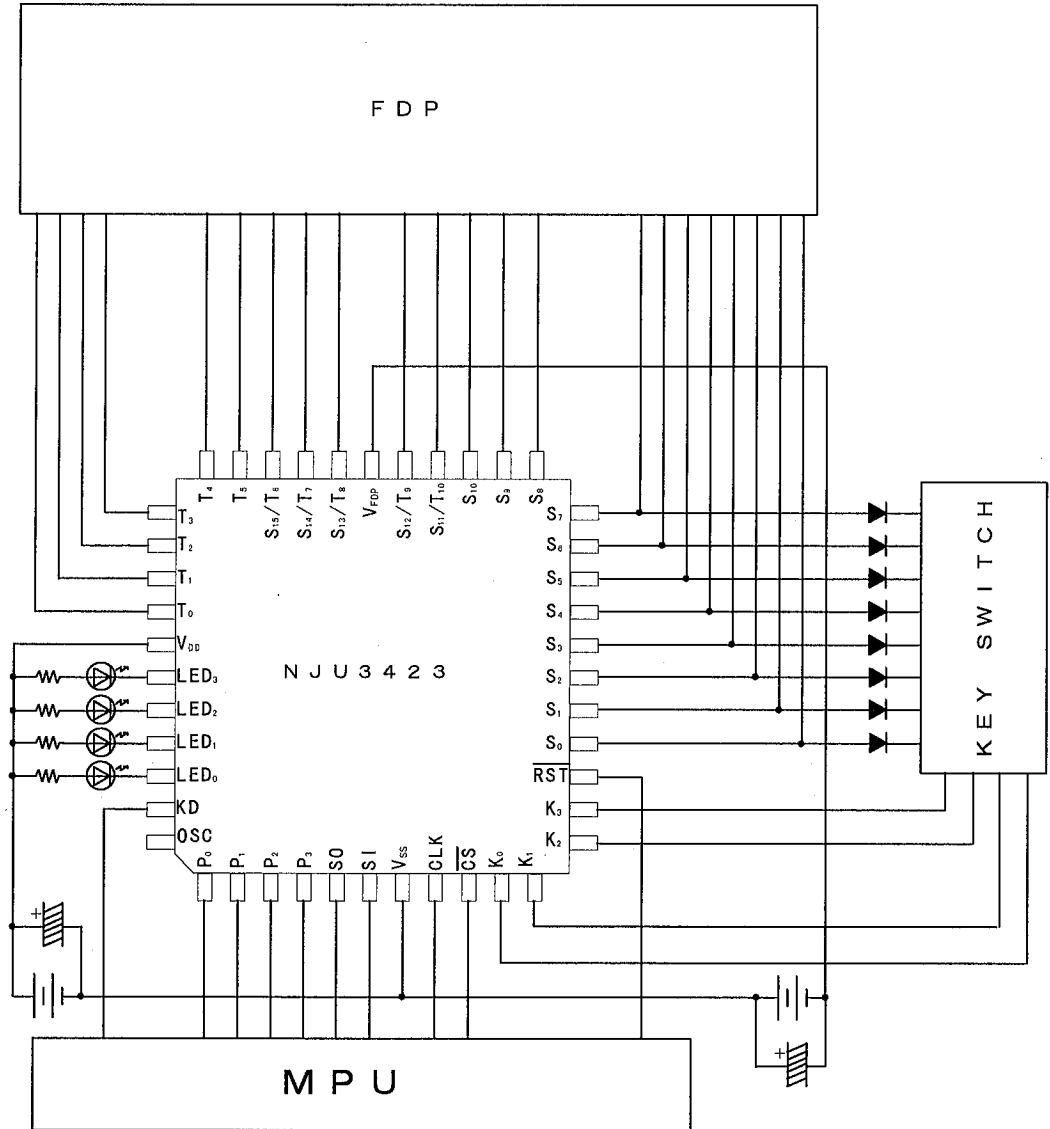


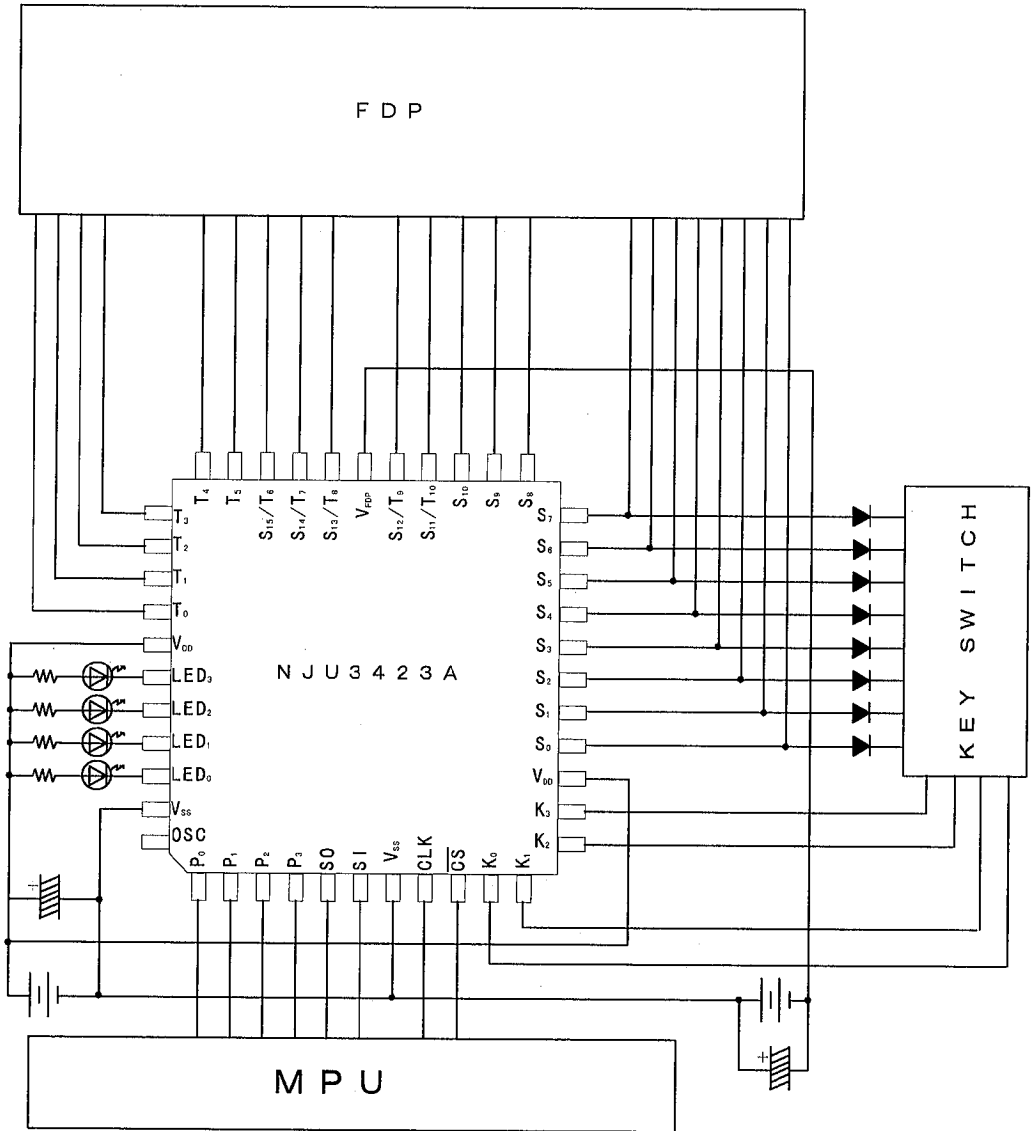
Fig.6

■ APPLICATION CIRCUIT

(1) NJU3423



(2) NJU3423A



MEMO

[CAUTION]

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