

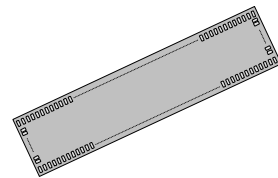
## 128COMMON x 80RGB LCD DRIVER FOR 4,096-COLOR STN DISPLAY

### ■ GENERAL DESCRIPTION

The NJU6815 is a 128COMMON x 80RGB LCD driver for 4,096-color STN display. It contains common drivers, RGB drivers, a serial and a parallel MPU interface circuit, an internal LCD power supply, grayscale palettes and 122,880-bit display data RAM. The segment drivers for RGB (Red, Green, Blue) independently produce optimum 16 grayscales from a built-in 32-grayscale palette, and the LSI achieves 4,096 colors (16x16x16). And the LSI features the display-rotation function which rotates an on-screen image in the unit of 90 degrees.

In addition, the NJU6815 operates with a low voltage of 1.7V and a low operating current, therefore it is ideally suited for battery-powered handheld applications.

### ■ PACKAGE



BUMP CHIP

### ■ FEATURES

- 4,096-color STN LCD driver
- Built-in LCD Drivers : 128-common Drivers x 80RGB Drivers (240-segment Drivers in B&W)
- Built-in Display Data RAM (DDRAM) : 122,880 bits for Graphic Display
- Programmable Display Mode
  - Variable 16-grayscale Mode : 4,096 Colors
  - Variable 8-grayscale Mode : 256 Colors
  - Fixed 8-grayscale Mode : 256 Colors
  - B&W Mode : Black & White
- 8-/16-bit Parallel Interface Selectable
- 8-/16-bit Bus Length for Display Data Selectable
- 3-/4-line Serial Interface Selectable
- Programmable Duty Ratio and Bias Ratio
- Programmable Internal Voltage Booster : Maximum 6 times
- Programmable Contrast Control : 128-step Electrical Variable Resistor (EVR)
- Various Useful Instructions
- Display-rotation Function / Mirror-inversion Function
- Low Operating Current : 450uA Typical at  $V_{DD}=3V$ , 4-time Boost, Checker Flag Display
- Low Logic Voltage : 1.7V to 3.3V
- Wide LCD Voltage Range : 5.0V to 18.0V
- C-MOS Technology
- Slim Chip for COG
- Package : Bump Chip / TCP

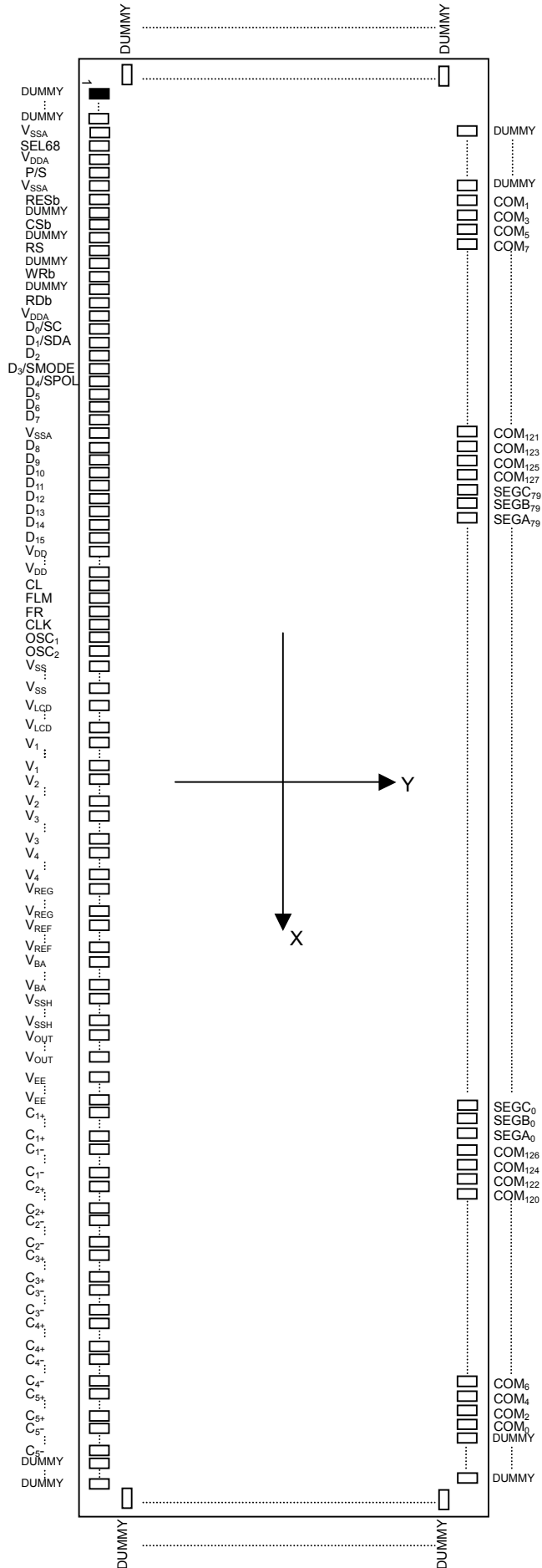
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## ■ PAD LOCATION



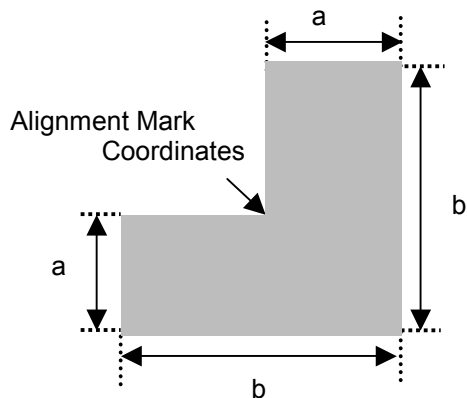
Chip Center :X=0um, Y=0um  
 Chip Size :X=16.70mm, Y= 2.64mm  
 Chip Thickness :625um ± 25um  
 Bump Pitch :42um(Min)  
 Bump Space :15um  
 Bump Size :24±3um x 140±5um  
 Bump Height :17.5um(Typical)  
 Bump Material :Au

NOTE1) Multiple PADs with successive numbers are internally connected.

NOTE2) Dummy PADs, symbolized with DUMMY, are electrically open.

NOTE3) The purpose of this drawing is to show the order of PADs. Use "PAD CORDINATE TABLE 1 to 4" for design.

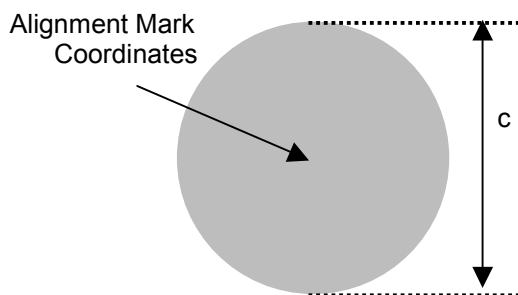
## Alignment Mark 1



a : 25 $\mu$ m  
b : 50 $\mu$ m

Alignment Mark Coordinates  
( -8168, 1138 )  
( 8168, -1138 )

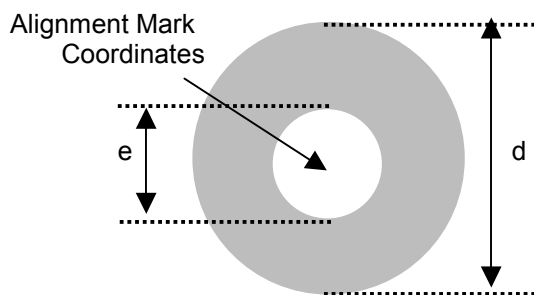
## Alignment Mark 2



c : 50 $\mu$ m

Alignment Mark Coordinates  
( 7982, -1115 )

## Alignment Mark 3



d : 50 $\mu$ m  
e : 20 $\mu$ m

Alignment Mark Coordinates  
( -7982, -1115 )

## ■ PAD COORDINATES 1

Chip Size 16,700μm x 2,640μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X(μm)	Y(μm)
1	DMY <sub>0</sub>	-7875.00	-1115.00
2	DMY <sub>1</sub>	-7833.00	-1115.00
3	DMY <sub>2</sub>	-7791.00	-1115.00
4	V <sub>SSA</sub>	-7749.00	-1115.00
5	V <sub>SSA</sub>	-7707.00	-1115.00
6	DMY <sub>3</sub>	-7665.00	-1115.00
7	SEL68	-7623.00	-1115.00
8	SEL68	-7581.00	-1115.00
9	DMY <sub>4</sub>	-7539.00	-1115.00
10	V <sub>DDA</sub>	-7497.00	-1115.00
11	V <sub>DDA</sub>	-7455.00	-1115.00
12	DMY <sub>5</sub>	-7413.00	-1115.00
13	P/S	-7371.00	-1115.00
14	P/S	-7329.00	-1115.00
15	DMY <sub>6</sub>	-7287.00	-1115.00
16	V <sub>SSA</sub>	-7245.00	-1115.00
17	V <sub>SSA</sub>	-7203.00	-1115.00
18	DMY <sub>7</sub>	-7161.00	-1115.00
19	RESB	-7119.00	-1115.00
20	RESB	-7077.00	-1115.00
21	DMY <sub>8</sub>	-7035.00	-1115.00
22	CSB	-6993.00	-1115.00
23	CSB	-6951.00	-1115.00
24	DMY <sub>9</sub>	-6909.00	-1115.00
25	RS	-6867.00	-1115.00
26	RS	-6825.00	-1115.00
27	DMY <sub>10</sub>	-6783.00	-1115.00
28	WRB	-6741.00	-1115.00
29	WRB	-6699.00	-1115.00
30	DMY <sub>11</sub>	-6657.00	-1115.00
31	RDB	-6615.00	-1115.00
32	RDB	-6573.00	-1115.00
33	DMY <sub>12</sub>	-6531.00	-1115.00
34	V <sub>DDA</sub>	-6489.00	-1115.00
35	V <sub>DDA</sub>	-6447.00	-1115.00
36	D <sub>0</sub>	-6321.00	-1115.00
37	D <sub>0</sub>	-6279.00	-1115.00
38	D <sub>1</sub>	-6153.00	-1115.00
39	D <sub>1</sub>	-6111.00	-1115.00
40	D <sub>2</sub>	-5985.00	-1115.00
41	D <sub>2</sub>	-5943.00	-1115.00
42	D <sub>3</sub>	-5817.00	-1115.00
43	D <sub>3</sub>	-5775.00	-1115.00
44	D <sub>4</sub>	-5649.00	-1115.00
45	D <sub>4</sub>	-5607.00	-1115.00
46	D <sub>5</sub>	-5481.00	-1115.00
47	D <sub>5</sub>	-5439.00	-1115.00
48	D <sub>6</sub>	-5313.00	-1115.00
49	D <sub>6</sub>	-5271.00	-1115.00
50	D <sub>7</sub>	-5145.00	-1115.00
51	D <sub>7</sub>	-5103.00	-1115.00
52	V <sub>SSA</sub>	-4977.00	-1115.00
53	V <sub>SSA</sub>	-4935.00	-1115.00
54	D <sub>8</sub>	-4809.00	-1115.00
55	D <sub>8</sub>	-4767.00	-1115.00
56	D <sub>9</sub>	-4641.00	-1115.00
57	D <sub>9</sub>	-4599.00	-1115.00
58	D <sub>10</sub>	-4473.00	-1115.00
59	D <sub>10</sub>	-4431.00	-1115.00
60	D <sub>11</sub>	-4305.00	-1115.00

No.	PAD NAME	X(μm)	Y(μm)
61	D <sub>11</sub>	-4263.00	-1115.00
62	D <sub>12</sub>	-4137.00	-1115.00
63	D <sub>12</sub>	-4095.00	-1115.00
64	D <sub>13</sub>	-3969.00	-1115.00
65	D <sub>13</sub>	-3927.00	-1115.00
66	D <sub>14</sub>	-3801.00	-1115.00
67	D <sub>14</sub>	-3759.00	-1115.00
68	D <sub>15</sub>	-3633.00	-1115.00
69	D <sub>15</sub>	-3591.00	-1115.00
70	V <sub>DD</sub>	-3465.00	-1115.00
71	V <sub>DD</sub>	-3423.00	-1115.00
72	V <sub>DD</sub>	-3381.00	-1115.00
73	V <sub>DD</sub>	-3339.00	-1115.00
74	V <sub>DD</sub>	-3297.00	-1115.00
75	V <sub>DD</sub>	-3255.00	-1115.00
76	V <sub>DD</sub>	-3213.00	-1115.00
77	V <sub>DD</sub>	-3171.00	-1115.00
78	V <sub>DD</sub>	-3129.00	-1115.00
79	CL	-2961.00	-1115.00
80	CL	-2919.00	-1115.00
81	FLM	-2793.00	-1115.00
82	FLM	-2751.00	-1115.00
83	FR	-2625.00	-1115.00
84	FR	-2583.00	-1115.00
85	CLK	-2457.00	-1115.00
86	CLK	-2415.00	-1115.00
87	DMY <sub>13</sub>	-2289.00	-1115.00
88	OSC1	-2247.00	-1115.00
89	OSC1	-2205.00	-1115.00
90	DMY <sub>14</sub>	-2163.00	-1115.00
91	OSC2	-2037.00	-1115.00
92	OSC2	-1995.00	-1115.00
93	V <sub>SS</sub>	-1869.00	-1115.00
94	V <sub>SS</sub>	-1827.00	-1115.00
95	V <sub>SS</sub>	-1785.00	-1115.00
96	V <sub>SS</sub>	-1743.00	-1115.00
97	V <sub>SS</sub>	-1701.00	-1115.00
98	V <sub>SS</sub>	-1659.00	-1115.00
99	V <sub>SS</sub>	-1617.00	-1115.00
100	V <sub>SS</sub>	-1575.00	-1115.00
101	V <sub>SS</sub>	-1533.00	-1115.00
102	DMY <sub>15</sub>	-1407.00	-1115.00
103	V <sub>LCD</sub>	-1281.00	-1115.00
104	V <sub>LCD</sub>	-1239.00	-1115.00
105	V <sub>LCD</sub>	-1197.00	-1115.00
106	V <sub>LCD</sub>	-1155.00	-1115.00
107	V <sub>LCD</sub>	-1113.00	-1115.00
108	V <sub>LCD</sub>	-1071.00	-1115.00
109	V <sub>LCD</sub>	-1029.00	-1115.00
110	V <sub>LCD</sub>	-987.00	-1115.00
111	V <sub>LCD</sub>	-945.00	-1115.00
112	DMY <sub>16</sub>	-903.00	-1115.00
113	V <sub>1</sub>	-861.00	-1115.00
114	V <sub>1</sub>	-819.00	-1115.00
115	V <sub>1</sub>	-777.00	-1115.00
116	V <sub>1</sub>	-735.00	-1115.00
117	V <sub>1</sub>	-693.00	-1115.00
118	V <sub>1</sub>	-651.00	-1115.00
119	V <sub>1</sub>	-609.00	-1115.00
120	V <sub>1</sub>	-567.00	-1115.00

No.	PAD NAME	X(μm)	Y(μm)
121	V <sub>1</sub>	-525.00	-1115.00
122	V <sub>2</sub>	-399.00	-1115.00
123	V <sub>2</sub>	-357.00	-1115.00
124	V <sub>2</sub>	-315.00	-1115.00
125	V <sub>2</sub>	-273.00	-1115.00
126	V <sub>2</sub>	-231.00	-1115.00
127	V <sub>2</sub>	-189.00	-1115.00
128	V <sub>2</sub>	-147.00	-1115.00
129	V <sub>2</sub>	-105.00	-1115.00
130	V <sub>2</sub>	-63.00	-1115.00
131	DMY <sub>17</sub>	-21.00	-1115.00
132	V <sub>3</sub>	21.00	-1115.00
133	V <sub>3</sub>	63.00	-1115.00
134	V <sub>3</sub>	105.00	-1115.00
135	V <sub>3</sub>	147.00	-1115.00
136	V <sub>3</sub>	189.00	-1115.00
137	V <sub>3</sub>	231.00	-1115.00
138	V <sub>3</sub>	273.00	-1115.00
139	V <sub>3</sub>	315.00	-1115.00
140	V <sub>3</sub>	357.00	-1115.00
141	V <sub>4</sub>	483.00	-1115.00
142	V <sub>4</sub>	525.00	-1115.00
143	V <sub>4</sub>	567.00	-1115.00
144	V <sub>4</sub>	609.00	-1115.00
145	V <sub>4</sub>	651.00	-1115.00
146	V <sub>4</sub>	693.00	-1115.00
147	V <sub>4</sub>	735.00	-1115.00
148	V <sub>4</sub>	777.00	-1115.00
149	V <sub>4</sub>	819.00	-1115.00
150	DMY <sub>18</sub>	861.00	-1115.00
151	V <sub>REG</sub>	903.00	-1115.00
152	V <sub>REG</sub>	945.00	-1115.00
153	V <sub>REG</sub>	987.00	-1115.00
154	V <sub>REG</sub>	1029.00	-1115.00
155	V <sub>REG</sub>	1071.00	-1115.00
156	V <sub>REG</sub>	1113.00	-1115.00
157	V <sub>REG</sub>	1155.00	-1115.00
158	V <sub>REG</sub>	1197.00	-1115.00
159	V <sub>REG</sub>	1239.00	-1115.00
160	DMY <sub>19</sub>	1281.00	-1115.00
161	V <sub>REF</sub>	1323.00	-1115.00
162	V <sub>REF</sub>	1365.00	-1115.00
163	V <sub>REF</sub>	1407.00	-1115.00
164	V <sub>REF</sub>	1449.00	-1115.00
165	V <sub>REF</sub>	1491.00	-1115.00
166	V <sub>REF</sub>	1533.00	-1115.00
167	V <sub>REF</sub>	1575.00	-1115.00
168	V <sub>REF</sub>	1617.00	-1115.00
169	V <sub>REF</sub>	1659.00	-1115.00
170	DMY <sub>20</sub>	1701.00	-1115.00
171	V <sub>BA</sub>	1743.00	-1115.00
172	V <sub>BA</sub>	1785.00	-1115.00
173	V <sub>BA</sub>	1827.00	-1115.00
174	V <sub>BA</sub>	1869.00	-1115.00
175	V <sub>BA</sub>	1911.00	-1115.00
176	V <sub>BA</sub>	1953.00	-1115.00
177	V <sub>BA</sub>	1995.00	-1115.00
178	V <sub>BA</sub>	2037.00	-1115.00
179	V <sub>BA</sub>	2079.00	-1115.00
180	DMY <sub>21</sub>	2121.00	-1115.00

## ■ PAD COORDINATES 2

Chip Size 16,700 $\mu$ m x 2,640 $\mu$ m (Chip Center 0 $\mu$ m x 0 $\mu$ m)

No.	PAD NAME	X( $\mu$ m)	Y( $\mu$ m)
181	V <sub>SSH</sub>	2163.00	-1115.00
182	V <sub>SSH</sub>	2205.00	-1115.00
183	V <sub>SSH</sub>	2247.00	-1115.00
184	V <sub>SSH</sub>	2289.00	-1115.00
185	V <sub>SSH</sub>	2331.00	-1115.00
186	V <sub>SSH</sub>	2373.00	-1115.00
187	V <sub>SSH</sub>	2415.00	-1115.00
188	V <sub>SSH</sub>	2457.00	-1115.00
189	V <sub>SSH</sub>	2499.00	-1115.00
190	V <sub>OUT</sub>	2667.00	-1115.00
191	V <sub>OUT</sub>	2709.00	-1115.00
192	V <sub>OUT</sub>	2751.00	-1115.00
193	V <sub>OUT</sub>	2793.00	-1115.00
194	V <sub>OUT</sub>	2835.00	-1115.00
195	V <sub>OUT</sub>	2877.00	-1115.00
196	V <sub>OUT</sub>	2919.00	-1115.00
197	V <sub>OUT</sub>	2961.00	-1115.00
198	V <sub>OUT</sub>	3003.00	-1115.00
199	V <sub>EE</sub>	3171.00	-1115.00
200	V <sub>EE</sub>	3213.00	-1115.00
201	V <sub>EE</sub>	3255.00	-1115.00
202	V <sub>EE</sub>	3297.00	-1115.00
203	V <sub>EE</sub>	3339.00	-1115.00
204	V <sub>EE</sub>	3381.00	-1115.00
205	V <sub>EE</sub>	3423.00	-1115.00
206	V <sub>EE</sub>	3465.00	-1115.00
207	V <sub>EE</sub>	3507.00	-1115.00
208	C <sub>1+</sub>	3633.00	-1115.00
209	C <sub>1+</sub>	3675.00	-1115.00
210	C <sub>1+</sub>	3717.00	-1115.00
211	C <sub>1+</sub>	3759.00	-1115.00
212	C <sub>1+</sub>	3801.00	-1115.00
213	C <sub>1+</sub>	3843.00	-1115.00
214	C <sub>1+</sub>	3885.00	-1115.00
215	C <sub>1+</sub>	3927.00	-1115.00
216	C <sub>1+</sub>	3969.00	-1115.00
217	DMY <sub>22</sub>	4011.00	-1115.00
218	C <sub>1-</sub>	4053.00	-1115.00
219	C <sub>1-</sub>	4095.00	-1115.00
220	C <sub>1-</sub>	4137.00	-1115.00
221	C <sub>1-</sub>	4179.00	-1115.00
222	C <sub>1-</sub>	4221.00	-1115.00
223	C <sub>1-</sub>	4263.00	-1115.00
224	C <sub>1-</sub>	4305.00	-1115.00
225	C <sub>1-</sub>	4347.00	-1115.00
226	C <sub>1-</sub>	4389.00	-1115.00
227	DMY <sub>23</sub>	4431.00	-1115.00
228	C <sub>2+</sub>	4473.00	-1115.00
229	C <sub>2+</sub>	4515.00	-1115.00
230	C <sub>2+</sub>	4557.00	-1115.00
231	C <sub>2+</sub>	4599.00	-1115.00
232	C <sub>2+</sub>	4641.00	-1115.00
233	C <sub>2+</sub>	4683.00	-1115.00
234	C <sub>2+</sub>	4725.00	-1115.00
235	C <sub>2+</sub>	4767.00	-1115.00
236	C <sub>2+</sub>	4809.00	-1115.00
237	DMY <sub>24</sub>	4851.00	-1115.00
238	C <sub>2-</sub>	4893.00	-1115.00
239	C <sub>2-</sub>	4935.00	-1115.00
240	C <sub>2-</sub>	4977.00	-1115.00

No.	PAD NAME	X( $\mu$ m)	Y( $\mu$ m)
241	C <sub>2-</sub>	5019.00	-1115.00
242	C <sub>2-</sub>	5061.00	-1115.00
243	C <sub>2-</sub>	5103.00	-1115.00
244	C <sub>2-</sub>	5145.00	-1115.00
245	C <sub>2-</sub>	5187.00	-1115.00
246	C <sub>2-</sub>	5229.00	-1115.00
247	DMY <sub>25</sub>	5271.00	-1115.00
248	C <sub>3+</sub>	5313.00	-1115.00
249	C <sub>3+</sub>	5355.00	-1115.00
250	C <sub>3+</sub>	5397.00	-1115.00
251	C <sub>3+</sub>	5439.00	-1115.00
252	C <sub>3+</sub>	5481.00	-1115.00
253	C <sub>3+</sub>	5523.00	-1115.00
254	C <sub>3+</sub>	5565.00	-1115.00
255	C <sub>3+</sub>	5607.00	-1115.00
256	C <sub>3+</sub>	5649.00	-1115.00
257	DMY <sub>26</sub>	5691.00	-1115.00
258	C <sub>3-</sub>	5733.00	-1115.00
259	C <sub>3-</sub>	5775.00	-1115.00
260	C <sub>3-</sub>	5817.00	-1115.00
261	C <sub>3-</sub>	5859.00	-1115.00
262	C <sub>3-</sub>	5901.00	-1115.00
263	C <sub>3-</sub>	5943.00	-1115.00
264	C <sub>3-</sub>	5985.00	-1115.00
265	C <sub>3-</sub>	6027.00	-1115.00
266	C <sub>3-</sub>	6069.00	-1115.00
267	DMY <sub>27</sub>	6111.00	-1115.00
268	C <sub>4+</sub>	6153.00	-1115.00
269	C <sub>4+</sub>	6195.00	-1115.00
270	C <sub>4+</sub>	6237.00	-1115.00
271	C <sub>4+</sub>	6279.00	-1115.00
272	C <sub>4+</sub>	6321.00	-1115.00
273	C <sub>4+</sub>	6363.00	-1115.00
274	C <sub>4+</sub>	6405.00	-1115.00
275	C <sub>4+</sub>	6447.00	-1115.00
276	C <sub>4+</sub>	6489.00	-1115.00
277	DMY <sub>28</sub>	6531.00	-1115.00
278	C <sub>4-</sub>	6573.00	-1115.00
279	C <sub>4-</sub>	6615.00	-1115.00
280	C <sub>4-</sub>	6657.00	-1115.00
281	C <sub>4-</sub>	6699.00	-1115.00
282	C <sub>4-</sub>	6741.00	-1115.00
283	C <sub>4-</sub>	6783.00	-1115.00
284	C <sub>4-</sub>	6825.00	-1115.00
285	C <sub>4-</sub>	6867.00	-1115.00
286	C <sub>4-</sub>	6909.00	-1115.00
287	DMY <sub>29</sub>	6951.00	-1115.00
288	C <sub>5+</sub>	6993.00	-1115.00
289	C <sub>5+</sub>	7035.00	-1115.00
290	C <sub>5+</sub>	7077.00	-1115.00
291	C <sub>5+</sub>	7119.00	-1115.00
292	C <sub>5+</sub>	7161.00	-1115.00
293	C <sub>5+</sub>	7203.00	-1115.00
294	C <sub>5+</sub>	7245.00	-1115.00
295	C <sub>5+</sub>	7287.00	-1115.00
296	C <sub>5+</sub>	7329.00	-1115.00
297	DMY <sub>30</sub>	7371.00	-1115.00
298	C <sub>5-</sub>	7413.00	-1115.00
299	C <sub>5-</sub>	7455.00	-1115.00
300	C <sub>5-</sub>	7497.00	-1115.00

No.	PAD NAME	X( $\mu$ m)	Y( $\mu$ m)
301	C <sub>5-</sub>	7539.00	-1115.00
302	C <sub>5-</sub>	7581.00	-1115.00
303	C <sub>5-</sub>	7623.00	-1115.00
304	C <sub>5-</sub>	7665.00	-1115.00
305	C <sub>5-</sub>	7707.00	-1115.00
306	C <sub>5-</sub>	7749.00	-1115.00
307	DMY <sub>31</sub>	7791.00	-1115.00
308	DMY <sub>32</sub>	7833.00	-1115.00
309	DMY <sub>33</sub>	7875.00	-1115.00
310	DMY <sub>34</sub>	8145.00	-1035.00
311	DMY <sub>35</sub>	8145.00	-993.00
312	DMY <sub>35</sub>	8145.00	-951.00
313	DMY <sub>35</sub>	8145.00	-909.00
314	DMY <sub>36</sub>	8145.00	-867.00
315	DMY <sub>37</sub>	8001.00	1115.00
316	DMY <sub>38</sub>	7959.00	1115.00
317	DMY <sub>39</sub>	7917.00	1115.00
318	DMY <sub>40</sub>	7875.00	1115.00
319	COM <sub>0</sub>	7833.00	1115.00
320	COM <sub>2</sub>	7791.00	1115.00
321	COM <sub>4</sub>	7749.00	1115.00
322	COM <sub>6</sub>	7707.00	1115.00
323	COM <sub>8</sub>	7665.00	1115.00
324	COM <sub>10</sub>	7623.00	1115.00
325	COM <sub>12</sub>	7581.00	1115.00
326	COM <sub>14</sub>	7539.00	1115.00
327	COM <sub>16</sub>	7497.00	1115.00
328	COM <sub>18</sub>	7455.00	1115.00
329	COM <sub>20</sub>	7413.00	1115.00
330	COM <sub>22</sub>	7371.00	1115.00
331	COM <sub>24</sub>	7329.00	1115.00
332	COM <sub>26</sub>	7287.00	1115.00
333	COM <sub>28</sub>	7245.00	1115.00
334	COM <sub>30</sub>	7203.00	1115.00
335	COM <sub>32</sub>	7161.00	1115.00
336	COM <sub>34</sub>	7119.00	1115.00
337	COM <sub>36</sub>	7077.00	1115.00
338	COM <sub>38</sub>	7035.00	1115.00
339	COM <sub>40</sub>	6993.00	1115.00
340	COM <sub>42</sub>	6951.00	1115.00
341	COM <sub>44</sub>	6909.00	1115.00
342	COM <sub>46</sub>	6867.00	1115.00
343	COM <sub>48</sub>	6825.00	1115.00
344	COM <sub>50</sub>	6783.00	1115.00
345	COM <sub>52</sub>	6741.00	1115.00
346	COM <sub>54</sub>	6699.00	1115.00
347	COM <sub>56</sub>	6657.00	1115.00
348	COM <sub>58</sub>	6615.00	1115.00
349	COM <sub>60</sub>	6573.00	1115.00
350	COM <sub>62</sub>	6531.00	1115.00
351	COM <sub>64</sub>	6489.00	1115.00
352	COM <sub>66</sub>	6447.00	1115.00
353	COM <sub>68</sub>	6405.00	1115.00
354	COM <sub>70</sub>	6363.00	1115.00
355	COM <sub>72</sub>	6321.00	1115.00
356	COM <sub>74</sub>	6279.00	1115.00
357	COM <sub>76</sub>	6237.00	1115.00
358	COM <sub>78</sub>	6195.00	1115.00
359	COM <sub>80</sub>	6153.00	1115.00
360	COM <sub>82</sub>	6111.00	1115.00



## ■ PAD COORDINATES 3

Chip Size 16,700μm x 2,640μm (Chip Center 0μm x 0μm )

No.	PAD NAME	X (μm)	Y (μm)
361	COM <sub>84</sub>	6069.00	1115.00
362	COM <sub>86</sub>	6027.00	1115.00
363	COM <sub>88</sub>	5985.00	1115.00
364	COM <sub>90</sub>	5943.00	1115.00
365	COM <sub>92</sub>	5901.00	1115.00
366	COM <sub>94</sub>	5859.00	1115.00
367	COM <sub>96</sub>	5817.00	1115.00
368	COM <sub>98</sub>	5775.00	1115.00
369	COM <sub>100</sub>	5733.00	1115.00
370	COM <sub>102</sub>	5691.00	1115.00
371	COM <sub>104</sub>	5649.00	1115.00
372	COM <sub>106</sub>	5607.00	1115.00
373	COM <sub>108</sub>	5565.00	1115.00
374	COM <sub>110</sub>	5523.00	1115.00
375	COM <sub>112</sub>	5481.00	1115.00
376	COM <sub>114</sub>	5439.00	1115.00
377	COM <sub>116</sub>	5397.00	1115.00
378	COM <sub>118</sub>	5355.00	1115.00
379	COM <sub>120</sub>	5313.00	1115.00
380	COM <sub>122</sub>	5271.00	1115.00
381	COM <sub>124</sub>	5229.00	1115.00
382	COM <sub>126</sub>	5187.00	1115.00
383	DMY <sub>41</sub>	5145.00	1115.00
384	DMY <sub>42</sub>	5103.00	1115.00
385	DMY <sub>43</sub>	5061.00	1115.00
386	SEGA <sub>0</sub>	5019.00	1115.00
387	SEGB <sub>0</sub>	4977.00	1115.00
388	SEGC <sub>0</sub>	4935.00	1115.00
389	SEGA <sub>1</sub>	4893.00	1115.00
390	SEGB <sub>1</sub>	4851.00	1115.00
391	SEGC <sub>1</sub>	4809.00	1115.00
392	SEGA <sub>2</sub>	4767.00	1115.00
393	SEGB <sub>2</sub>	4725.00	1115.00
394	SEGC <sub>2</sub>	4683.00	1115.00
395	SEGA <sub>3</sub>	4641.00	1115.00
396	SEGB <sub>3</sub>	4599.00	1115.00
397	SEGC <sub>3</sub>	4557.00	1115.00
398	SEGA <sub>4</sub>	4515.00	1115.00
399	SEGB <sub>4</sub>	4473.00	1115.00
400	SEGC <sub>4</sub>	4431.00	1115.00
401	SEGA <sub>5</sub>	4389.00	1115.00
402	SEGB <sub>5</sub>	4347.00	1115.00
403	SEGC <sub>5</sub>	4305.00	1115.00
404	SEGA <sub>6</sub>	4263.00	1115.00
405	SEGB <sub>6</sub>	4221.00	1115.00
406	SEGC <sub>6</sub>	4179.00	1115.00
407	SEGA <sub>7</sub>	4137.00	1115.00
408	SEGB <sub>7</sub>	4095.00	1115.00
409	SEGC <sub>7</sub>	4053.00	1115.00
410	SEGA <sub>8</sub>	4011.00	1115.00
411	SEGB <sub>8</sub>	3969.00	1115.00
412	SEGC <sub>8</sub>	3927.00	1115.00
413	SEGA <sub>9</sub>	3885.00	1115.00
414	SEGB <sub>9</sub>	3843.00	1115.00
415	SEGC <sub>9</sub>	3801.00	1115.00
416	SEGA <sub>10</sub>	3759.00	1115.00
417	SEGB <sub>10</sub>	3717.00	1115.00
418	SEGC <sub>10</sub>	3675.00	1115.00
419	SEGA <sub>11</sub>	3633.00	1115.00
420	SEGB <sub>11</sub>	3591.00	1115.00

No.	PAD NAME	X (μm)	Y (μm)
421	SEGC <sub>11</sub>	3549.00	1115.00
422	SEGA <sub>12</sub>	3507.00	1115.00
423	SEGB <sub>12</sub>	3465.00	1115.00
424	SEGC <sub>12</sub>	3423.00	1115.00
425	SEGA <sub>13</sub>	3381.00	1115.00
426	SEGB <sub>13</sub>	3339.00	1115.00
427	SEGC <sub>13</sub>	3297.00	1115.00
428	SEGA <sub>14</sub>	3255.00	1115.00
429	SEGB <sub>14</sub>	3213.00	1115.00
430	SEGC <sub>14</sub>	3171.00	1115.00
431	SEGA <sub>15</sub>	3129.00	1115.00
432	SEGB <sub>15</sub>	3087.00	1115.00
433	SEGC <sub>15</sub>	3045.00	1115.00
434	SEGA <sub>16</sub>	3003.00	1115.00
435	SEGB <sub>16</sub>	2961.00	1115.00
436	SEGC <sub>16</sub>	2919.00	1115.00
437	SEGA <sub>17</sub>	2877.00	1115.00
438	SEGB <sub>17</sub>	2835.00	1115.00
439	SEGC <sub>17</sub>	2793.00	1115.00
440	SEGA <sub>18</sub>	2751.00	1115.00
441	SEGB <sub>18</sub>	2709.00	1115.00
442	SEGC <sub>18</sub>	2667.00	1115.00
443	SEGA <sub>19</sub>	2625.00	1115.00
444	SEGB <sub>19</sub>	2583.00	1115.00
445	SEGC <sub>19</sub>	2541.00	1115.00
446	SEGA <sub>20</sub>	2499.00	1115.00
447	SEGB <sub>20</sub>	2457.00	1115.00
448	SEGC <sub>20</sub>	2415.00	1115.00
449	SEGA <sub>21</sub>	2373.00	1115.00
450	SEGB <sub>21</sub>	2331.00	1115.00
451	SEGC <sub>21</sub>	2289.00	1115.00
452	SEGA <sub>22</sub>	2247.00	1115.00
453	SEGB <sub>22</sub>	2205.00	1115.00
454	SEGC <sub>22</sub>	2163.00	1115.00
455	SEGA <sub>23</sub>	2121.00	1115.00
456	SEGB <sub>23</sub>	2079.00	1115.00
457	SEGC <sub>23</sub>	2037.00	1115.00
458	SEGA <sub>24</sub>	1995.00	1115.00
459	SEGB <sub>24</sub>	1953.00	1115.00
460	SEGC <sub>24</sub>	1911.00	1115.00
461	SEGA <sub>25</sub>	1869.00	1115.00
462	SEGB <sub>25</sub>	1827.00	1115.00
463	SEGC <sub>25</sub>	1785.00	1115.00
464	SEGA <sub>26</sub>	1743.00	1115.00
465	SEGB <sub>26</sub>	1701.00	1115.00
466	SEGC <sub>26</sub>	1659.00	1115.00
467	SEGA <sub>27</sub>	1617.00	1115.00
468	SEGB <sub>27</sub>	1575.00	1115.00
469	SEGC <sub>27</sub>	1533.00	1115.00
470	SEGA <sub>28</sub>	1491.00	1115.00
471	SEGB <sub>28</sub>	1449.00	1115.00
472	SEGC <sub>28</sub>	1407.00	1115.00
473	SEGA <sub>29</sub>	1365.00	1115.00
474	SEGB <sub>29</sub>	1323.00	1115.00
475	SEGC <sub>29</sub>	1281.00	1115.00
476	SEGA <sub>30</sub>	1239.00	1115.00
477	SEGB <sub>30</sub>	1197.00	1115.00
478	SEGC <sub>30</sub>	1155.00	1115.00
479	SEGA <sub>31</sub>	1113.00	1115.00
480	SEGB <sub>31</sub>	1071.00	1115.00

No.	PAD NAME	X (μm)	Y (μm)
481	SEGC <sub>31</sub>	1029.00	1115.00
482	SEGA <sub>32</sub>	987.00	1115.00
483	SEGB <sub>32</sub>	945.00	1115.00
484	SEGC <sub>32</sub>	903.00	1115.00
485	SEGA <sub>33</sub>	861.00	1115.00
486	SEGB <sub>33</sub>	819.00	1115.00
487	SEGC <sub>33</sub>	777.00	1115.00
488	SEGA <sub>34</sub>	735.00	1115.00
489	SEGB <sub>34</sub>	693.00	1115.00
490	SEGC <sub>34</sub>	651.00	1115.00
491	SEGA <sub>35</sub>	609.00	1115.00
492	SEGB <sub>35</sub>	567.00	1115.00
493	SEGC <sub>35</sub>	525.00	1115.00
494	SEGA <sub>36</sub>	483.00	1115.00
495	SEGB <sub>36</sub>	441.00	1115.00
496	SEGC <sub>36</sub>	399.00	1115.00
497	SEGA <sub>37</sub>	357.00	1115.00
498	SEGB <sub>37</sub>	315.00	1115.00
499	SEGC <sub>37</sub>	273.00	1115.00
500	SEGA <sub>38</sub>	231.00	1115.00
501	SEGB <sub>38</sub>	189.00	1115.00
502	SEGC <sub>38</sub>	147.00	1115.00
503	SEGA <sub>39</sub>	105.00	1115.00
504	SEGB <sub>39</sub>	63.00	1115.00
505	SEGC <sub>39</sub>	21.00	1115.00
506	SEGA <sub>40</sub>	-21.00	1115.00
507	SEGB <sub>40</sub>	-63.00	1115.00
508	SEGC <sub>40</sub>	-105.00	1115.00
509	SEGA <sub>41</sub>	-147.00	1115.00
510	SEGB <sub>41</sub>	-189.00	1115.00
511	SEGC <sub>41</sub>	-231.00	1115.00
512	SEGA <sub>42</sub>	-273.00	1115.00
513	SEGB <sub>42</sub>	-315.00	1115.00
514	SEGC <sub>42</sub>	-357.00	1115.00
515	SEGA <sub>43</sub>	-399.00	1115.00
516	SEGB <sub>43</sub>	-441.00	1115.00
517	SEGC <sub>43</sub>	-483.00	1115.00
518	SEGA <sub>44</sub>	-525.00	1115.00
519	SEGB <sub>44</sub>	-567.00	1115.00
520	SEGC <sub>44</sub>	-609.00	1115.00
521	SEGA <sub>45</sub>	-651.00	1115.00
522	SEGB <sub>45</sub>	-693.00	1115.00
523	SEGC <sub>45</sub>	-735.00	1115.00
524	SEGA <sub>46</sub>	-777.00	1115.00
525	SEGB <sub>46</sub>	-819.00	1115.00
526	SEGC <sub>46</sub>	-861.00	1115.00
527	SEGA <sub>47</sub>	-903.00	1115.00
528	SEGB <sub>47</sub>	-945.00	1115.00
529	SEGC <sub>47</sub>	-987.00	1115.00
530	SEGA <sub>48</sub>	-1029.00	1115.00
531	SEGB <sub>48</sub>	-1071.00	1115.00
532	SEGC <sub>48</sub>	-1113.00	1115.00
533	SEGA <sub>49</sub>	-1155.00	1115.00
534	SEGB <sub>49</sub>	-1197.00	1115.00
535	SEGC <sub>49</sub>	-1239.00	1115.00
536	SEGA <sub>50</sub>	-1281.00	1115.00
537	SEGB <sub>50</sub>	-1323.00	1115.00
538	SEGC <sub>50</sub>	-1365.00	1115.00
539	SEGA <sub>51</sub>	-1407.00	1115.00
540	SEGB <sub>51</sub>	-1449.00	1115.00

## ■ PAD COORDINATES 4

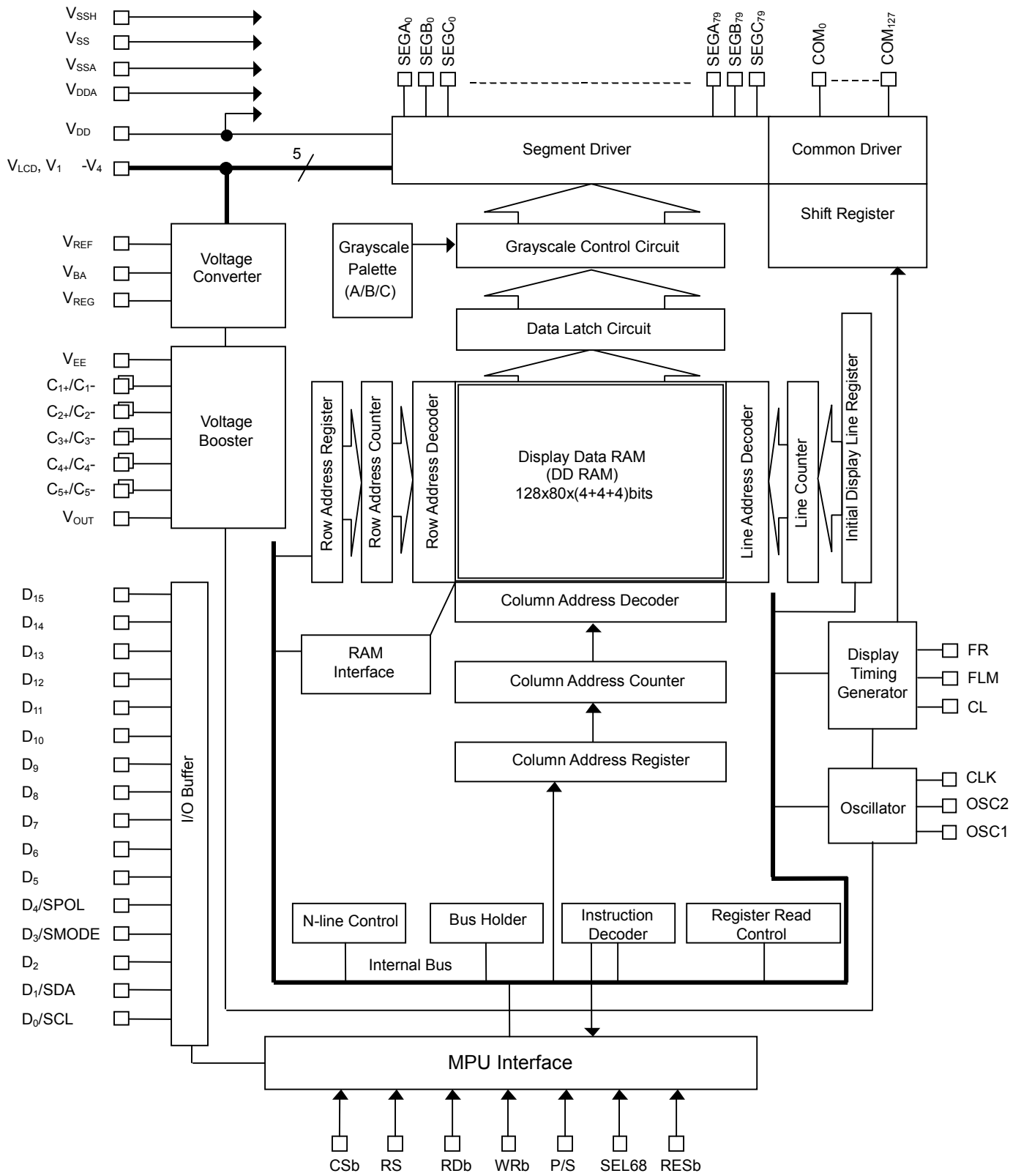
Chip Size 16,700μm x 2,640μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X(μm)	Y(μm)
541	SEGC <sub>51</sub>	-1491.00	1115.00
542	SEGA <sub>52</sub>	-1533.00	1115.00
543	SEGB <sub>52</sub>	-1575.00	1115.00
544	SEGC <sub>52</sub>	-1617.00	1115.00
545	SEGA <sub>53</sub>	-1659.00	1115.00
546	SEGB <sub>53</sub>	-1701.00	1115.00
547	SEGC <sub>53</sub>	-1743.00	1115.00
548	SEGA <sub>54</sub>	-1785.00	1115.00
549	SEGB <sub>54</sub>	-1827.00	1115.00
550	SEGC <sub>54</sub>	-1869.00	1115.00
551	SEGA <sub>55</sub>	-1911.00	1115.00
552	SEGB <sub>55</sub>	-1953.00	1115.00
553	SEGC <sub>55</sub>	-1995.00	1115.00
554	SEGA <sub>56</sub>	-2037.00	1115.00
555	SEGB <sub>56</sub>	-2079.00	1115.00
556	SEGC <sub>56</sub>	-2121.00	1115.00
557	SEGA <sub>57</sub>	-2163.00	1115.00
558	SEGB <sub>57</sub>	-2205.00	1115.00
559	SEGC <sub>57</sub>	-2247.00	1115.00
560	SEGA <sub>58</sub>	-2289.00	1115.00
561	SEGB <sub>58</sub>	-2331.00	1115.00
562	SEGC <sub>58</sub>	-2373.00	1115.00
563	SEGA <sub>59</sub>	-2415.00	1115.00
564	SEGB <sub>59</sub>	-2457.00	1115.00
565	SEGC <sub>59</sub>	-2499.00	1115.00
566	SEGA <sub>60</sub>	-2541.00	1115.00
567	SEGB <sub>60</sub>	-2583.00	1115.00
568	SEGC <sub>60</sub>	-2625.00	1115.00
569	SEGA <sub>61</sub>	-2667.00	1115.00
570	SEGB <sub>61</sub>	-2709.00	1115.00
571	SEGC <sub>61</sub>	-2751.00	1115.00
572	SEGA <sub>62</sub>	-2793.00	1115.00
573	SEGB <sub>62</sub>	-2835.00	1115.00
574	SEGC <sub>62</sub>	-2877.00	1115.00
575	SEGA <sub>63</sub>	-2919.00	1115.00
576	SEGB <sub>63</sub>	-2961.00	1115.00
577	SEGC <sub>63</sub>	-3003.00	1115.00
578	SEGA <sub>64</sub>	-3045.00	1115.00
579	SEGB <sub>64</sub>	-3087.00	1115.00
580	SEGC <sub>64</sub>	-3129.00	1115.00
581	SEGA <sub>65</sub>	-3171.00	1115.00
582	SEGB <sub>65</sub>	-3213.00	1115.00
583	SEGC <sub>65</sub>	-3255.00	1115.00
584	SEGA <sub>66</sub>	-3297.00	1115.00
585	SEGB <sub>66</sub>	-3339.00	1115.00
586	SEGC <sub>66</sub>	-3381.00	1115.00
587	SEGA <sub>67</sub>	-3423.00	1115.00
588	SEGB <sub>67</sub>	-3465.00	1115.00
589	SEGC <sub>67</sub>	-3507.00	1115.00
590	SEGA <sub>68</sub>	-3549.00	1115.00
591	SEGB <sub>68</sub>	-3591.00	1115.00
592	SEGC <sub>68</sub>	-3633.00	1115.00
593	SEGA <sub>69</sub>	-3675.00	1115.00
594	SEGB <sub>69</sub>	-3717.00	1115.00
595	SEGC <sub>69</sub>	-3759.00	1115.00
596	SEGA <sub>70</sub>	-3801.00	1115.00
597	SEGB <sub>70</sub>	-3843.00	1115.00
598	SEGC <sub>70</sub>	-3885.00	1115.00
599	SEGA <sub>71</sub>	-3927.00	1115.00
600	SEGB <sub>71</sub>	-3969.00	1115.00

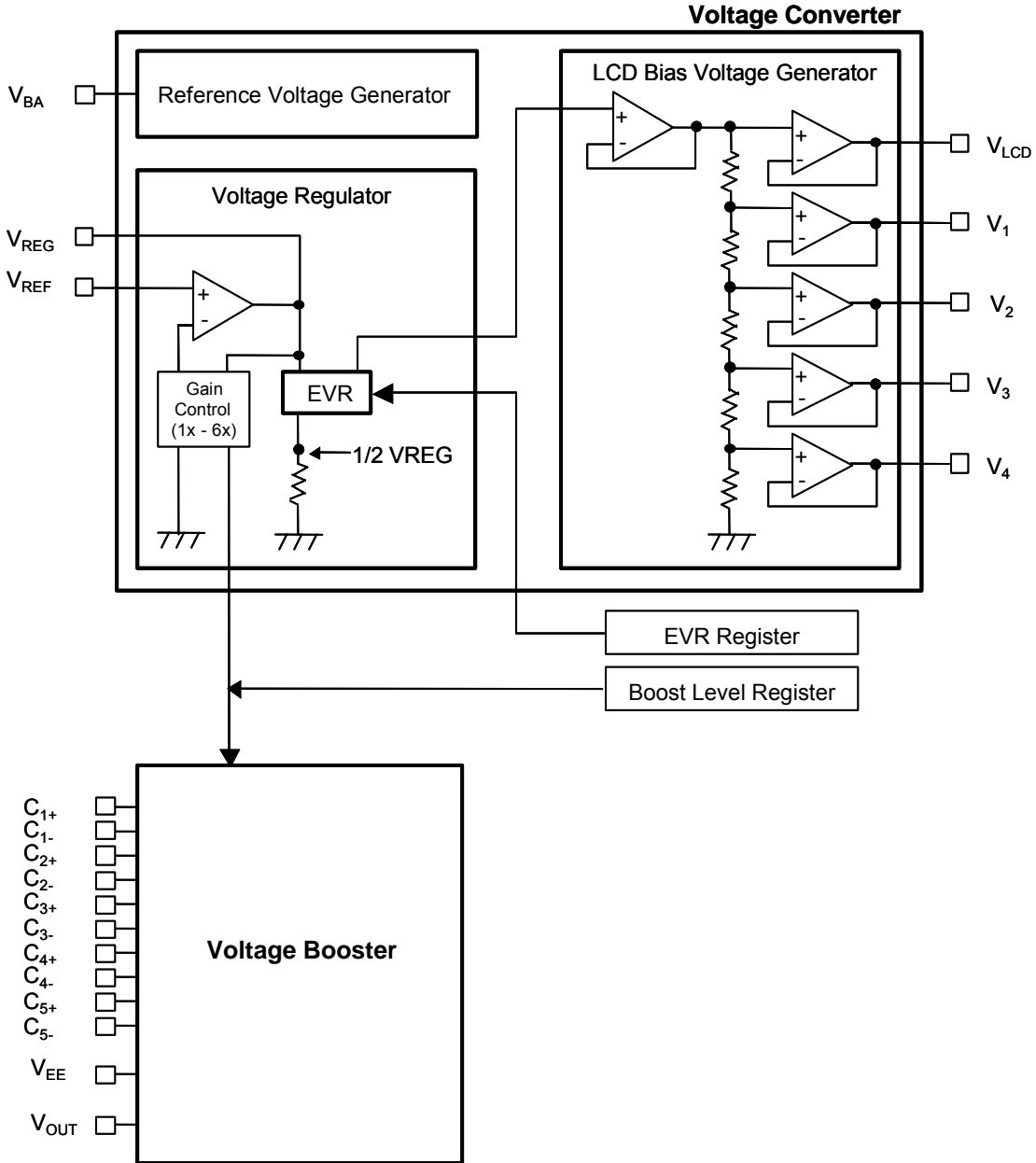
No.	PAD NAME	X(μm)	Y(μm)
601	SEGC <sub>71</sub>	-4011.00	1115.00
602	SEGA <sub>72</sub>	-4053.00	1115.00
603	SEGB <sub>72</sub>	-4095.00	1115.00
604	SEGC <sub>72</sub>	-4137.00	1115.00
605	SEGA <sub>73</sub>	-4179.00	1115.00
606	SEGB <sub>73</sub>	-4221.00	1115.00
607	SEGC <sub>73</sub>	-4263.00	1115.00
608	SEGA <sub>74</sub>	-4305.00	1115.00
609	SEGB <sub>74</sub>	-4347.00	1115.00
610	SEGC <sub>74</sub>	-4389.00	1115.00
611	SEGA <sub>75</sub>	-4431.00	1115.00
612	SEGB <sub>75</sub>	-4473.00	1115.00
613	SEGC <sub>75</sub>	-4515.00	1115.00
614	SEGA <sub>76</sub>	-4557.00	1115.00
615	SEGB <sub>76</sub>	-4599.00	1115.00
616	SEGC <sub>76</sub>	-4641.00	1115.00
617	SEGA <sub>77</sub>	-4683.00	1115.00
618	SEGB <sub>77</sub>	-4725.00	1115.00
619	SEGC <sub>77</sub>	-4767.00	1115.00
620	SEGA <sub>78</sub>	-4809.00	1115.00
621	SEGB <sub>78</sub>	-4851.00	1115.00
622	SEGC <sub>78</sub>	-4893.00	1115.00
623	SEGA <sub>79</sub>	-4935.00	1115.00
624	SEGB <sub>79</sub>	-4977.00	1115.00
625	SEGC <sub>79</sub>	-5019.00	1115.00
626	DMY <sub>44</sub>	-5061.00	1115.00
627	DMY <sub>45</sub>	-5103.00	1115.00
628	DMY <sub>46</sub>	-5145.00	1115.00
629	COM <sub>127</sub>	-5187.00	1115.00
630	COM <sub>125</sub>	-5229.00	1115.00
631	COM <sub>123</sub>	-5271.00	1115.00
632	COM <sub>121</sub>	-5313.00	1115.00
633	COM <sub>119</sub>	-5355.00	1115.00
634	COM <sub>117</sub>	-5397.00	1115.00
635	COM <sub>115</sub>	-5439.00	1115.00
636	COM <sub>113</sub>	-5481.00	1115.00
637	COM <sub>111</sub>	-5523.00	1115.00
638	COM <sub>109</sub>	-5565.00	1115.00
639	COM <sub>107</sub>	-5607.00	1115.00
640	COM <sub>105</sub>	-5649.00	1115.00
641	COM <sub>103</sub>	-5691.00	1115.00
642	COM <sub>101</sub>	-5733.00	1115.00
643	COM <sub>99</sub>	-5775.00	1115.00
644	COM <sub>97</sub>	-5817.00	1115.00
645	COM <sub>95</sub>	-5859.00	1115.00
646	COM <sub>93</sub>	-5901.00	1115.00
647	COM <sub>91</sub>	-5943.00	1115.00
648	COM <sub>89</sub>	-5985.00	1115.00
649	COM <sub>87</sub>	-6027.00	1115.00
650	COM <sub>85</sub>	-6069.00	1115.00
651	COM <sub>83</sub>	-6111.00	1115.00
652	COM <sub>81</sub>	-6153.00	1115.00
653	COM <sub>79</sub>	-6195.00	1115.00
654	COM <sub>77</sub>	-6237.00	1115.00
655	COM <sub>75</sub>	-6279.00	1115.00
656	COM <sub>73</sub>	-6321.00	1115.00
657	COM <sub>71</sub>	-6363.00	1115.00
658	COM <sub>69</sub>	-6405.00	1115.00
659	COM <sub>67</sub>	-6447.00	1115.00
660	COM <sub>65</sub>	-6489.00	1115.00

No.	PAD NAME	X(μm)	Y(μm)
661	COM <sub>63</sub>	-6531.00	1115.00
662	COM <sub>61</sub>	-6573.00	1115.00
663	COM <sub>59</sub>	-6615.00	1115.00
664	COM <sub>57</sub>	-6657.00	1115.00
665	COM <sub>55</sub>	-6699.00	1115.00
666	COM <sub>53</sub>	-6741.00	1115.00
667	COM <sub>51</sub>	-6783.00	1115.00
668	COM <sub>49</sub>	-6825.00	1115.00
669	COM <sub>47</sub>	-6867.00	1115.00
670	COM <sub>45</sub>	-6909.00	1115.00
671	COM <sub>43</sub>	-6951.00	1115.00
672	COM <sub>41</sub>	-6993.00	1115.00
673	COM <sub>39</sub>	-7035.00	1115.00
674	COM <sub>37</sub>	-7077.00	1115.00
675	COM <sub>35</sub>	-7119.00	1115.00
676	COM <sub>33</sub>	-7161.00	1115.00
677	COM <sub>31</sub>	-7203.00	1115.00
678	COM <sub>29</sub>	-7245.00	1115.00
679	COM <sub>27</sub>	-7287.00	1115.00
680	COM <sub>25</sub>	-7329.00	1115.00
681	COM <sub>23</sub>	-7371.00	1115.00
682	COM <sub>21</sub>	-7413.00	1115.00
683	COM <sub>19</sub>	-7455.00	1115.00
684	COM <sub>17</sub>	-7497.00	1115.00
685	COM <sub>15</sub>	-7539.00	1115.00
686	COM <sub>13</sub>	-7581.00	1115.00
687	COM <sub>11</sub>	-7623.00	1115.00
688	COM <sub>9</sub>	-7665.00	1115.00
689	COM <sub>7</sub>	-7707.00	1115.00
690	COM <sub>5</sub>	-7749.00	1115.00
691	COM <sub>3</sub>	-7791.00	1115.00
692	COM <sub>1</sub>	-7833.00	1115.00
693	DMY <sub>47</sub>	-7875.00	1115.00
694	DMY <sub>48</sub>	-7917.00	1115.00
695	DMY <sub>49</sub>	-7959.00	1115.00
696	DMY <sub>50</sub>	-8001.00	1115.00
697	DMY <sub>51</sub>	-8043.00	-867.00
698	DMY <sub>52</sub>	-8085.00	-909.00
699	DMY <sub>52</sub>	-8127.00	-951.00
700	DMY <sub>52</sub>	-8169.00	-993.00
701	DMY <sub>53</sub>	-8211.00	-1035.00

## ■ BLOCK DIAGRAM



## ■ LCD POWER SUPPLY BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION 1

No.	Terminal	I/O	Function						
70~78	V <sub>DD</sub>	Power	Power Supply for Logic Circuits						
93~101	V <sub>SS</sub>	Power	GND for Logic Circuits						
181~189	V <sub>SSH</sub>	Power	GND for High Voltage Circuits						
10,11 34,35 52,53	V <sub>DDA</sub>	Power	V <sub>DDA</sub> is internally connected to V <sub>DD</sub> to fix SEL68 or P/S to "H" if necessary, and cannot be used as main power supply. • V <sub>DDA</sub> should be open if not used.						
4,5 16,17	V <sub>SSA</sub>	Power	V <sub>SSA</sub> is internally connected to V <sub>SS</sub> to fix SEL68 or P/S to "L" if necessary, and cannot be used as main GND. • V <sub>SSA</sub> should be open if not used.						
103~111 113~121 122~130 132~140 141~149	V <sub>LCD</sub> V <sub>1</sub> V <sub>2</sub> V <sub>3</sub> V <sub>4</sub>	Power	LCD Bias Voltages • When the internal LCD power supply is used, internal LCD bias voltages (V <sub>LCD</sub> and V <sub>1</sub> -V <sub>4</sub> ) are activated by the "Power Control" instruction. Stabilizing capacitors are required between each bias voltage and V <sub>SS</sub> . • When the external LCD power supply is used, LCD bias voltages are externally supplied on V <sub>LCD</sub> , V <sub>1</sub> , V <sub>2</sub> , V <sub>3</sub> and V <sub>4</sub> individually, with the following relation maintained: V <sub>SSH</sub> <V <sub>4</sub> <V <sub>3</sub> <V <sub>2</sub> <V <sub>1</sub> <V <sub>LCD</sub>						
208~216 218~226	C <sub>1+</sub> C <sub>1-</sub>	Power	Capacitor Connection for Voltage Booster						
228~236 238~246	C <sub>2+</sub> C <sub>2-</sub>	Power	Capacitor Connection for Voltage Booster						
248~256 258~266	C <sub>3+</sub> C <sub>3-</sub>	Power	Capacitor Connection for Voltage Booster						
268~276 278~286	C <sub>4+</sub> C <sub>4-</sub>	Power	Capacitor Connection for Voltage Booster						
288~296 298~306	C <sub>5+</sub> C <sub>5-</sub>	Power	Capacitor Connection for Voltage Booster						
171~179	V <sub>BA</sub>	Power	Reference-Voltage Generator Output						
161~169	V <sub>REF</sub>	Power	Voltage Regulator Input						
199~207	V <sub>EE</sub>	Power	Voltage Booster Input • V <sub>EE</sub> is normally connected to V <sub>DD</sub> .						
190~198	V <sub>OUT</sub>	Power	Voltage Booster Output • Input if an external LCD power supply is used.						
151~159	V <sub>REG</sub>	Power	Voltage Regulator Output						
19,20	RESb	I	Reset • Active "L"						
7,8	SEL68	I	MPU Mode Select <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>SEL86</td> <td>H</td> <td>L</td> </tr> <tr> <td>MPU</td> <td>68-series</td> <td>80-series</td> </tr> </table>	SEL86	H	L	MPU	68-series	80-series
SEL86	H	L							
MPU	68-series	80-series							

## ■ TERMINAL DESCRIPTION 2

No.	Terminal	I/O	Function						
36,37	D <sub>0</sub> /SCL	I/O	<u>Parallel Interface</u> D <sub>7</sub> to D <sub>0</sub> : 8-bit Bi-directional Bus  • In the parallel interface mode (P/S="H"), D <sub>7</sub> -D <sub>0</sub> are connected to 8-bit bi-directional MPU bus.						
38,39	D <sub>1</sub> /SDA	I/O							
42,43	D <sub>3</sub> /SMODE	I/O	<u>Serial Interface</u> SDA : Serial Data SCL : Serial Clock SMODE : 3-/4-line Serial Mode Select SPOL : RS Polarity Select (3-line Serial Interface Mode)						
44,45	D <sub>4</sub> /SPOL	I/O	• In the 3 or 4-line serial interface mode (P/S="L"), D <sub>0</sub> is assigned to SCL, and D <sub>1</sub> to SDA. • In the 3-line serial interface mode, D <sub>4</sub> is assigned to SPOL.						
40,41 46,47 48,49 50,51	D <sub>2</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	I/O	• Serial data on SDA is latched at the rising edge of SCL signal in order of D <sub>7</sub> , D <sub>6</sub> ,... and D <sub>0</sub> , and then converted into 8-bit parallel data at the timing of the internal signal produced from the 8 <sup>th</sup> SCL. • SCL should be set to "L" right after data transmission or during non-access.						
54,55 56,57 58,59 60,61 62,63 64,65 66,67 68,69	D <sub>8</sub> D <sub>9</sub> D <sub>10</sub> D <sub>11</sub> D <sub>12</sub> D <sub>13</sub> D <sub>14</sub> D <sub>15</sub>	I/O	8-bit Bi-directional Bus • In the 16-bit bus length mode, D <sub>15</sub> -D <sub>8</sub> are assigned to upper 8-bit data bus. • In the serial interface mode or the 8-bit parallel interface mode, D <sub>15</sub> -D <sub>8</sub> should be fixed to "H" or "L".						
22,23	CSb	I	Chip Select • Active "L"						
25,26	RS	I	Register Select • This signal interprets transferred data as display data or instruction. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>RS</th> <th>H</th> <th>L</th> </tr> </thead> <tbody> <tr> <td>Data</td> <td>Instruction</td> <td>Display Data</td> </tr> </tbody> </table>	RS	H	L	Data	Instruction	Display Data
RS	H	L							
Data	Instruction	Display Data							
31,32	RDb (E)	I	80-series MPU Interface (P/S="H", SEL68="L") Data Read (RDb) Signal • Active "L" 68-series MPU Interface (P/S="H", SEL68="H") Enable Signal • Active "H"						
28,29	WRb (R/W)	I	80-series MPU Interface (P/S="H", SEL68="L") Data Write (WRb) Signal • Active "L" 68-series MPU Interface (P/S="H", SEL68="H") Data Read or Write (R/W) Signal <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>R/W</th> <th>H</th> <th>L</th> </tr> </thead> <tbody> <tr> <td>Status</td> <td>Read</td> <td>Write</td> </tr> </tbody> </table>	R/W	H	L	Status	Read	Write
R/W	H	L							
Status	Read	Write							

## ■ TERMINAL DESCRIPTION 3

No.	Terminal	I/O	Function																		
13,14	P/S	I	Parallel/Serial Interface Mode Select																		
			<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">P/S</th> <th style="width: 15%;">Chip Select</th> <th style="width: 20%;">Display / Instruction</th> <th style="width: 20%;">Data</th> <th style="width: 15%;">Read /Write</th> <th style="width: 10%;">Serial Clock</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>CSb</td> <td>RS</td> <td>D<sub>0</sub> ~ D<sub>7</sub></td> <td>RDb, WRb</td> <td>-</td> </tr> <tr> <td>L</td> <td>CSb</td> <td>RS</td> <td>SDA (D<sub>1</sub>)</td> <td>Write Only</td> <td>SCL (D<sub>0</sub>)</td> </tr> </tbody> </table>	P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock	H	CSb	RS	D <sub>0</sub> ~ D <sub>7</sub>	RDb, WRb	-	L	CSb	RS	SDA (D <sub>1</sub> )	Write Only	SCL (D <sub>0</sub> )
			P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock													
H	CSb	RS	D <sub>0</sub> ~ D <sub>7</sub>	RDb, WRb	-																
L	CSb	RS	SDA (D <sub>1</sub> )	Write Only	SCL (D <sub>0</sub> )																
<ul style="list-style-type: none"> <li>In the serial interface mode (P/S="L"), RDb, WRb, D<sub>2</sub> and D<sub>5</sub>-D<sub>15</sub> should be fixed to "H" or "L",.</li> </ul>																					
79,80	CL	O	Line Clock <ul style="list-style-type: none"> <li>CL is normally open.</li> </ul>																		
81,82	FLM	O	First Line Maker <ul style="list-style-type: none"> <li>FLM is normally open.</li> </ul>																		
83,84	FR	O	Frame Rate <ul style="list-style-type: none"> <li>FR is normally open.</li> </ul>																		
85,86	CLK	O	Clock Output <ul style="list-style-type: none"> <li>CLK is normally open.</li> </ul>																		
88,89 91,92	OSC1 OSC2	I O	OSC <ul style="list-style-type: none"> <li>When the internal oscillator is used, fix OSC1 to "H" or "L" and leave OSC2 open. To attain more accurate frequency, connect OSC1 and OSC2 with an external resistor.</li> <li>When the internal oscillator is not used, input external clock to OSC1 and leave OSC2 open.</li> </ul>																		
386~625	SEGA <sub>0</sub> ~SEGA <sub>79</sub>  SEGB <sub>0</sub> ~SEGB <sub>79</sub>  SEGC <sub>0</sub> ~SEGC <sub>79</sub>	O	Segment Drivers																		
			<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">REV Register</th> <th style="width: 35%;">OFF</th> <th style="width: 35%;">ON</th> </tr> </thead> <tbody> <tr> <td>Normal</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td>Reverse</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> </tr> </tbody> </table>	REV Register	OFF	ON	Normal	0	1	Reverse	1	0									
			REV Register	OFF	ON																
Normal	0	1																			
Reverse	1	0																			
<ul style="list-style-type: none"> <li>Segment drivers output the following voltage levels.</li> </ul> <p>B/W Mode (Example)</p>																					
319~382 629~692	COM <sub>0</sub> ~ COM <sub>127</sub>	O	Common Drivers <ul style="list-style-type: none"> <li>Common drivers output the following voltage levels.</li> </ul> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Data</th> <th style="width: 20%;">FR</th> <th style="width: 60%;">Output Levels</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>V<sub>SSH</sub></td> </tr> <tr> <td>L</td> <td>H</td> <td>V<sub>1</sub></td> </tr> <tr> <td>H</td> <td>L</td> <td>V<sub>LCD</sub></td> </tr> <tr> <td>L</td> <td>L</td> <td>V<sub>4</sub></td> </tr> </tbody> </table>	Data	FR	Output Levels	H	H	V <sub>SSH</sub>	L	H	V <sub>1</sub>	H	L	V <sub>LCD</sub>	L	L	V <sub>4</sub>			
Data	FR	Output Levels																			
H	H	V <sub>SSH</sub>																			
L	H	V <sub>1</sub>																			
H	L	V <sub>LCD</sub>																			
L	L	V <sub>4</sub>																			

NOTE) DUMMY PADS: No. 1~3, 6, 9, 12, 15, 18, 21, 24, 27, 30, 33, 87, 90, 102, 112, 131, 150, 160, 170, 180, 217, 227, 237, 247, 257, 267, 277, 287, 297, 307~318, 383~385, 626~628, 693~701

## ■ FUNCTIONAL DESCRIPTION

### (1) MPU INTERFACE

#### (1-1) Selection of Parallel/Serial Interface Mode

The P/S selects a parallel or a serial interface mode, as shown in Table 1. In the serial interface mode, neither display data in the DDRAM nor instruction data in the registers can be read out.

**Table 1 Selection of Parallel/Serial Interface Mode**

P/S	I/F Mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D <sub>7</sub> -D <sub>0</sub> (D <sub>15</sub> -D <sub>0</sub> )
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

NOTE) “-” : Fix to “H” or “L”.

#### (1-2) Selection of MPU Mode

In the parallel interface mode, the SEL68 selects 68 or 80-series MPU mode, as shown in Table 2.

**Table 2 Selection of MPU Mode**

SEL68	MPU Mode	CSb	RS	RDb	WRb	Data
H	68-series MPU	CSb	RS	E	R/W	D <sub>7</sub> -D <sub>0</sub> (D <sub>15</sub> -D <sub>0</sub> )
L	80-series MPU	CSb	RS	RDb	WRb	D <sub>7</sub> -D <sub>0</sub> (D <sub>15</sub> -D <sub>0</sub> )

#### (1-3) Data Recognition

In the parallel interface mode, the data from MPU is interpreted as display data or instruction according to the combination of the RS, RDb and WRb (R/W) signals, as shown in Table 3.

**Table 3 Data Recognition (Parallel Interface Mode)**

RS	68-series	80-series		Function
	R/W	RDb	WRb	
H	H	L	H	Read Instruction
H	L	H	L	Write Instruction
L	H	L	H	Read Display Data
L	L	H	L	Write Display Data

#### (1-4) Selection of 3-/4-line Serial Interface Mode

In the serial interface mode, the SMODE selects 3- or 4-line serial interface mode, as shown in Table 4.

**Table 4 Selection of 3-/4-line Serial Interface Mode**

SMODE	Serial Interface Mode
H	3-line
L	4-line

#### (1-5) 4-line Serial Interface Mode

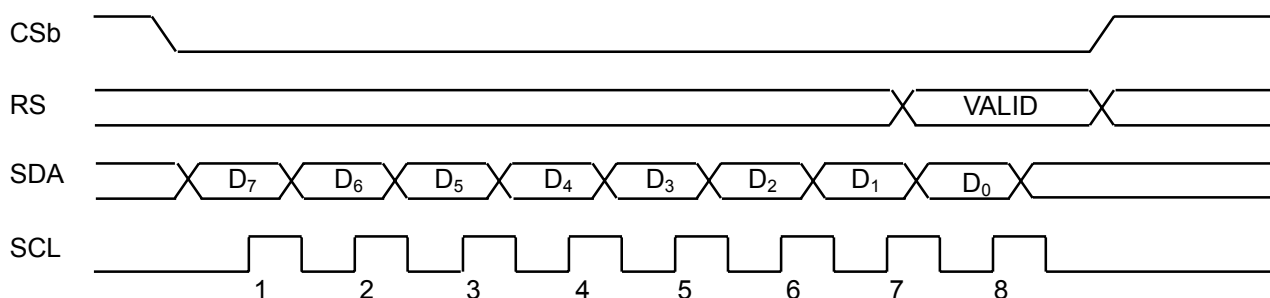
While the chip select is active (CSb=“L”), the SDA and SCL are enabled. While the chip select is inactive (CSb=“H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 8-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of D<sub>7</sub>, D<sub>6</sub>,..., and D<sub>0</sub>, and converted into 8-bit parallel data at the timing of the internal signal produced from the 8<sup>th</sup> SCL signal. The data on the SDA is interpreted as display data or instruction according to the RS.



**Table 5 Data Recognition (4-line Serial Interface)**

RS	Data Recognition
H	Instruction
L	Display Data

Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb=“H”) temporary whenever 8-bit data transmission is completed. Fig 1 illustrates the interface timing of the 4-line serial interface mode.



**Fig 1 4-line Serial Interface Timing**

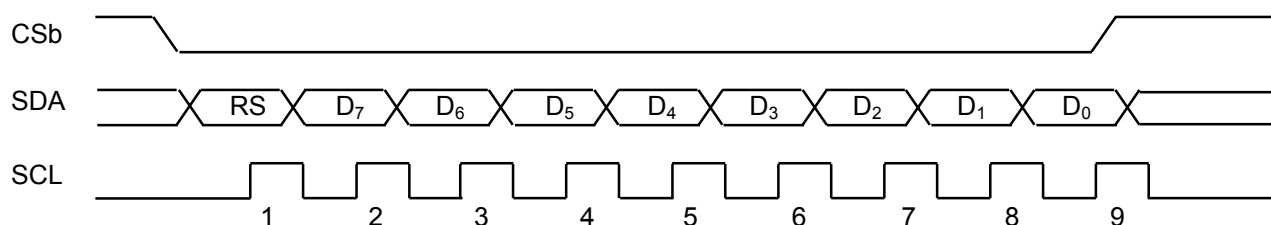
### (1-6) 3-line Serial Interface Mode

While the chip select is active (CSb=“L”), the SDA and SCL are enabled. While the chip select is not active (CSb=“H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 9-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of RS, D<sub>7</sub>, D<sub>6</sub>,..., and D<sub>0</sub>, and then converted into 9-bit parallel data at the timing of the internal signal produced from the 9<sup>th</sup> SCL signal. The data on the SDA is interpreted as display data or instruction according to the combination of the RS bit and the SPOL status, as follows.

**Table 6 Data Recognition (3-line Serial Interface)**

SPOL=L		SPOL=H	
RS	Data Recognition	RS	Data Recognition
0	Display Data	0	Instruction
1	Instruction	1	Display Data

Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb=“H”) temporary whenever 9-bit data transmission is completed. Fig 2 illustrates the interface timing of the 3-line serial interface mode.



**Fig 2 3-line Serial Interface Timing**

## (1-7) Accessing DDRAM

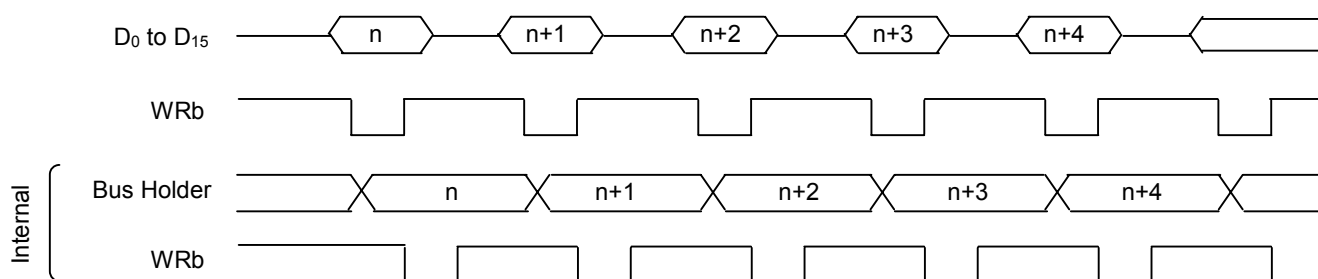
While the chip select is active (CSb="L"), the data from MPU can be written into the DDRAM or the instruction register. When the RS is "L", the data is interpreted as display data which is stored in the DDRAM. The display data is latched at the rising edge of the WRb signal in the 80-series MPU mode, or at the falling edge of the E signal in the 68-series MPU mode.

**Table 7 Data Recognition**

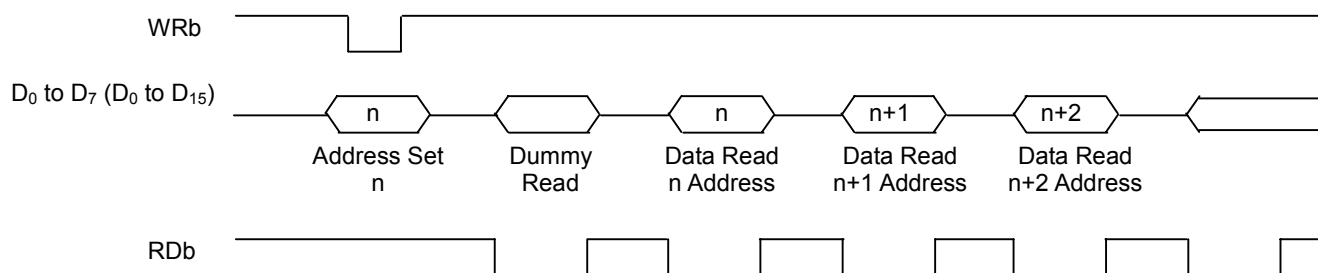
RS	Data Recognition
L	Display Data
H	Instruction

In the DDRAM read sequence, be sure to execute a dummy read right after setting an address or right after writing display data or instruction. The data from MPU is temporarily held in the internal bus-holder, then released on the internal data-bus, therefore a dummy data is read out by the 1<sup>st</sup> "Display Data Read" instruction. After that, the display data is read out from a specified address by the 2<sup>nd</sup> instruction. Note that the "Display Data Read" instruction cannot be used in the serial interface mode.

### Display Data Write Operation



### Display Data Read Operation

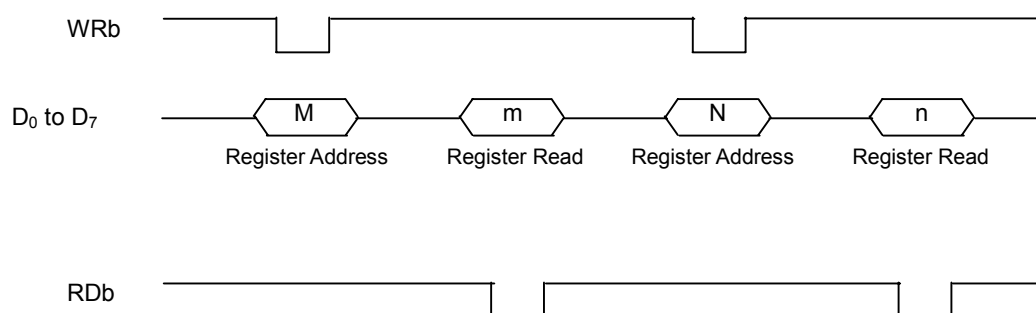


**Fig 3 Internal-signal Timing of Display Data Read/Write Operations**

NOTE) In 16-bit bus length mode, instruction is transmitted to/from instruction register in 16 bits, as well as display data.

## (1-8) Accessing Instruction Register

Each instruction register has a specific address in between (0H) and (FH), and instruction data is read out from the register by the “Register Address” and ”Register Read” instructions. For more information, refer to “(14-23) Register Address” and “(14-24) Register Read”.



**Fig 4 Access Timing of Instruction Register**

## (1-9) Selection of 8-/16-bit Bus Length (Parallel Interface Mode)

Either 8- or 16-bit bus length is selected by the D<sub>0</sub> (WLS) bit of the “Bus Length” instruction. In the 16-bit bus length mode, instruction as well as display data is transmitted to/from the instruction registers in 16 bits (D<sub>15</sub> to D<sub>0</sub>). However, only lower 8 bits (D<sub>7</sub> to D<sub>0</sub>) are valid for instruction register access. And only 12 bits are actually stored in the DDRAM, even though entire 16 bits (D<sub>15</sub> to D<sub>0</sub>) are transmitted for DDRAM access. For more information, refer to “(4-4) Bit Assignment of Display Data”.

**Table 8 Selection of 8-/16-bit Bus Length Mode**

WLS	Bus Length Mode
L	8-bit Bus Length
H	16-bit Bus Length

## (2) INITIAL DISPLAY LINE REGISTER

The address data in the initial display line register specifies the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. The initial COM is the start position of common scanning, which is specified by the “Initial COM” instruction.

The row address, which is established in the initial display line register, is preset into the line counter whenever the FLM becomes “H”. At the rising edge of the CL signal, the line counter is counted-up, then 240-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit to decide a grayscale level, then the segment drivers A<sub>i</sub>, B<sub>i</sub> and C<sub>i</sub> (i=0 to 79) generate LCD waveforms.

## (3) COLUMN AND ROW ADDRESS COUNTERS

The column and row address counters designate a column address and a row address respectively for DDRAM access, but they are completely independent from the line counter. The line counter provides a line address which is synchronized with display control timings such as the FLM and the CL.

## (4) DDRAM

### (4-1) DDRAM Address Range

The DDRAM is capable of 128 bits for row address and 960 bits (12-bit x 80-segment) for column address. The range of the column address is from (00H) to (4FH), and the row address is from (00H) to (7FH). Setting outside these ranges is not allowed, otherwise it may cause malfunctions. For DDRAM access, two data transmissions are needed for 1 RGB-pixel in the 8-bit bus length mode, and one transmission in the 16-bit bus length mode.

#### 8-bit Bus Length

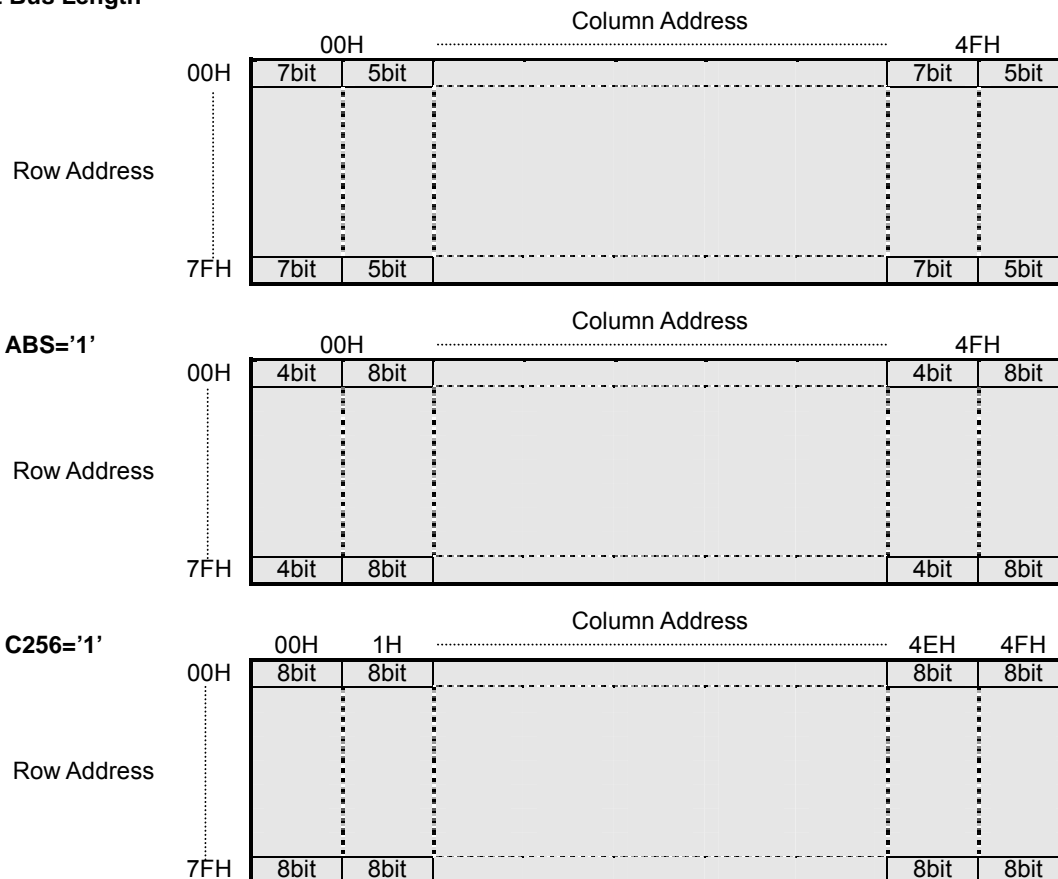


Fig 5 Range of Column Address in 8-bit Bus Length

#### 16-bit Bus Length

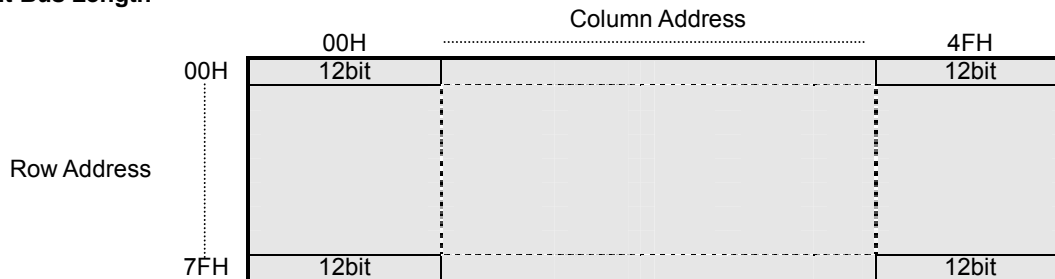


Fig 6 Range of Column Address in 16-bit Bus Length

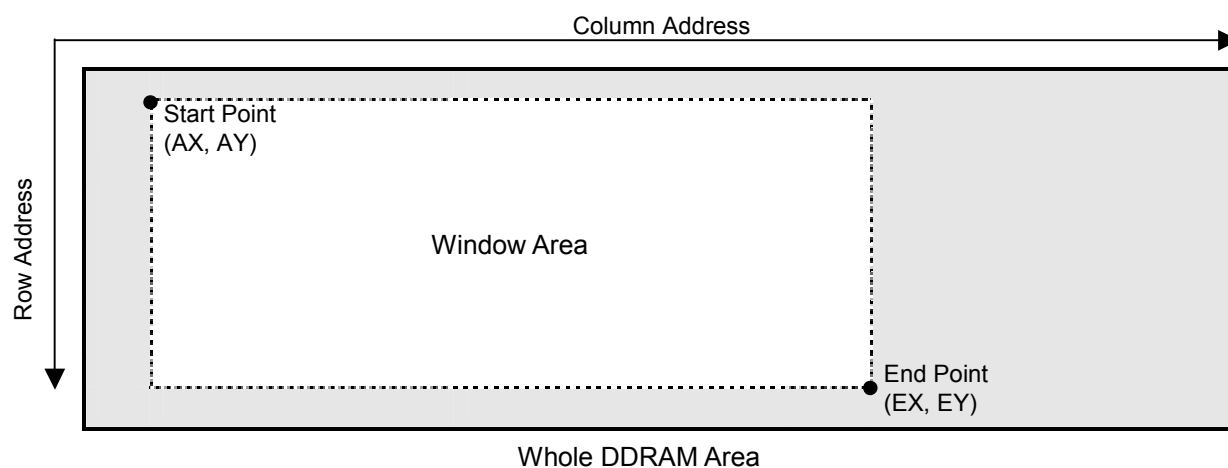
## (4-2) Window Area for DDRAM Access

Be sure to set up window area prior to DDRAM access. This area is set by the “Increment/Decrement Control” instruction and the designation of the start point and the end point.

By the “Increment/Decrement Control”, either auto-increment or -decrement is set for column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up or down, whenever the DDRAM is accessed. And, the start point is specified by the “Window Start Column Address” and “Window Start Row Address” instructions, and the end point by the “Window End Column Address” and “Window End Row Address” instructions. For more information, refer to “(14-9) Increment/Decrement Control”, “(14-25) Window End Column Address” and “(14-26) Window End Row Address”. The typical sequence of the window area setting is listed below.

1. Set D<sub>2</sub> (HV), D<sub>1</sub> (XD) and D<sub>0</sub> (YD) of “Increment/Decrement Control” instruction.
2. Set start point by “Window Start Column Address” and “Window Start Row Address” instructions.
3. Set end point by “Window End Column Address” and “Window End Row Address” instructions.
4. Window area is set up, and DDRAM can be accessed.

NOTE) The order of address setting is column address first, then row address.



**Fig 7 Window Area**

NOTE1) The following relation should be maintained to avoid malfunctions.

- AX (Window Start Column Address) < EX (Window End Column Address) < Maximum Column Address
- AY (Window Start Row Address) < EY (Window End Row Address) < Maximum Row Address

NOTE2) The display-rotation function or the mirror-inversion function is enabled by this setting. Refer to “(4-3) DDRAM Access Direction”.

NOTE3) A read-modify-write operation is enabled by setting “1” at the D<sub>3</sub> (AIM) of the “Increment/Decrement Control” instruction. Refer to the description about “AIM” bit in “(14-9) Increment/Decrement Control”.

## (4-3) DDRAM Access Direction (Display-rotation and Mirror-inversion Functions)

The access direction of the DDRAM is selected out of eight options by setting the D<sub>2</sub> (HV), D<sub>1</sub> (XD) and D<sub>0</sub> (YD) bits of the "Increment/Decrement Control" instruction. This function allows the display data to be rotated 90, 180 or 270 degrees or mirror-inversed while being written onto the DDRAM. The following table shows the correspondences between instruction setting and on-screen image.

No.	HV	XD	YD	DDRAM Access Direction	On-screen Image	Valid Address
0	0	0	0			AX < EX AY < EY
1	0	0	1			AX < EX AY > EY
2	0	1	0			AX > EX AY < EY
3	0	1	1			AX > EX AY > EY
4	1	0	0			AX < EX AY < EY
5	1	0	1			AX < EX AY > EY
6	1	1	0			AX > EX AY < EY
7	1	1	1			AX > EX AY > EY

Fig 8 Display-rotation Function and Mirror-inverse Function

NOTE1) The same display data is used for each option's on-screen image. Only difference is "HV", "XD" and "YD" bits setting.

NOTE2) The following relation must be maintained to avoid malfunctions.

AX (Window Start Column Address) < EX (Window End Column Address) < Maximum Column Address

AY (Window Start Row Address) < EY (Window End Row Address) < Maximum Row Address

(4-4) Bit Assignment of Display Data

(4-4-1) Bit Assignment Overview

These maps is used for grasping general outlines of the variations in the bit assignment of display data.

Table 9-1 RAM MAP 1 (Variable 16-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	WLS	ABS	C256	SEG <sub>0</sub>												SEG <sub>1</sub>												SEG <sub>78</sub>												SEG <sub>79</sub>																															
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C																																			
				A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>
1	0	0		X=00H												X=01H												X=4EH												X=4FH																															
1	1	0		X=00H												X=01H												X=4EH												X=4FH																															
0	0	0		X=00H (Upper)				X=00H (Lower)				X=01H (Upper)				X=01H (Lower)				X=4EH (Upper)				X=4EH (Lower)				X=4FH (Upper)				X=4FH (Lower)																																							
0	1	0		X=00H (Upper)				X=00H (Lower)				X=01H (Upper)				X=01H (Lower)				X=4EH (Upper)				X=4EH (Lower)				X=4FH (Upper)				X=4FH (Lower)																																							

Table 9-2 RAM MAP 2 (Variable 8-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	WLS	ABS	C256	SEG <sub>0</sub>												SEG <sub>1</sub>												SEG <sub>78</sub>												SEG <sub>79</sub>																			
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C																							
				A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>
0	0	1		X=00H												X=01H												X=4EH												X=4FH																			

Table 10 SWAP

SWAP	Palette A			Palette B			Palette C		
	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>
0	SEGAX			SEGBX			SEGCX		
1	SEGCX			SEGBX			SEGAX		

NOTE1) On the RAM MAP 2, A<sub>0</sub>, B<sub>0</sub>, C<sub>1</sub> and C<sub>0</sub> bits are fixed to "1".  
 NOTE2) The functions of the variable 8-grayscale mode are different from those of the fixed 8-grayscale mode.  
 NOTE3) The contents of the DDRAM at "C256=0" are not compatible with the contents at "C256=1".  
 NOTE4) "C256=1" can be used in the 8-bit bus length mode, but not in the 16-bit bus length mode.  
 NOTE5) In the 8-bit bus length mode at "C256=0", odd accesses are prohibited because display data for 1 pixel is completed in successive two accesses.  
 NOTE6) In the 8-bit bus length mode at "C256=0", write upper bits first, then lower bits. This order is always adopted regardless of the "HV", "XD" and "YD" bits.

## (4-4-2) Bit Assignment in Variable 16-grayscale Mode

16-bit Bus Length (MON=0, PWM=0, C256=0, WLS=1)

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	0	X=00H								↔	X=4FH															
Display Data in DDRAM		D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	↔	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>
Grayscale Palette Segment Driver		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA <sub>0</sub>				SEGB <sub>0</sub>				SEGC <sub>0</sub>				↔	SEGA <sub>79</sub>				SEGB <sub>79</sub>				SEGC <sub>79</sub>			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	1	X=00H								↔	X=4FH															
Display Data in DDRAM		D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	↔	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>
Grayscale Palette Segment Driver		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC <sub>0</sub>				SEGB <sub>0</sub>				SEGA <sub>0</sub>				↔	SEGC <sub>79</sub>				SEGB <sub>79</sub>				SEGA <sub>79</sub>			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	0	X=00H								↔	X=4FH															
Display Data in DDRAM		D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
Grayscale Palette Segment Driver		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA <sub>0</sub>				SEGB <sub>0</sub>				SEGC <sub>0</sub>				↔	SEGA <sub>79</sub>				SEGB <sub>79</sub>				SEGC <sub>79</sub>			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	1	X=00H								↔	X=4FH															
Display Data in DDRAM		D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
Grayscale Palette Segment Driver		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC <sub>0</sub>				SEGB <sub>0</sub>				SEGA <sub>0</sub>				↔	SEGC <sub>79</sub>				SEGB <sub>79</sub>				SEGA <sub>79</sub>			



**8-bit Bus Length (MON=0, PWM=0, C256=0, WLS=0)**

ABS	SWAP	Column Address / Display Data / Segment Driver																										
0	0	X=00H(Upper)								X=00H(Lower)					↔	X=4FH(Upper)								X=4FH(Lower)				
Display Data in DDRAM Grayscale Palette Segment Driver		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>		
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C					
		SEGA <sub>0</sub>				SEGB <sub>0</sub>				SEGC <sub>0</sub>				↔	SEGA <sub>79</sub>				SEGB <sub>79</sub>				SEGC <sub>79</sub>					

ABS	SWAP	Column Address / Display Data / Segment Driver																										
0	1	X=00H(Upper)								X=00H(Lower)					↔	X=4FH(Upper)								X=4FH(Lower)				
Display Data in DDRAM Grayscale Palette Segment Driver		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>		
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C					
		SEGC <sub>0</sub>				SEGB <sub>0</sub>				SEGA <sub>0</sub>				↔	SEGC <sub>79</sub>				SEGB <sub>79</sub>				SEGA <sub>79</sub>					

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	0	X=00H (Upper)				X=00H(Lower)								↔	X=4FH (Upper)				X=4FH(Lower)							
Display Data in DDRAM Grayscale Palette Segment Driver		D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA <sub>0</sub>				SEGB <sub>0</sub>				SEGC <sub>0</sub>				↔	SEGA <sub>79</sub>				SEGB <sub>79</sub>				SEGC <sub>79</sub>			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	1	X=00H (Upper)				X=00H(Lower)								↔	X=4FH (Upper)				X=4FH(Lower)							
Display Data in DDRAM Grayscale Palette Segment Driver		D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC <sub>0</sub>				SEGB <sub>0</sub>				SEGA <sub>0</sub>				↔	SEGC <sub>79</sub>				SEGB <sub>79</sub>				SEGA <sub>79</sub>			

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## (4-4-3) Bit Assignment in variable 8-grayscale Mode

8-bit Bus Length (MON=0, PWM=0, C256=1, WLS=0)

ABS	SWAP	Column Address / Display Data / Segment Driver																
*	0	X=00H								↔	X=4FH							
Display Data in DDRAM		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
Grayscale Palette		Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
Segment Driver		SEGA <sub>0</sub>			SEGB <sub>0</sub>			SEGC <sub>0</sub>		↔	SEGA <sub>79</sub>			SEGB <sub>79</sub>			SEGC <sub>79</sub>	

ABS	SWAP	Column Address / Display Data / Segment Driver																
*	1	X=00H								↔	X=4FH							
Display Data in DDRAM		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
Grayscale Palette		Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
Segment Driver		SEGC <sub>0</sub>			SEGB <sub>0</sub>			SEGA <sub>0</sub>		↔	SEGC <sub>79</sub>			SEGB <sub>79</sub>			SEGA <sub>79</sub>	

## (4-4-4) Bit Assignment in Fixed 8-grayscale Mode

16-bit Bus Length (MON=0, PWM=1, C256=0, WLS=1)

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	0	X=00H								↔	X=4FH															
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	↔	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA <sub>0</sub>				SEGB <sub>0</sub>				SEGC <sub>0</sub>				↔	SEGA <sub>79</sub>				SEGB <sub>79</sub>				SEGC <sub>79</sub>			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	1	X=00H								↔	X=4FH															
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	↔	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC <sub>0</sub>				SEGB <sub>0</sub>				SEGA <sub>0</sub>				↔	SEGC <sub>79</sub>				SEGB <sub>79</sub>				SEGA <sub>79</sub>			

NOTE) The data indicated with a slash mark ( / ) are invalid.

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	0	X=00H								↔	X=4FH															
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA <sub>0</sub>				SEGB <sub>0</sub>				SEGC <sub>0</sub>				↔	SEGA <sub>79</sub>				SEGB <sub>79</sub>				SEGC <sub>79</sub>			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	1	X=00H								↔	X=4FH															
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC <sub>0</sub>				SEGB <sub>0</sub>				SEGA <sub>0</sub>				↔	SEGC <sub>79</sub>				SEGB <sub>79</sub>				SEGA <sub>79</sub>			

NOTE) The data indicated with a slash mark ( / ) is invalid.

# NJU6815

## 8-bit Bus Length (MON=0, PWM=1, C256=0, WLS=0)

ABS	SWAP	Column Address / Display Data / Segment Driver																										
0	0	X=00H(Upper)				X=00H(Lower)				↔	X=4FH(Upper)				X=4FH(Lower)													
Display Data in DDRAM		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
	Grayscale Palette	Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C					
	Segment Driver	SEGA <sub>0</sub>				SEGB <sub>0</sub>				SEGC <sub>0</sub>				↔	SEGA <sub>79</sub>				SEGB <sub>79</sub>				SEGC <sub>79</sub>					

ABS	SWAP	Column Address / Display Data / Segment Driver																										
0	1	X=00H(Upper)				X=00H(Lower)				↔	X=4FH(Upper)				X=4FH(Lower)													
Display Data in DDRAM		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
	Grayscale Palette	Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C					
	Segment Driver	SEGC <sub>0</sub>				SEGB <sub>0</sub>				SEGA <sub>0</sub>				↔	SEGC <sub>79</sub>				SEGB <sub>79</sub>				SEGA <sub>79</sub>					

NOTE) The data indicated with a slash mark (/) is invalid.

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	0	X=00H(Upper)				X=00H(Lower)				↔	X=4FH(Upper)				X=4FH(Lower)											
Display Data in DDRAM		D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
	Grayscale Palette	Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
	Segment Driver	SEGA <sub>0</sub>				SEGB <sub>0</sub>				SEGC <sub>0</sub>				↔	SEGA <sub>79</sub>				SEGB <sub>79</sub>				SEGC <sub>79</sub>			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	1	X=00H(Upper)				X=00H(Lower)				↔	X=4FH(Upper)				X=4FH(Lower)											
Display Data in DDRAM		D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
	Grayscale Palette	Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
	Segment Driver	SEGC <sub>0</sub>				SEGB <sub>0</sub>				SEGA <sub>0</sub>				↔	SEGC <sub>79</sub>				SEGB <sub>79</sub>				SEGA <sub>79</sub>			

NOTE) The data indicated with a slash mark (/) is invalid.

## 8-bit Bus Length (MON=0, PWM=1, C256=1, WLS=0)

ABS	SWAP	Column Address / Display Data / Segment Driver																								
*	0	X=00H								↔	X=4FH															
Display Data in DDRAM		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>								
	Grayscale Palette	Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
	Segment Driver	SEGA <sub>0</sub>				SEGB <sub>0</sub>				SEGC <sub>0</sub>				↔	SEGA <sub>79</sub>				SEGB <sub>79</sub>				SEGC <sub>79</sub>			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
*	1	X=00H								↔	X=4FH															
Display Data in DDRAM		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>								
	Grayscale Palette	Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
	Segment Driver	SEGC <sub>0</sub>				SEGB <sub>0</sub>				SEGA <sub>0</sub>				↔	SEGC <sub>79</sub>				SEGB <sub>79</sub>				SEGA <sub>79</sub>			

## (4-4-5) Bit Assignment in B&W Mode

16-bit Bus Length (MON=1, PWM=\*, C256=0, WLS=1)

ABS	SWAP	Column Address / Display Data / Segment Driver																
0	0	X=00H						↔	X=4FH									
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	↔	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>
		Palette A	Palette B	Palette C	↔	Palette A	Palette B	Palette C										
		SEGA <sub>0</sub>	SEGB <sub>0</sub>	SEGC <sub>0</sub>	↔	SEGA <sub>79</sub>	SEGB <sub>79</sub>	SEGC <sub>79</sub>										

ABS	SWAP	Column Address / Display Data / Segment Driver																
0	1	X=00H						↔	X=4FH									
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	↔	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>
		Palette A	Palette B	Palette C	↔	Palette A	Palette B	Palette C										
		SEGC <sub>0</sub>	SEGB <sub>0</sub>	SEGA <sub>0</sub>	↔	SEGC <sub>79</sub>	SEGB <sub>79</sub>	SEGA <sub>79</sub>										

ABS	SWAP	Column Address / Display Data / Segment Driver																
1	0	X=00H						↔	X=4FH									
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	↔	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>
		Palette A	Palette B	Palette C	↔	Palette A	Palette B	Palette C										
		SEGA <sub>0</sub>	SEGB <sub>0</sub>	SEGC <sub>0</sub>	↔	SEGA <sub>79</sub>	SEGB <sub>79</sub>	SEGC <sub>79</sub>										

ABS	SWAP	Column Address / Display Data / Segment Driver																
1	1	X=00H						↔	X=4FH									
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	↔	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>
		Palette A	Palette B	Palette C	↔	Palette A	Palette B	Palette C										
		SEGC <sub>0</sub>	SEGB <sub>0</sub>	SEGA <sub>0</sub>	↔	SEGC <sub>79</sub>	SEGB <sub>79</sub>	SEGA <sub>79</sub>										

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

# NJU6815

8-bit Bus Length (MON=1, PWM=\*, C256=0, WLS=0)

ABS	SWAP	Column Address / Display Data / Segment Driver														
0	0	X=00H(Upper)				↔	X=4FH(Upper)									
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		Palette A			Palette B			Palette C	↔	Palette A			Palette B			Palette C
		SEGA <sub>0</sub>			SEGB <sub>0</sub>			SEGC <sub>0</sub>	↔	SEGA <sub>79</sub>			SEGB <sub>79</sub>			SEGC <sub>79</sub>

ABS	SWAP	Column Address / Display Data / Segment Driver														
0	1	X=00H(Upper)				↔	X=4FH(Upper)									
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		Palette A			Palette B			Palette C	↔	Palette A			Palette B			Palette C
		SEGC <sub>0</sub>			SEGB <sub>0</sub>			SEGA <sub>0</sub>	↔	SEGC <sub>79</sub>			SEGB <sub>79</sub>			SEGA <sub>79</sub>

ABS	SWAP	Column Address / Display Data / Segment Driver																				
1	0	X=00H(Upper)		X=00H(Lower)				↔	X=4FH(Upper)		X=4FH(Lower)											
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	↔	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		Palette A		Palette B		Palette C		↔	Palette A		Palette B		Palette C									
		SEGA <sub>0</sub>		SEGB <sub>0</sub>		SEGC <sub>0</sub>		↔	SEGA <sub>79</sub>		SEGB <sub>79</sub>		SEGC <sub>79</sub>									

ABS	SWAP	Column Address / Display Data / Segment Driver																				
1	1	X=00H(Upper)		X=00H(Lower)				↔	X=4FH(Upper)		X=4FH(Lower)											
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	↔	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		Palette A		Palette B		Palette C		↔	Palette A		Palette B		Palette C									
		SEGC <sub>0</sub>		SEGB <sub>0</sub>		SEGA <sub>0</sub>		↔	SEGC <sub>79</sub>		SEGB <sub>79</sub>		SEGA <sub>79</sub>									

NOTE) The data indicated with a slash mark ( / ) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=\*, C256=1, WLS=0)

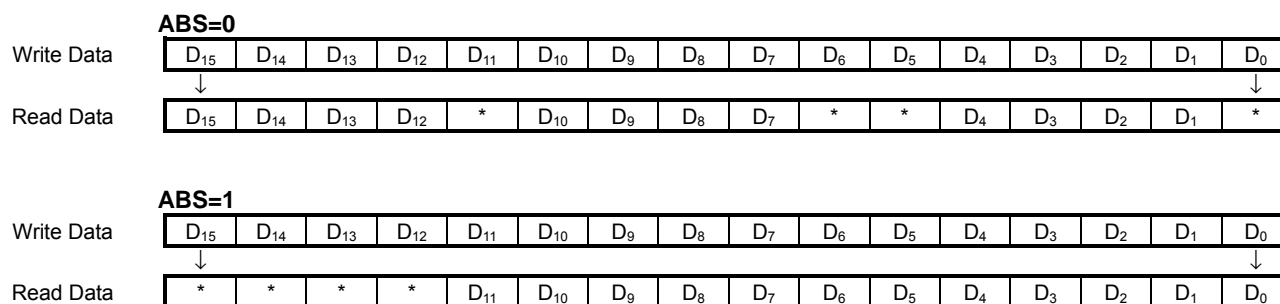
ABS	SWAP	Column Address / Display Data / Segment Driver																
*	0	X=00H								↔	X=4FH							
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
		SEGA <sub>0</sub>			SEGB <sub>0</sub>			SEGC <sub>0</sub>		↔	SEGA <sub>79</sub>			SEGB <sub>79</sub>			SEGC <sub>79</sub>	

ABS	SWAP	Column Address / Display Data / Segment Driver																
*	1	X=00H								↔	X=4FH							
Display Data in DDRAM	Grayscale Palette Segment Driver	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	↔	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
		Palette A			Palette B			Palette C		↔	Palette A			Palette B			Palette C	
		SEGC <sub>0</sub>			SEGB <sub>0</sub>			SEGA <sub>0</sub>		↔	SEGC <sub>79</sub>			SEGB <sub>79</sub>			SEGA <sub>79</sub>	

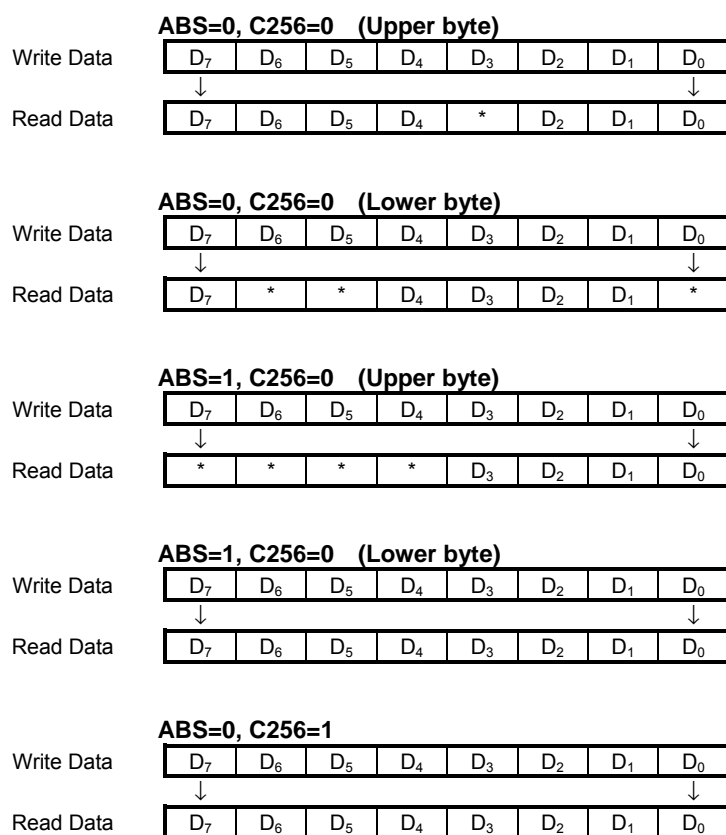
NOTE) The data indicated with a slash mark ( / ) is invalid, and only MSB bits are effective.

## (4-5) Write Data and Read Data

### 16-bit Bus Length



### 8-bit Bus Length



NOTE) \* : Invalid Data

## (5) GRAYSCALE CONTROL CIRCUIT

### (5-1) Display Mode Selection

A display mode is selected by the combination of the D<sub>2</sub> (MON) bit of the “Display Control (1)” instruction and the D<sub>3</sub> (PWM) and D<sub>2</sub> (C256) bits of the “Display Mode Control” instruction, as shown below.

**Table 11 Display Mode Selection**

MON	PWM	C256 (NOTE1)	Display Mode		Bus Length		Oscillation (NOTE2)
0	0	0	Variable 16-grayscale Mode	4096 Colors	8-/16-bit	(WLS=0/1)	f <sub>OSC1</sub>
		1	Variable 8-grayscale Mode	256 Colors	8-bit	(WLS=0)	
	1	0	Fixed 8-grayscale Mode	256 Colors	8-/16-bit	(WLS=0/1)	f <sub>OSC2</sub>
		1			8-bit	(WLS=0)	
1	*	0	B&W Mode	Black & White	8-/16-bit	(WLS=0/1)	f <sub>OSC3</sub>
		1			8-bit	(WLS=0)	

NOTE1) In the variable grayscale mode, “C256” bit selects either 16-grayscale (4K colors) or 8-grayscale (256 colors). When C256=“0” (16-grayscale), all 12 bits are assigned to 1 RGB-pixel. When C256=“1” (8-grayscale), only 8 bits are assigned and the 8-bit bus length should be used. In the fixed 8-grayscale mode or the B&W mode, the “C256” bit is usually “1”. For more information how the display data is assigned, refer to “(4-4) Bit Assignment of Display Data”.

NOTE2) Oscillation frequency is decided according to the display mode, and is fine-tuned by the “Frequency Control” Instruction. Refer to “(10) OSCILLATOR” and “OSCILLATION FREQUENCY AND FRAME FREQUENCY”.

#### (5-1-1) Variable 16-grayscale Mode

In this mode, each of the palettes A<sub>j</sub>, B<sub>j</sub> and C<sub>j</sub> (j=0-15) is capable of selecting 16 from 32 grayscales (0/31-31/31) by setting palette data in the grayscale palette. Then, each of the segment drivers SEG<sub>Ai</sub>, SEG<sub>Bi</sub> and SEG<sub>Ci</sub> (i=0 to 79) generates 16 grayscales to achieve 4,096 colors. Refer to Table 12-1 and Table 12-2.

#### (5-1-2) Variable 8-grayscale Mode

Each of the palettes A<sub>j</sub>, B<sub>j</sub> and C<sub>j</sub> (j=0-15) is capable of selecting 8 from 32 grayscales (0/31-31/31). 2 segment drivers of 1 RGB-group (SEG<sub>Ai</sub>, SEG<sub>Bi</sub> and SEG<sub>Ci</sub> (i=0 to 79)) generate 8 grayscales, and the other driver does 4 grayscales to achieve 256 colors. Refer to Table 13-1 through Table 13-4. The 8-bit bus length is usually used in this mode.

#### (5-1-3) Fixed 8-grayscale Mode

The palette setting is not necessary, because the palettes A<sub>j</sub>, B<sub>j</sub> and C<sub>j</sub> (j=0-15) are always fixed at 4 or 8 grayscales between 0/7 and 7/7. 2 segment drivers of 1 RGB-group (SEG<sub>Ai</sub>, SEG<sub>Bi</sub> and SEG<sub>Ci</sub> (i=0 to 79)) are fixed at 8 grayscales, and the other driver is 4 grayscales, then results in 256 colors. Refer to Table 14-1 and Table 14-2.

#### (5-1-4) B&W Mode

The palette setting is not necessary, where the only MSB bits of display data are valid. Refer to Table 15.



## (6) GRAYSCALE PALETTE

### (6-1) Grayscale Selection in Variable 16-grayscale Mode

**Table 12-1 Grayscale selection**

( Palette Aj, Bj, and Cj )

Display Data MSB---LSB	Palette Name
0 0 0 0	Palette A0/B0/C0
0 0 0 1	Palette A1/B1/C1
0 0 1 0	Palette A2/B2/C2
0 0 1 1	Palette A3/B3/C3
0 1 0 0	Palette A4/B4/C4
0 1 0 1	Palette A5/B5/C5
0 1 1 0	Palette A6/B6/C6
0 1 1 1	Palette A7/B7/C7
1 0 0 0	Palette A8/B8/C8
1 0 0 1	Palette A9/B9/C9
1 0 1 0	Palette A10/B10/C10
1 0 1 1	Palette A11/B11/C11
1 1 0 0	Palette A12/B12/C12
1 1 0 1	Palette A13/B13/C13
1 1 1 0	Palette A14/B14/C14
1 1 1 1	Palette A15/B15/C15

**Table 12-2 Grayscale Palette**

( Palette Aj, Bj, and Cj )

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0	Palette A0/B0/C0	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette A8/B8/C8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette A2/B2/C2	1 0 1 0 1	21/31	Palette A10/B10/C10
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette A4/B4/C4	1 1 0 0 1	25/31	Palette A12/B12/C12
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette A6/B6/C6	1 1 1 0 1	29/31	Palette A14/B14/C14
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=0"

NOTE2) Applied to palette Aj, Bj and Cj (j=0 to 15)

## (6-2) Grayscale Selection in Variable 8-grayscale Mode

**Table 13-1 Grayscale selection**

( Palette Aj and Bj )

Display Data MSB---LSB	Palette Name
0 0 0 *	Palette A1/B1/C1
0 0 1 *	Palette A3/B3/C3
0 1 0 *	Palette A5/B5/C5
0 1 1 *	Palette A7/B7/C7
1 0 0 *	Palette A9/B9/C9
1 0 1 *	Palette A11/B11/C11
1 1 0 *	Palette A13/B13/C13
1 1 1 *	Palette A15/B15/C15

**Table 13-2 Grayscale Palette**

( Palette Aj and Bj )

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0	0		1 0 0 0	16/31	
0 0 0 1	1/31		1 0 0 1	17/31	
0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=1".

NOTE2) Applied to palette Aj and Bj (j=0 to 15)

NOTE3) Palette 0, 2, 4, 6, 8, 10, 12 and 14 are disabled.

**Table 13-3 Grayscale selection**

( Palette Cj )

Display Data MSB---LSB	Palette Name
0 0 **	Palette A3/B3/C3
0 1 **	Palette A7/B7/C7
1 0 **	Palette A11/B11/C11
1 1 **	Palette A15/B15/C15

**Table 13-4 Grayscale Palette**

( Palette Cj )

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0	0		1 0 0 0	16/31	
0 0 0 1	1/31		1 0 0 1	17/31	
0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=1"

NOTE2) Applied to palette Cj (j=0 to 15)

NOTE3) Palette 0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13 and 14 are disabled.

## (6-3) Grayscale Selection in Fixed 8-grayscale Mode

**Table 14-1 Grayscale Selection**

( Palette Aj and Bj )

Display Data MSB- - - -LSB	Grayscale
0 0 0 *	0/7
0 0 1 *	1/7
0 1 0 *	2/7
0 1 1 *	3/7
1 0 0 *	4/7
1 0 1 *	5/7
1 1 0 *	6/7
1 1 1 *	7/7

**Table 14-2 Grayscale Palette**

( Palette Cj )

Display Data MSB- - - -LSB	Grayscale
0 0 **	0/7
0 1 **	3/7
1 0 **	5/7
1 1 **	7/7

NOTE1) "MON=0", "PWM=1", "C256=0 or 1"

## (6-4) Grayscale Selection in B&W Mode

**Table 15 Grayscale Selection**

Display Data MSB- - - -LSB	Grayscale
0 ***	0
1 ***	1

NOTE1) "MON=1", "PWM=0 or 1" and "C256=0 or 1"

## (7) DISPLAY TIMING GENERATOR

The display timing generator generates timing clocks such as the CL (Line Clock), FR (Frame Rate) and FLM (First Line Maker) by dividing an oscillation frequency. These clocks are used inside the LSI, and are activated by setting "1" at the D<sub>0</sub> (SON) bit of the "Duty-1 /Display Clock ON/OFF" instruction.

The CL is used for the line counter and the data latch circuit. At the rising edge of the CL signal, the line counter is counted up, then 240-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit, then segment drivers A<sub>i</sub>, B<sub>i</sub> and C<sub>i</sub> (i=0 to 79) produce LCD driving waveforms. The internal data-transmission timing between the DDRAM and segment drivers is completely independent of external data-transmission timing, so that MPU makes access to the LSI without concern for the LSI's internal operation.

The FR and FLM are generated by the CL. The FR toggles once every frame in the default status, and is programmed to toggle once every N lines. And the FLM is used to specify an initial display line, which is preset whenever the FLM becomes "H".

## (8) DATA LATCH CIRCUIT

The data latch circuit is used to temporarily store display data which is released to the grayscale control circuit. The display data in this circuit is updated in synchronization with the CL. The "All Pixels ON/OFF", "Display ON/OFF" and "Reverse Display ON/OFF" instructions control the data in this circuit, but does not change the data in the DDRAM.

## (9) COMMON DRIVERS AND SEGMENT DRIVERS

The LSI includes 128-common drivers and 240-segment drivers. The common drivers generate LCD driving waveforms formed on the V<sub>LCD</sub>, V<sub>1</sub>, V<sub>4</sub> and V<sub>SSH</sub> levels. The segment drivers generate waveforms formed on the V<sub>LCD</sub>, V<sub>2</sub>, V<sub>3</sub> and V<sub>SSH</sub> levels.

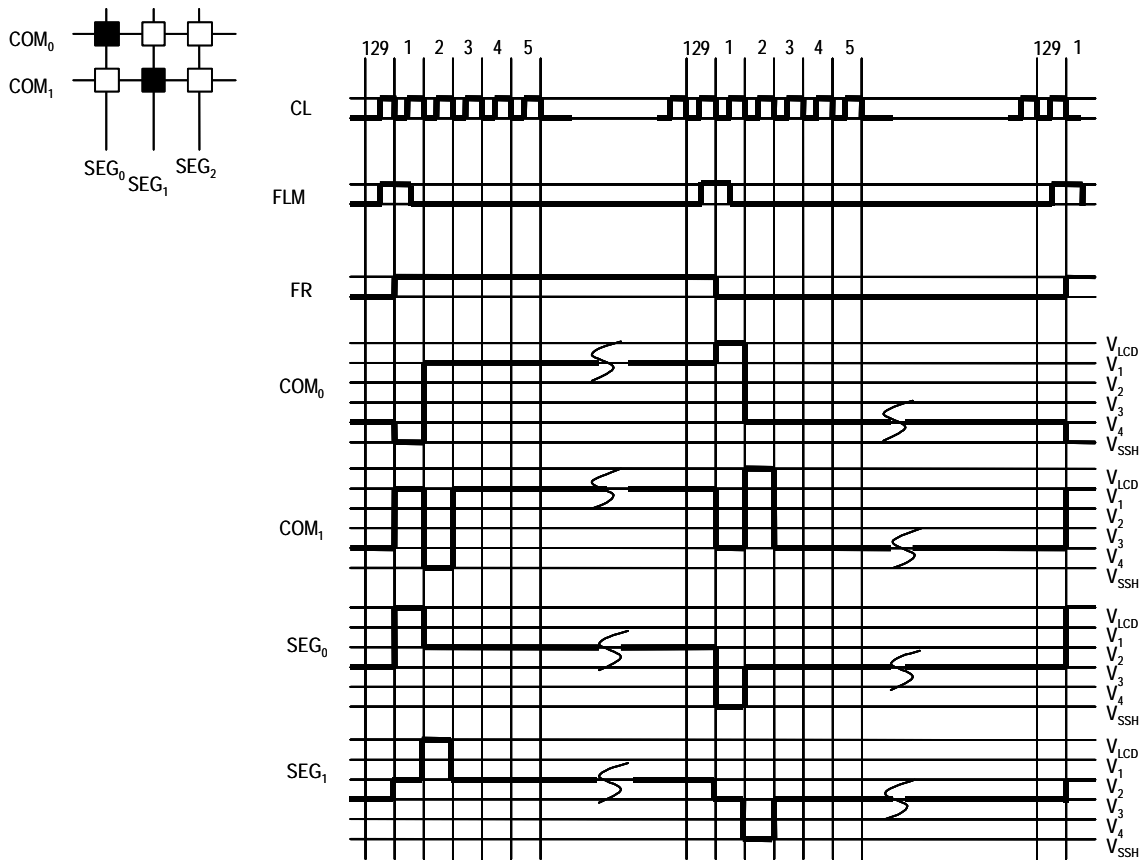


Fig 9 LCD Driving Waveforms (B&W Mode, Color Reverse OFF, 1/129 Duty)

## (10) OSCILLATOR

The oscillator is equipped with a resistor and a capacitor, and generates internal clocks used for the display timing generator and the voltage booster. The internal resistor is enabled by setting “0” at the D<sub>1</sub> (CKS) bit of the “Bus Length” instruction. For more accurate frequency, using an external resistor or external clock is recommended.

When using the internal resistor, the resistance is controlled to optimize frame frequency for different LCD panels, by setting the D<sub>2</sub>-D<sub>0</sub> (RF2-RF0) bits of the “Frequency Control” instruction. For more safety, make sure what is the best frequency in the particular application.

### (10-1) Using Internal Resistor (CKS=0)

In this case, the OSC1 should be fixed at “H” or “L” and the OSC2 is open. The oscillation frequency is varied according to the display mode, as follows.

**Table 16 Oscillation Frequency vs. Display Mode**

Symbol	MON	PWM	Display Mode
f <sub>OSC1</sub>	0	0	Variable 8-/16-grayscale Mode
f <sub>OSC2</sub>	0	1	Fixed 8-grayscale Mode
f <sub>OSC3</sub>	1	*	B&W Mode

\*: Don't care

### (10-2) Using External Resistor (CKS=1)

Be sure to connect the OSC1 and OSC2 with an external resistor. The frequency of the oscillator should be adjusted to the same value generated by the internal resistor.

### (10-3) Using External Clock (CKS=1)

Input external clock to the OSC1 and leave the OSC2 open. The external clock with 50% duty is recommended. The frequency of the external clock should be the same value generated by the internal resistor.

## (11) LCD POWER SUPPLY

The internal LCD power supply is organized into the voltage converter and the voltage booster. The voltage converter consists of the reference voltage generator, the voltage regulator with EVR and the LCD bias voltage generator. The configuration of the LCD power supply is arranged by setting the D<sub>3</sub> (AMPON) and D<sub>1</sub> (DCON) bits of the “Power Control” instruction. For this configuration, the internal LCD power supply can be partially used in combination with an external supply voltage, as shown in Table 17.

**Table 17 Configuration of LCD Power Supply**

DCON	AMPON	Voltage Booster	Voltage Converter	External Supply Voltage	NOTE
0	0	Inactive	Inactive	V <sub>OUT</sub> , V <sub>LCD</sub> , V <sub>1</sub> , V <sub>2</sub> , V <sub>3</sub> , V <sub>4</sub>	1, 3, 4
0	1	Inactive	Active	V <sub>OUT</sub>	2, 3, 4
1	1	Active	Active	—	-

NOTE1) No internal LCD power supply is used. The LCD bias voltages are externally supplied, and the C<sub>1+</sub>, C<sub>1-</sub>, C<sub>2+</sub>, C<sub>2-</sub>, C<sub>3+</sub>, C<sub>3-</sub>, C<sub>4+</sub>, C<sub>4-</sub>, C<sub>5+</sub>, C<sub>5-</sub>, V<sub>REF</sub>, V<sub>REG</sub> and V<sub>EE</sub> are open.

NOTE2) Only the voltage converter is used. The V<sub>OUT</sub> is externally supplied, and the C<sub>1+</sub>, C<sub>1-</sub>, C<sub>2+</sub>, C<sub>2-</sub>, C<sub>3+</sub>, C<sub>3-</sub>, C<sub>4+</sub>, C<sub>4-</sub>, C<sub>5+</sub>, C<sub>5-</sub> and V<sub>EE</sub> are open. The reference voltage is supplied on the V<sub>REF</sub>.

NOTE3) The following relation among each LCD bias voltages must be maintained.

$$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SSH}$$

NOTE4) If the internal LCD power supply doesn't have enough capability to drive the particular LCD panel, use the external LCD power supply. Otherwise, it may affect display quality.

## (11-1) Voltage Booster

The internal voltage booster generates up to  $6xV_{EE}$  voltage. The boost level is selected from 2x, 3x, 4x, 5x or 6x by setting the  $D_2$ - $D_0$  ( $VU_2$ - $VU_0$ ) bits of the "Boost Level" instruction. The boost voltage  $V_{OUT}$  must not exceed 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

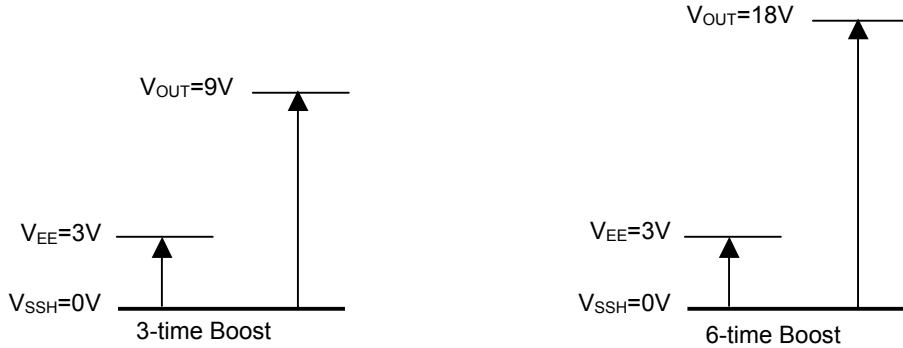


Fig 10 Boost Voltage

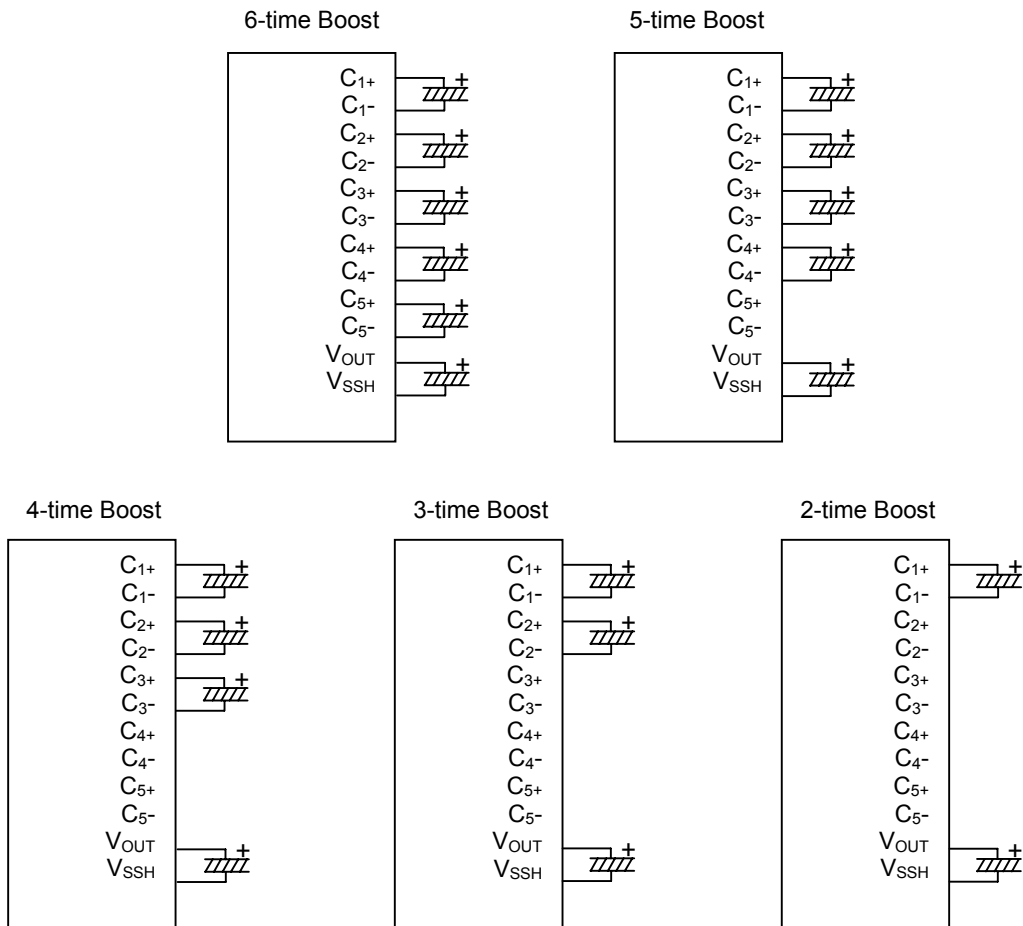


Fig 11 External Capacitor Connection of Voltage Booster

## (11-2) Voltage Converter

### (11-2-1) Reference Voltage Generator

The reference voltage generator produces the reference voltage ( $V_{BA}=0.9 \times V_{EE}$ ). When using the internal LCD power supply, connect the  $V_{BA}$  and the  $V_{REF}$ , or supply  $0.9 \times V_{EE}$  or lower voltage on the  $V_{REF}$ . When using an external LCD power supply, the  $V_{BA}$  should be open. Refer to Fig 12, 14 and 15.

### (11-2-2) Voltage Regulator

The voltage regulator consists of an operational amplifier with gain control and EVR. The  $V_{REF}$  voltage is multiplied to obtain the  $V_{REG}$  voltage, and its multiple (boost level) is set by the  $D_2$ - $D_0$  (VU2-VU0) bits of the “Boost Level” instruction. The formula is shown below.

$$V_{REG} = V_{REF} \times N \quad (N: \text{Boost Level})$$

### (11-2-3) Electrical Variable Resistor (EVR)

The EVR is used to fine-tune the  $V_{LCD}$  voltage to optimize display contrast. The EVR value is controlled in 128 steps by setting the  $D_2$ - $D_0$  (DV<sub>2</sub>-DV<sub>0</sub>) bits of the “EVR Control” instruction. The formula is shown below.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \quad (M: \text{EVR Value})$$

### (11-2-4) LCD Bias Voltage Generator

The LCD bias voltage generator consists of buffer amplifiers and bleeder resistors to generate the LCD bias voltages such as the  $V_{LCD}$ ,  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$ , and its bias ratio is selected from 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11 and 1/12.

As shown in Fig 12, when using only the internal LCD power supply, the capacitors CA2 are connected to the  $V_{LCD}$ ,  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$  respectively.

As shown in Fig 13, when using no internal LCD power supply, the LCD bias voltages are externally supplied on the  $V_{LCD}$ ,  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$ , and the internal LCD power supply should be turned off by setting “0” at the “DCON” and “AMPON” bits. And the  $C_{1+}$ ,  $C_{1-}$ ,  $C_{2+}$ ,  $C_{2-}$ ,  $C_{3+}$ ,  $C_{3-}$ ,  $C_{4+}$ ,  $C_{4-}$ ,  $C_{5+}$ ,  $C_{5-}$ ,  $V_{EE}$ ,  $V_{REF}$  and  $V_{REG}$  are open.

Fig 14 and 15 show typical peripheral circuits when partially using the LCD power supply without the reference voltage generator.

Fig 16 shows the circuit when partially using the LCD power supply without the voltage booster.

## (11-3) External Components for LCD Power Supply

Using Only Internal LCD Power Supply (6x boost)

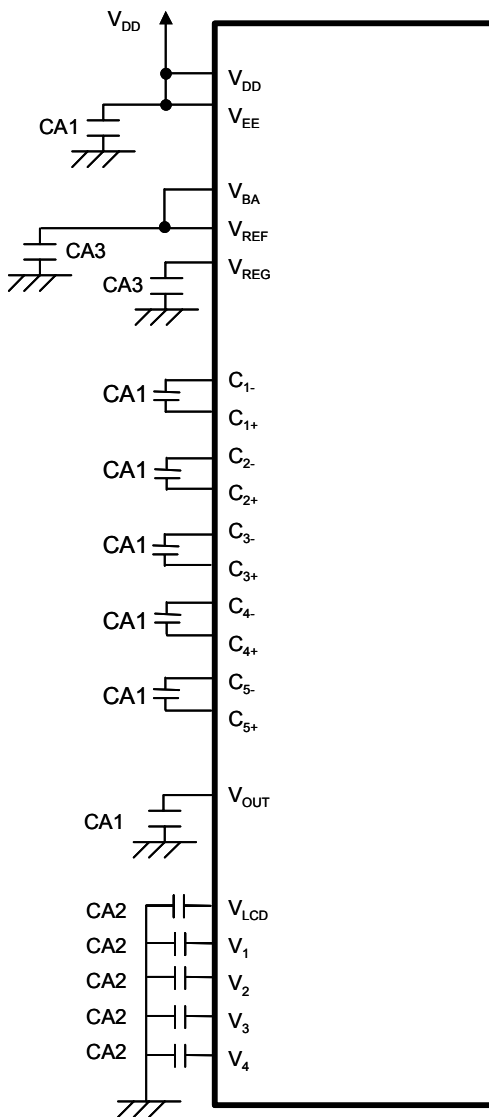


Fig 12

Using Only External LCD Power Supply

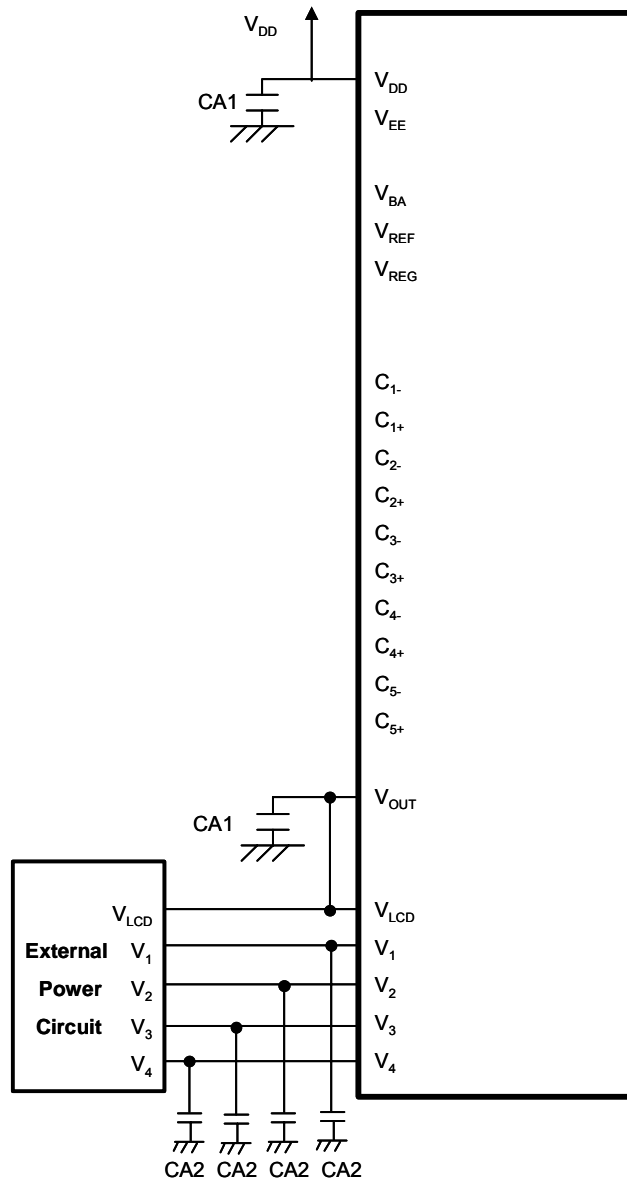


Fig 13

Reference Values

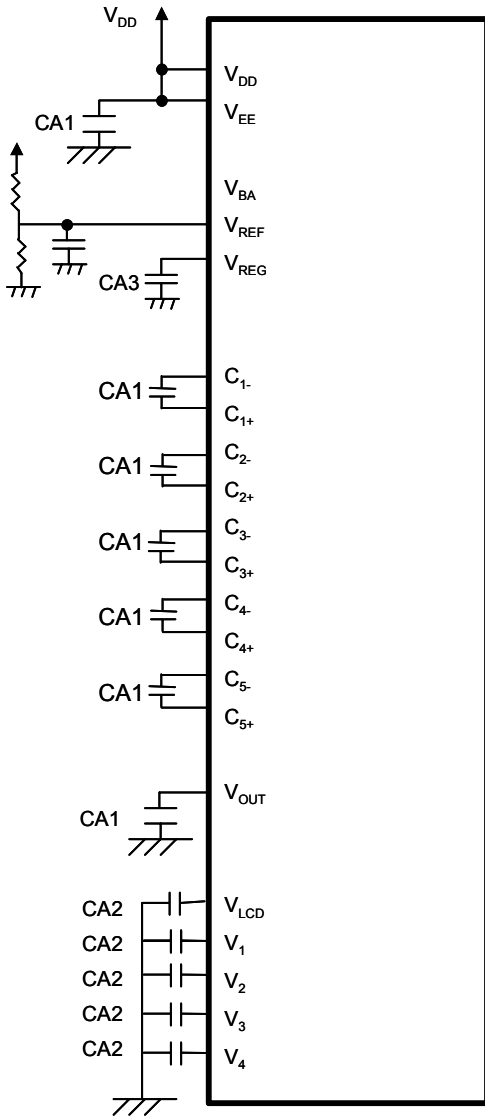
CA1	1.0 to 4.7 $\mu$ F
CA2	1.0 to 2.2 $\mu$ F
CA3	0.1 $\mu$ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines ( $V_{DD}$ ,  $V_{SS}$ ,  $V_{EE}$ ,  $V_{SSH}$ ,  $V_{OUT}$ ,  $V_{LCD}$ ,  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$ ) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

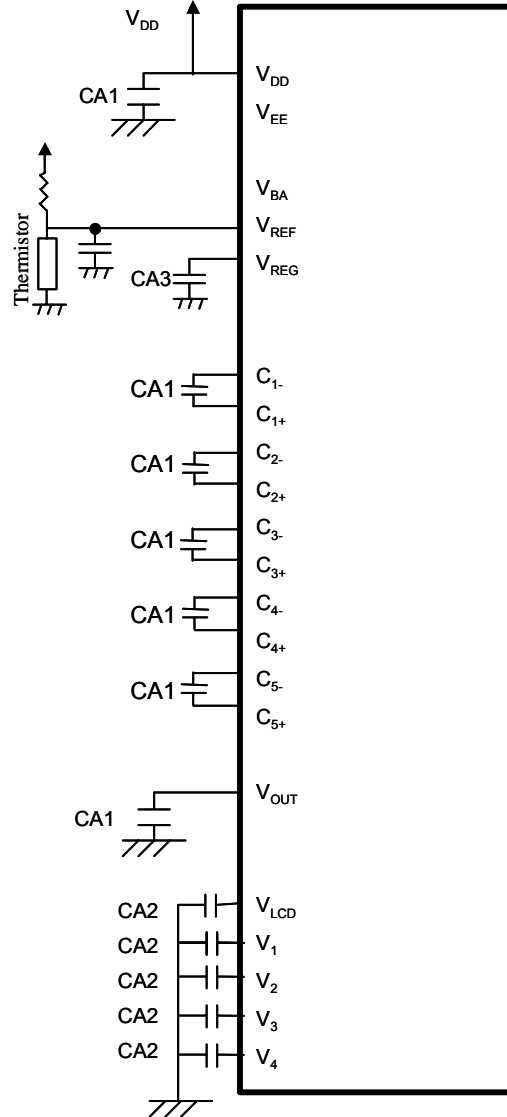


**Using Internal LCD Power Supply  
Without Reference Voltage Generator(1)  
(6x boost)**



**Fig 14**

**Using Internal LCD Power Supply  
Without Reference Voltage Generator(1)  
(6x boost)**



**Fig 15**

**Reference Values**

CA1	1.0 to 4.7 $\mu$ F
CA2	1.0 to 2.2 $\mu$ F
CA3	0.1 $\mu$ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines ( $V_{DD}$ ,  $V_{SS}$ ,  $V_{EE}$ ,  $V_{SSH}$ ,  $V_{OUT}$ ,  $V_{LCD}$ ,  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$ ) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

## Using Internal LCD Power Supply Without Voltage Booster

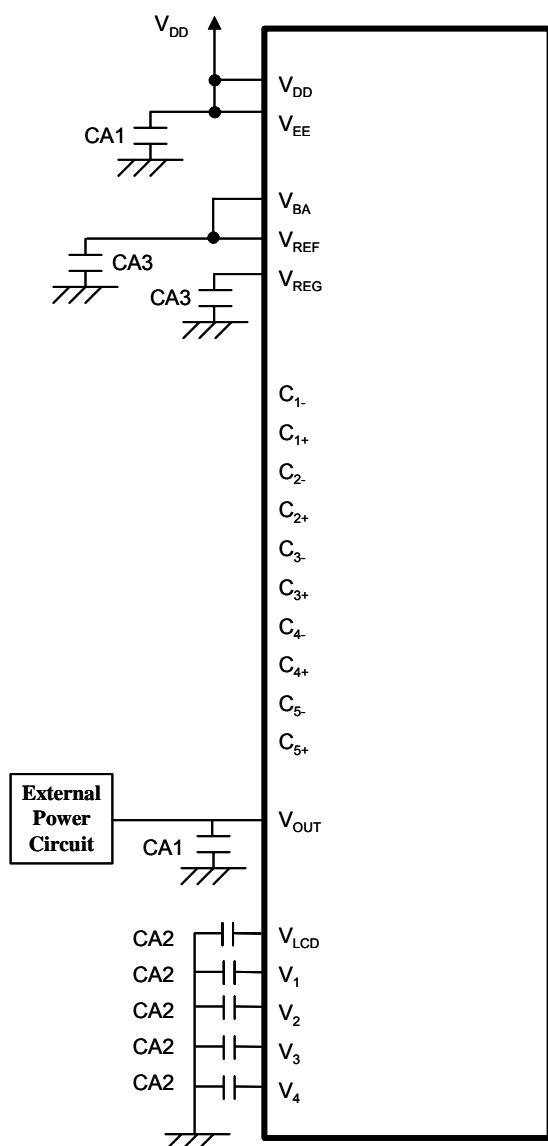


Fig 16

### Reference Values

CA1	1.0 to 4.7 $\mu$ F
CA2	1.0 to 2.2 $\mu$ F
CA3	0.1 $\mu$ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines ( $V_{DD}$ ,  $V_{SS}$ ,  $V_{EE}$ ,  $V_{SSH}$ ,  $V_{OUT}$ ,  $V_{LCD}$ ,  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$ ) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

## (11-4) Discharge Circuit

The LSI incorporates two discharge circuits which are independently controlled for the  $V_{LCD}$  and  $V_1$ - $V_4$  and for the  $V_{OUT}$ . The  $V_{LCD}$  and  $V_1$ - $V_4$  are discharged by setting "1" at the  $D_0$  (DIS) bit of the "Discharge ON/OFF" instruction or the reset by the RESb. And the  $V_{OUT}$  (100K $\Omega$  internal resistor between  $V_{OUT}$  and  $V_{EE}$ ) is discharged by setting "1" at the  $D_1$  (DIS2) bit of this instruction. Be sure to turned off the internal or external LCD power supply when this instruction is executed, otherwise it may function as a current load and affect an operating current. Refer to "(14-22) Discharge ON/OFF".

## (11-5) Power ON/OFF

To protect the LSI from overcurrent, the following sequences must be maintained to turn on and off the power supply. In addition to the following discussions, refer to "(18) TYPICAL INSTRUCTION SEQUENCES".

### (11-5-1) Power ON/OFF in Using Internal LCD Power Supply

#### Power ON

First " $V_{DD}$  and  $V_{EE}$  ON", next "Reset by RESb", then "Internal LCD power supply ON". Be sure to execute the "Display ON" instruction later than the completion of this power ON sequence. Otherwise, unexpected pixels may be turned on instantly.

#### Power OFF

First "Reset by RESb or "HALT" instruction", next " $V_{DD}$  and  $V_{EE}$  OFF". If using different power sources for the  $V_{DD}$  and the  $V_{EE}$  individually, the  $V_{EE}$  must be turned off after the reset or the "HALT". After that, the  $V_{DD}$  can be turned off, waiting until the LCD bias voltages ( $V_{LCD}$ ,  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$ ) drop below the threshold level of LCD pixels.

### (11-5-2) Power ON/OFF in Using External LCD Power Supply

#### Power ON

First " $V_{DD}$  and  $V_{EE}$  ON", next "Reset by RESb", then "External LCD power supply ON". When using only external  $V_{OUT}$ , first " $V_{DD}$  ON", next "Reset by RESb", then "External  $V_{OUT}$  ON", as well.

#### Power OFF

First "Reset by RESb or "HALT" instruction" to isolate external LCD bias voltages, next " $V_{DD}$  OFF". For more safety, placing a resistor in series on the  $V_{LCD}$  line (or the  $V_{OUT}$  line in using only the external  $V_{OUT}$ ) is recommended. That resistance is usually between 50 $\Omega$  and 100 $\Omega$ .

## (12) RESET FUNCTION

The reset function initializes the LSI to the following default status by setting the RESb to “L”. Connecting the RESb with MPU’s reset is recommended so that the LSI and MPU is initialized at a time.

### Default Status

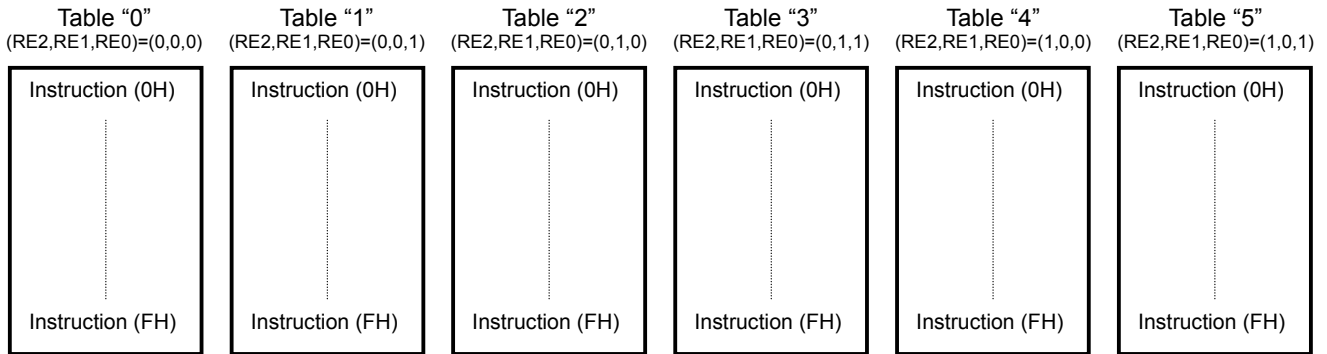
1. Display Data in DDRAM	:Undefined
2. Window Start Column Address	:(00)H
3. Window Start Row Address	:(00)H
4. Initial Display Line	:(0)H (1st line)
5. Display ON/OFF	:OFF
6. Reverse Display ON/OFF	:OFF (Normal)
7. Duty Cycle Ratio	:1/129 Duty (DSE=0)
8. N-line Inversion ON/OFF	:OFF
9. COM Scan Direction	:COM <sub>0</sub> → COM <sub>127</sub>
10. Increment/Decrement Control	:(HV, XD, YD)=(0, 0, 0)
11. Read-modify-write	:OFF (AIM=0)
12. Swap	:OFF (Normal)
13. EVR Value	:(0, 0, 0, 0, 0, 0, 0)
14. Internal LCD Power Supply	:OFF
15. Display Mode	:Grayscale Mode
16. LCD Bias Ratio	:1/9 Bias
17. Palette 0	:(0, 0, 0, 0, 0)
18. Palette 1	:(0, 0, 0, 1, 1)
19. Palette 2	:(0, 0, 1, 0, 1)
20. Palette 3	:(0, 0, 1, 1, 1)
21. Palette 4	:(0, 1, 0, 0, 1)
22. Palette 5	:(0, 1, 0, 1, 1)
23. Palette 6	:(0, 1, 1, 0, 1)
24. Palette 7	:(0, 1, 1, 1, 1)
25. Palette 8	:(1, 0, 0, 0, 1)
26. Palette 9	:(1, 0, 0, 1, 1)
27. Palette 10	:(1, 0, 1, 0, 1)
28. Palette 11	:(1, 0, 1, 1, 1)
29. Palette 12	:(1, 1, 0, 0, 1)
30. Palette 13	:(1, 1, 0, 1, 1)
31. Palette 14	:(1, 1, 1, 0, 1)
32. Palette 15	:(1, 1, 1, 1, 1)
33. Display Mode Control	:Variable 16-grayscale Mode (4,096 Colors)
34. Bus Length	:8-bit Bus Length
35. Discharge ON/OFF	:OFF (DIS,DIS2)=(0,0)

(13) INSTRUCTION TABLES

(13-1) Instruction Table and Register Address

The LSI incorporates 6 instruction tables as shown in Fig 17, and each instruction table has a specific address in between “0” and “5”. And each instruction register has a specific address in between (0H) and (FH), and instruction is read out from the register by the “Register Address” and “Register Read” instructions.

Fig 18 shows part of the instruction sequence, where the instruction table should be specified prior to other instructions. However, when some instructions of the same table are sequentially executed, the table selection may be omitted. In addition, the “Display Data Write”, “Display Data Read” and “Register Read” instructions can be performed in any table.



NOTE) Address (FH) is assigned to “Instruction Table Select” in any table.

Fig 17 Instruction Table Overview

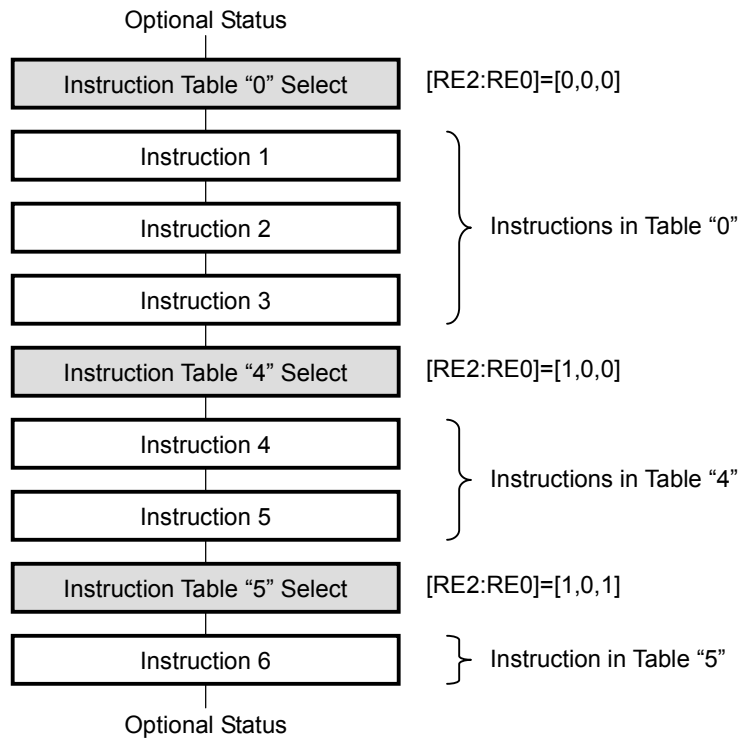


Fig 18 Outline of Instruction Sequence

## (13-2) Instruction Table 0 (RE2, RE1, RE0)=(0, 0, 0)

Instructions/ Register Address [NH]	Code (80 Series MPU I/F)							Code								Functions	
	CSb	RS	RDb	WRb	RE2	RE1	RE0	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		
1	Display Data Write	0	0	1	0	0/1	0/1	0/1	Write Data								Writing Display Data
2	Display Data Read	0	0	0	1	0/1	0/1	0/1	Read Data								Reading Display Data
3	Window Start Column Address (Lower) [0H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Setting Column Address for start point
	Window Start Column Address (Upper) [1H]	0	1	1	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	Setting Column Address for start point	
4	Window Start Row Address (Lower) [2H]	0	1	1	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Setting Row Address for start point	
	Window Start Row Address (Upper) [3H]	0	1	1	0	0	0	0	0	1	1	*	AY6	AY5	AY4	Setting Row Address for start point	
5	Initial Display Line (Lower) [4H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Setting Row Address for Initial COM
	Initial Display Line (Upper) [5H]	0	1	1	0	0	0	0	0	1	0	1	*	LA6	LA5	LA4	Setting Row Address for Initial COM
6	N-line Inversion (Lower) [6H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	Setting the Number of N-line Inversion
	N-line Inversion (Upper) [7H]	0	1	1	0	0	0	0	0	1	1	1	*	N6	N5	N4	Setting the Number of N-line Inversion
7	Display Control (1) [8H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/OFF	SHIFT : Common Scan Direction MON : Grayscale/B/W Mode ALLON : All Pixels ON/OFF ON/OFF : Display ON/OFF
8	Display Control (2) [9H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	*	REV : Reverse Display ON/OFF NLIN : N-line Inversion ON/OFF SWAP : SWAP ON/OFF
9	Increment/Decrement Control [AH]	0	1	1	0	0	0	0	1	0	1	0	AIM	HV	XD	YD	AIM : Read-Modify-Write ON/OFF HV : Horizontal/ Vertical Direction XD : X Increment / Decrement YD : Y Increment / Decrement
10	Power Control [BH]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON : Voltage Converter ON/OFF HALT : Power Save ON/OFF DCON : Voltage Booster ON/OFF ACL : Reset
11	Duty Cycle Ratio [CH]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Setting LCD Duty Cycle Ratio
12	Boost Level [DH]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	Setting Boost Level
13	LCD Bias Ratio [EH]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Setting LCD Bias Ratio
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) \* : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

**(13-3) Instruction Table 1 (RE2, RE1, RE0)=(0, 0, 1)**

Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Palette A0/A8 (Lower) [0H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Setting Palette Data : A0(PS=0) /A8(PS=1)
Palette A0/A8 (Upper) [1H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Setting Palette Data : A0(PS=0) /A8(PS=1)
Palette A1/A9 (Lower) [2H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Setting Palette Data : A1(PS=0) /A9(PS=1)
Palette A1/A9 (Upper) [3H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Setting Palette Data : A1(PS=0) /A9(PS=1)
Palette A2/A10 (Lower) [4H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Setting Palette Data : A2(PS=0) /A10(PS=1)
Palette A2/A10 (Upper) [5H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Setting Palette Data : A2(PS=0) /A10(PS=1)
Palette A3/A11 (Lower) [6H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/P A112	PA31/ PA111	PA30/ PA110	Setting Palette Data : A3(PS=0) /A11(PS=1)
Palette A3/A11 (Upper) [7H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Setting Palette Data : A3(PS=0) /A11(PS=1)
Palette A4/A12 (Lower) [8H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/P A122	PA41/ PA121	PA40/ PA120	Setting Palette Data : A4(PS=0) /A12(PS=1)
Palette A4/A12 (Upper) [9H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Setting Palette Data : A4(PS=0) /A12(PS=1)
Palette A5/A13 (Lower) [AH]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/P A132	PA51/ PA131	PA50/ PA130	Setting Palette Data : A5(PS=0) /A13(PS=1)
Palette A5/A13 (Upper) [BH]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Setting Palette Data : A5(PS=0) /A13(PS=1)
Palette A6/A14 (Lower) [CH]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/P A142	PA61/ PA141	PA60/ PA140	Setting Palette Data : A6(PS=0) /A14(PS=1)
Palette A6/A14 (Upper) [DH]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Setting Palette Data : A6(PS=0) /A14(PS=1)
14 Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) \* : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-4) Instruction Table 2 (RE2, RE1, RE0)=(0, 1, 0)

Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code							Functions	
	CSb	RS	RDb	WRb	RE2	RE1	RE0	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>		D <sub>0</sub>
Palette A7/A15 (Lower) [0H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/P A152	PA71/ PA151	PA70/ PA150	Setting Palette Data : A7(PS=0) /A15(PS=1)
Palette A7/A15 (Upper) [1H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Setting Palette Data : A7(PS=0) /A15(PS=1)
Palette B0/B8 (Lower) [2H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Setting Palette Data : B0(PS=0) /B8(PS=1)
Palette B0/B8 (Upper) [3H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PB84	Setting Palette Data : B0(PS=0) /B8(PS=1)
Palette B1/B9 (Lower) [4H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Setting Palette Data : B1(PS=0) /B9(PS=1)
Palette B1/B9 (Upper) [5H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Setting Palette Data : B1(PS=0) /B9(PS=1)
Palette B2/B10 (Lower) [6H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Setting Palette Data : B2(PS=0) /B10(PS=1)
Palette B2/B10 (Upper) [7H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Setting Palette Data : B2(PS=0) /B10(PS=1)
Palette B3/B11 (Lower) [8H]	0	1	1	0	0	1	0	1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Setting Palette Data : B3(PS=0) /B11(PS=1)
Palette B3/B11 (Upper) [9H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Setting Palette Data : B3(PS=0) /B11(PS=1)
Palette B4/B12 (Lower) [AH]	0	1	1	0	0	1	0	1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Setting Palette Data : B4(PS=0) /B12(PS=1)
Palette B4/B12 (Upper) [BH]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Setting Palette Data : B4(PS=0) /B12(PS=1)
Palette B5/B13 (Lower) [CH]	0	1	1	0	0	1	0	1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Setting Palette Data : B5(PS=0) /B13(PS=1)
Palette B5/B13 (Upper) [DH]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Setting Palette Data : B5(PS=0) /B13(PS=1)
14 Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Tablet

NOTE1) \* : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.



**(13-5) Instruction Table 3 (RE2, RE1, RE0)=(0, 1, 1)**

Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code							Functions	
	CSb	RS	RD <sub>b</sub>	WR <sub>b</sub>	RE2	RE1	RE0	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>		D <sub>0</sub>
Palette B6/B14 (Lower) [0H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Setting Palette Data : B6(PS=0) /B14(PS=1)
Palette B6/B14 (Upper) [1H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Setting Palette Data : B6(PS=0) /B14(PS=1)
Palette B7/B15 (Lower) [2H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Setting Palette Data : B7(PS=0) /B15(PS=1)
Palette B7/B15 (Upper) [3H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Setting Palette Data : B7(PS=0) /B15(PS=1)
Palette C0/C8 (Lower) [4H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Setting Palette Data : C0(PS=0) /C8(PS=1)
Palette C0/C8 (Upper) [5H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Setting Palette Data : C0(PS=0) /C8(PS=1)
Palette C1/C9 (Lower) [6H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Setting Palette Data : C1(PS=0) /C9(PS=1)
Palette C1/C9 (Upper) [7H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Setting Palette Data : C1(PS=0) /C9(PS=1)
Palette C2/C10 (Lower) [8H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Setting Palette Data : C2(PS=0) /C10(PS=1)
Palette C2/C10 (Upper) [9H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Setting Palette Data : C2(PS=0) /C10(PS=1)
Palette C3/C11 (Lower) [AH]	0	1	1	0	0	1	1	1	0	1	0	PC33P C113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Setting Palette Data : C3(PS=0) /C11(PS=1)
Palette C3/C11 (Upper) [BH]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Setting Palette Data : C3(PS=0) /C11(PS=1)
Palette C4/C12 (Lower) [CH]	0	1	1	0	0	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Setting Palette Data : C4(PS=0) /C12(PS=1)
Palette C4/C12 (Upper) [DH]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44/ PC124	Setting Palette Data : C4(PS=0) /C12(PS=1)
14 Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) \* : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-6) Instruction Table 4 (RE2, RE1, RE0)=(1, 0, 0)

Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code							Functions	
	CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1		D0
15 Palette C5/C13 (Lower) [0H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Setting Palette Data : C5(PS=0) /C13(PS=1)
Palette C5/C13 (Upper) [1H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Setting Palette Data : C5(PS=0) /C13(PS=1)
Palette C6/C14 (Lower) [2H]	0	1	1	0	1	0	0	0	0	1	0	PC63/P C143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Setting Palette Data : C6(PS=0) /C14(PS=1)
Palette C6/C14 (Upper) [3H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC144	Setting Palette Data : C6(PS=0) /C14(PS=1)
Palette C7/C15 (Lower) [4H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Setting Palette Data : C7(PS=0) /C15(PS=1)
Palette C7/C15 (Upper) [5H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Setting Palette Data : C7(PS=0) /C15(PS=1)
16 Initial COM [6H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Setting start COM for scanning
17 Duty-1 /Display Clock ON/OFF [7H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display Clock ON/OFF DSE : Duty-1 ON/OFF
18 Display Mode Control [8H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	*	*	PWM : Variable/Fixed Grayscale Mode C256 : 256-color Mode ON/OFF
19 Bus Length [9H]	0	1	1	0	1	0	0	1	0	0	1	*	ABS	CKS	WLS	ABS : Bit Assignment CKS : Oscillator Set WLS : 8-/16-bit Bus Length
20 EVR Control (Lower) [AH]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Setting EVR Value (Lower Bit)
EVR Control (Upper) [BH]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Setting EVR Value (Upper Bit)
21 Frequency Control [DH]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Adjusting Oscillation Frequency
22 Discharge ON/OFF [EH]	0	1	1	0	1	0	0	1	1	1	0	*	*	DIS2	DIS	Discharge ON/OFF
23 Register Address [CH]	0	1	1	0	1	0	0	1	1	0	0	Register Address				Setting Register Address
24 Register Read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data				Reading Instruction
14 Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table Select

NOTE1) \* : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

**(13-7) Instruction Table 5 (RE2, RE1, RE0)=(1, 0, 1)**

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	
25	Window End Column Address (Lower) [0H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Setting Column Address for end point
	Window End Column Address (Upper) [1H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Setting Column Address for end point
26	Window End Row Address (Lower) [2H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Setting Row Address for end point
	Window End Row Address (Upper) [3H]	0	1	1	0	1	0	1	0	0	1	1	*	EY6	EY5	EY4	Setting Row Address for end point
27	Initial Line-reverse Address (Lower) [4H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Setting Start Line for Line-reverse Display
	Initial Line-reverse Address (Upper) [5H]	0	1	1	0	1	0	1	0	1	0	1	*	LS6	LS5	LS4	Setting Start Line for Line-reverse Display
28	Last Line-reverse Address (Lower) [6H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Setting End Line for Line-reverse Display
	Last Line-reverse Address (Upper) [7H]	0	1	1	0	1	0	1	0	1	1	1	*	LE6	LE5	LE4	Setting End Line for Line-reverse Display
29	Line Reverse ON/OFF [8H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink Set LREV : Line-reverse ON/OFF
30	Upper/Lower Palette Select [9H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	PS : Upper/Lower Palette Register
31	PWM Control [AH]	0	1	1	0	1	0	1	1	0	1	0	PWMS	PWMA	PWMB	PWMC	Setting PWM Mode
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) \* : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

## (14) INSTRUCTION DESCRIPTIONS

This chapter provides detailed descriptions about each instruction. These descriptions are written with the assumption that 80-series MPU is used. When using 68-series MPU, the polarities of the E and R/W signals differ from those of the RDb and WRb signals.

### (14-1) Display Data Write

The “Display Data Write” instruction writes display data on a specified DDRAM address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	1	0	0/1	0/1	0/1

D7	D6	D5	D4	D3	D2	D1	D0
Display Data							

### (14-2) Display Data Read

The “Display Data Read” instruction reads out display data from a specified DDRAM address. One dummy read is necessary right after DDRAM address setting.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	0	1	0/1	0/1	0/1

D7	D6	D5	D4	D3	D2	D1	D0
Display Data							

### (14-3) Window Start Column Address

The “Window Start Column Address” instruction specifies the column address of the start point. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

(Default: AX3-AX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	AX7	AX6	AX5	AX4

(Default: AX7-AX4=0H / Register Address: 1H)

### (14-4) Window Start Row Address

The “Window Start Row Address” instruction specifies the row address of the start point. Available setting range is from (00H) to (7FH), and outside this range is not allowed. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	AY3	AY2	AY1	AY0

(Default: AY3-AY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	AY6	AY5	AY4

(Default: AY6-AY4=0H / Register Address: 3H)

### (14-5) Initial Display Line

This instruction sets the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. For more information, refer to “(14-16) Initial COM”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	LA3	LA2	LA1	LA0

(Default: LA3-LA0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	LA6	LA5	LA4

(Default: LA6-LA4=0H / Register Address: 5H)

**Table 18 Initial Display Line Address**

LA6	LA5	LA4	LA3	LA2	LA1	LA0	Row Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:							:
1	1	1	1	1	1	1	127

**(14-6) N-line Inversion**

The number of N line is selected in between “2” and “128”. When the N-line inversion is enabled by setting “1” at the D<sub>2</sub> (NLIN) bit of the “Display Control (2)” instruction, the FR toggles once every N lines. When the N-line inversion is disabled by setting “0” at this bit, the FR toggles by the frame.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	1	0	N3	N2	N1	N0

(Default: N3-N0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	1	1	*	N6	N5	N4

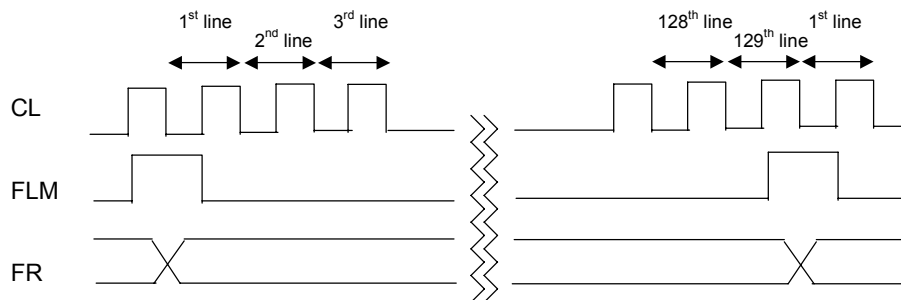
(Default: N6-N4=0H / Register Address: 7H)

**Table 19 N-line Inversion**

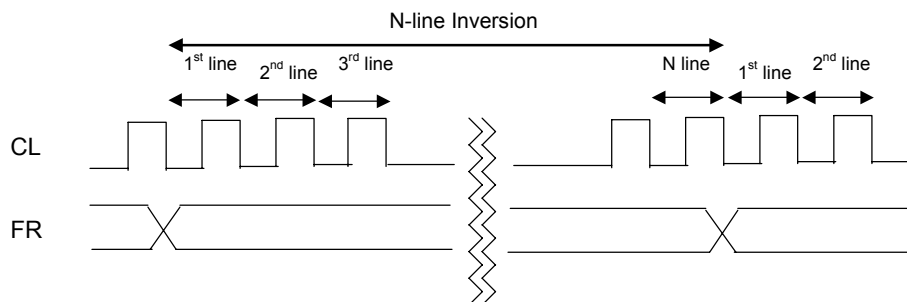
N6	N5	N4	N3	N2	N1	N0	N Line
0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	1	2
:							:
:							:
:							:
1	1	1	1	1	1	1	128

NOTE1) N Line=(N Value)+1

**N-line inversion OFF**



**N-line inversion ON**



**Fig 19 N-line Inversion Timing (1/129 Duty)**

## (14-7) Display Control (1)

The “Display Control (1)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON /OFF

(Default: [SHIFT,MON,ALLON,ON/OFF]=0H / Register Address: 8H)

### D<sub>0</sub> (ON/OFF)

ON/OFF=0 : Display OFF (All COM/SEG fixed at V<sub>SSH</sub> level)

ON/OFF=1 : Display ON

### D<sub>1</sub> (ALLON)

This bit forcibly turns on all pixels regardless of display data. This bit has a priority over the “REV” bit of the “Display Control (2)” instruction.

ALLON=0 : Normal

ALLON=1 : All pixels ON

### D<sub>2</sub> (MON)

MON=0 : Grayscale Mode (Variable 16-grayscale, Variable 8-grayscale or Fixed 8-grayscale Mode)

MON=1 : B&W Mode

### D<sub>3</sub> (SHIFT)

SHIFT=0 : COM<sub>0</sub> → COM<sub>127</sub>

SHIFT=1 : COM<sub>0</sub> ← COM<sub>127</sub>

## (14-8) Display Control (2)

The “Display Control (2)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	0	1	REV	NLIN	SWAP	*

(Default: [REV,NLIN,SWAP]=0H / Register Address: 9H)

### D<sub>1</sub> (SWAP)

This bit swaps palettes A<sub>j</sub> and palettes C<sub>j</sub> (j=0-15). This function reduces the restrictions on the IC position of an LCD module. For more information, refer to “(16) SWAP FUNCTION”.

SWAP=0 : SWAP OFF  
 SWAP=1 : SWAP ON

### D<sub>2</sub> (NLIN)

This bit enables the N-line inversion.

NLIN=0 : N-line Inversion OFF (FR toggles by the frame.)  
 NLIN=1 : N-line Inversion ON (FR toggles once every N lines.)

### D<sub>3</sub> (REV)

This bit enables the reverse display function that reverses the polarities of all display data without changing the DDRAM.

REV=0 : Reverse Display OFF (Normal)  
 REV=1 : Reverse Display ON

**Table 20 Reverse Display ON/OFF**

REV	Display	DDRAM Data → Display Data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

## (14-9) Increment/Decrement Control

The “HV”, “XD” and “YD” bits set either auto-increment or auto-decrement mode to the column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up or down, whenever the DDRAM is accessed. This instruction is used for the window area setting as well as the “Window Start Column/Row Address” and “Window End Column/Row Address” instructions. The display-rotation function or the mirror-inversion function is also enabled by this setting. For more information, refer to “(4-3) DDRAM Access Direction”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	AIM	HV	XD	YD

(Default: [AIM,HV,XD,YD]=0H / Register Address: AH)

### D<sub>0</sub> (YD), D<sub>1</sub> (XD), D<sub>2</sub> (HV)

**Table 21 Horizontal/Vertical & Increment/Decrement**

HV	XD	YD	X	Y	Direction
0	0	0	Increment	Increment	Horizontal
0	0	1	Increment	Decrement	
0	1	0	Decrement	Increment	
0	1	1	Decrement	Decrement	
1	0	0	Increment	Increment	Vertical
1	0	1	Increment	Decrement	
1	1	0	Decrement	Increment	
1	1	1	Decrement	Decrement	

### D<sub>3</sub> (AIM)

**Table 22 Read-modify-write ON/OFF**

AIM	Increment Mode	NOTE
0	Read-modify-write OFF	1
1	Read-modify-write ON	2

NOTE1) Increment or decrement in writing and reading display data

NOTE2) Increment or decrement in writing display data only



## (14-10) Power Control

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	AMPON	HALT	DCON	ACL

(Default: [AMPON,HALT,DCON,ACL]=0H / Register Address: BH)

### D<sub>0</sub> (ACL)

This bit initializes the internal LCD power supply.

ACL=0 : Initialization OFF (Normal)  
 ACL=1 : Initialization ON

NOTE) During the initialization, "1" is read out as the status of the "ACL" bit by the "Register Read" instruction. After the initialization, it is "0". As the CLK triggers the initialization, the "wait time" at least equivalent to 2 cycles of the CLK is required for the next instruction.

### D<sub>1</sub> (DCON)

The "DCON" bit activates the voltage booster.

DCON=0 : Voltage Booster OFF  
 DCON=1 : Voltage Booster ON

### D<sub>2</sub> (HALT)

The "HALT" bit enables the power save mode. During the power save, operating current is down to the stand-by level. The internal state of the LSI in the power save mode is listed below.

HALT=0 : Power Save OFF (Normal)  
 HALT=1 : Power Save ON

#### Internal State in Power Save Mode (HALT="1")

- Internal oscillator and internal LCD power supply are halted.
- All segment and common drivers are fixed at V<sub>SSH</sub> level.
- External clock to the OSC1 cannot be accepted.
- Display data in the DDRAM is being maintained.
- Data in the instruction registers are being maintained.
- V<sub>LCD</sub>, V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub> and V<sub>4</sub> are in high impedance.

NOTE) In the power save ON sequence, execute the "Display OFF" prior to the "Power Save ON". In the power save OFF sequence, execute the "Power save OFF" prior to the "Display ON". If the "Power Save ON/OFF" instruction is executed during the "Display ON", unexpected pixels may be turned on instantly.

### D<sub>3</sub> (AMPON)

The "AMPON" bit activates the voltage converter which includes the reference voltage generator, the voltage regulator and the LCD bias generator.

AMPON=0 : Voltage Converter OFF  
 AMPON=1 : Voltage Converter ON

## (14-11) Duty Cycle Ratio

The “Duty Cycle Ratio” instruction selects LCD duty cycle ratio, and is used to carry out the partial display in combination with other instructions such as the “Boost Level”, the “LCD Bias Ratio” and the “EVR Control”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	0	0	DS3	DS2	DS1	DS0

(Default: DS3-DS0=0H / Register Address: CH)

**Table 23 Duty Cycle Ratio**

DS3	DS2	DS1	DS0	Duty Cycle Ratio		# of Commons
				DSE=0	DES=1	
0	0	0	0	1/129	1/128	128 commons
0	0	0	1	1/121	1/120	120 commons
0	0	1	0	1/113	1/112	112 commons
0	0	1	1	1/105	1/104	104 commons
0	1	0	0	1/97	1/96	96 commons
0	1	0	1	1/89	1/88	88 commons
0	1	1	0	1/81	1/80	80 commons
0	1	1	1	1/73	1/72	72 commons
1	0	0	0	1/65	1/64	64 commons
1	0	0	1	1/57	1/56	56 commons
1	0	1	0	1/49	1/48	48 commons
1	0	1	1	1/41	1/40	40 commons
1	1	0	0	1/33	1/32	32 commons
1	1	0	1	1/25	1/24	24 commons
1	1	1	0	1/17	1/16	16 commons
1	1	1	1	Inhibited		

NOTE) Duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting “1” at the D<sub>1</sub> (DSE) bit of the “Duty-1 ON/OFF” instruction. Refer to “(14-17) Duty-1 /Display Clock ON/OFF”.

## (14-12) Boost Level

The “Boost level” selects the multiple of the voltage booster.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	0	1	*	VU2	VU1	VU0

(Default: VU2-VU0=0H / Register Address: DH)

**Table 24 Boost Level**

VU2	VU1	VU0	Boost Level
0	0	0	1 time (No boost)
0	0	1	2 times
0	1	0	3 times
0	1	1	4 times
1	0	0	5 times
1	0	1	6 times
1	1	0	Inhibited
1	1	1	Inhibited

## (14-13) LCD Bias Ratio

The "LCD bias ratio" selects LCD bias ratio.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	1	0	*	B2	B1	B0

(Default: B2-B0=0H / Register Address: EH)

**Table 25 LCD Bias Ratio**

B2	B1	B0	LCD Bias Ratio
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

## (14-14) Instruction Table Select

This instruction specifies an instruction table, and should be executed prior to other instructions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	1	1	TST0	RE2	RE1	RE0

(Default: TST0, RE2-RE0=0H / Register Address: FH)

**Table 26 Instruction Table Select**

RE2	RE1	RE0	Instructions
0	0	0	Instruction Table (0)
0	0	1	Instruction Table (1)
0	1	0	Instruction Table (2)
0	1	1	Instruction Table (3)
1	0	0	Instruction Table (4)
1	0	1	Instruction Table (5)

NOTE) "TST0" bit must be "0". This is used for maker tests only.

## (14-15) Palette A / B / C

### Palette A0 (PS=0) / Palette A8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

(Register Address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	*	*	PA04/ PA84

(Register Address: 1H)

### Palette A1 (PS=0) / Palette A9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	*	*	PA14/ PA94

(Register Address: 3H)

### Palette A2 (PS=0) / Palette A10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	*	PA24/ PA104

(Register Address: 5H)

### Palette A3 (PS=0) / Palette A11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	*	PA34/ PA114

(Register Address: 7H)

### Palette A4 (PS=0) / Palette A12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	*	*	PA44/ PA124

(Register Address: 9H)

NOTE) Refer to the tables in "(6) GRAYSCALE PALETTE" for default setting.

**Palette A5 (PS=0) / Palette A13 (PS=1)**

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	1	1	*	*	*	PA54/ PA134

(Register Address: BH)

**Palette A6 (PS=0) / Palette A14 (PS=1)**

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	0	1	*	*	*	PA64/ PA144

(Register Address: DH)

**Palette A7 (PS=0) / Palette A15 (PS=1)**

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	1	*	*	*	PA74/ PA154

(Register Address: 1H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

## Palette B0 (PS=0) / Palette B8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	*	*	PB04/ PB84

(Register Address: 3H)

## Palette B1 (PS=0) / Palette B9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	*	PB14/ PB94

(Register Address: 5H)

## Palette B2 (PS=0) / Palette B10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	*	PB24/ PB104

(Register Address: 7H)

## Palette B3 (PS=0) / Palette B11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	*	*	PB34/ PB114

(Register Address: 9H)

## Palette B4 (PS=0) / Palette B12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	*	*	*	PB44/ PB124

(Register Address: BH)

NOTE) Refer to the tables in "(6) GRAYSCALE PALETTE" for default setting.

**Palette B5 (PS=0) / Palette B13 (PS=1)**

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	0	1	*	*	*	PB54/ PB134

(Register Address: DH)

**Palette B6 (PS=0) / Palette B14 (PS=1)**

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	1	*	*	*	PB64/ PB144

(Register Address: 1H)

**Palette B7 (PS=0) / Palette B15 (PS=1)**

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	1	*	*	*	PB74/ PB154

(Register Address: 3H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

## Palette C0 (PS=0) / Palette C8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	0	1	*	*	*	PC04/ PC84

(Register Address: 5H)

## Palette C1 (PS=0) / Palette C9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	1	1	*	*	*	PC14/ PC94

(Register Address: 7H)

## Palette C2 (PS=0) / Palette C10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	0	1	*	*	*	PC24/ PC104

(Register Address: 9H)

## Palette C3 (PS=0) / Palette C11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	1	1	*	*	*	PC34/ PC114

(Register Address: BH)

## Palette C4 (PS=0) / Palette C12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	0	1	*	*	*	PC44/ PC124

(Register Address: DH)

NOTE) Refer to the tables in "(6) GRAYSCALE PALETTE" for default setting.



**Palette C5 (PS=0) / Palette C13 (PS=1)**

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	1	*	*	*	PC54/ PC134

(Register Address: 1H)

**Palette C6 (PS=0) / Palette C14 (PS=1)**

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	0	PC63/ PC143	PC62/ PC142	PC61/ PB141	PC60/ PB140

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	1	*	*	*	PC64/ PC144

(Register Address: 3H)

**Palette C7 (PS=0) / Palette C15 (PS=1)**

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	0	1	*	*	*	PC74/ PC154

(Register Address: 5H)

NOTE) Refer to the tables in "(6) GRAYSCALE PALETTE" for default setting.

## (14-16) Initial COM

The “Initial COM” instruction specifies the common driver for a scan start common.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	1	0	SC3	SC2	SC1	SC0

(Default: SC3-SC0=0H / Register Address: 6H)

**Table 27 Initial COM**

SC3	SC2	SC1	SC0	Initial COM (SHIFT=0)	Initial COM (SHIFT=1)
0	0	0	0	COM <sub>0</sub>	COM <sub>127</sub>
0	0	0	1	COM <sub>4</sub>	COM <sub>123</sub>
0	0	1	0	COM <sub>8</sub>	COM <sub>119</sub>
0	0	1	1	COM <sub>16</sub>	COM <sub>111</sub>
0	1	0	0	COM <sub>24</sub>	COM <sub>103</sub>
0	1	0	1	COM <sub>32</sub>	COM <sub>95</sub>
0	1	1	0	COM <sub>40</sub>	COM <sub>87</sub>
0	1	1	1	COM <sub>48</sub>	COM <sub>79</sub>
1	0	0	0	COM <sub>56</sub>	COM <sub>71</sub>
1	0	0	1	COM <sub>64</sub>	COM <sub>63</sub>
1	0	1	0	COM <sub>72</sub>	COM <sub>55</sub>
1	0	1	1	COM <sub>80</sub>	COM <sub>47</sub>
1	1	0	0	COM <sub>88</sub>	COM <sub>39</sub>
1	1	0	1	COM <sub>96</sub>	COM <sub>31</sub>
1	1	1	0	COM <sub>104</sub>	COM <sub>23</sub>
1	1	1	1	COM <sub>112</sub>	COM <sub>15</sub>

## (14-17) Duty-1 /Display Clock ON/OFF

This instruction controls ON (Duty-1) /OFF (Duty-0) and Display Clock ON/OFF.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	1	1	*	*	DSE	SON

(Default: SON,DSE=0H / Register Address: 7H)

### D<sub>0</sub> (SON)

SON=0 : CL, FLM, FR, and CLK are fixed at “L” level.  
 SON=1 : CL, FLM, FR, and CLK are enabled.

### D<sub>1</sub> (DSE)

The duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting “1” at the “DSE” bit.

DSE=0 : OFF (Duty-0)  
 DSE=1 : ON (Duty-1)

NOTE) For the last common timing at “DSE=0”, all common drivers generate non-selective waveforms, and segment drivers generate the same waveforms as for the previous common timing. For instance, in 1/129 duty cycle, the segment waveforms for 129<sup>th</sup> common timing are the same as for 128<sup>th</sup> common timing (last line).

## (14-18) Display Mode Control

The “Display Mode Control” instruction sets up display modes such as the variable or fixed grayscale mode and the variable 8- or 16-grayscale mode. The D<sub>2</sub> (MON) bit of the “Display Control (1)” is used in combination. Refer to “(5) GRAY SCALE CONTROL CIRCUIT” and “(14-7) Display Control (1).”

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	0	0	PWM	C256	*	*

(Default: PWM,C256=0H / Register Address: 8H)

### D<sub>3</sub> (PWM)

PWM=0 : Variable grayscale Mode (Variable 8-/16-grayscale Mode)  
 PWM=1 : Fixed 8-grayscale Mode

### D<sub>2</sub> (C256)

C256=0 : Variable 16-grayscale Mode at “PWM=0” (4096 colors)  
 C256=1 : Variable 8-grayscale Mode at “PWM=0” (256 colors)

### (14-19) Bus Length

This instruction selects 8- or 16-bit bus length, and sets oscillator configuration as well.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	0	1	*	ABS	CKS	WLS

(Default: ABS,CKS,WLS=0H / Register Address: 9H)

### D<sub>0</sub> (WLS)

WLS=0: 8-bit Bus Length  
 WLS=1: 16-bit Bus Length

### D<sub>1</sub> (CKS)

CKS =0: Internal Oscillator using an internal resistor  
 CKS =1: External Clock, or Internal Oscillator using an external resistor

NOTE) Refer to “(10) OSCILLATOR”.

### D<sub>2</sub> (ABS)

ABS=0: ABS Mode OFF (Normal)  
 ABS=1: ABS Mode ON

### (14-20) EVR Control

The “EVR Control” instruction adjusts V<sub>LCD</sub> to optimize display contrast. This instruction is finally effective when both upper and lower bytes are transmitted in order to prevent high V<sub>LCD</sub>. The setting order is upper byte first, then lower byte. Refer to “(11-2-3) Electrical Variable Resistor (EVR)”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	1	0	DV <sub>3</sub>	DV <sub>2</sub>	DV <sub>1</sub>	DV <sub>0</sub>

(Default: DV<sub>3</sub>-DV<sub>0</sub>=0H / Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	0	1	1	*	DV <sub>6</sub>	DV <sub>5</sub>	DV <sub>4</sub>

(Default: DV<sub>6</sub>-DV<sub>4</sub>=0H / Register Address: BH)

**Table 28 EVR Control**

DV <sub>6</sub>	DV <sub>5</sub>	DV <sub>4</sub>	DV <sub>3</sub>	DV <sub>2</sub>	DV <sub>1</sub>	DV <sub>0</sub>	V <sub>LCD</sub>
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	1	High

### Formula of V<sub>LCD</sub>

$$V_{LCD} [V] = 0.5x V_{REG} + M (V_{REG} - 0.5x V_{REG}) / 127$$

$$V_{BA} = V_{EE} \times 0.9$$

$$V_{REG} = V_{REF} \times N$$

V<sub>BA</sub> : Output of the reference voltage generator

V<sub>REF</sub> : Input of the voltage regulator

V<sub>REG</sub> : Output of the voltage regulator

N : Boost level

M : EVR Value

## (14-21) Frequency Control

The "Frequency Control" instruction adjusts the frame frequency.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	Rf2	Rf1	Rf0

(Default: DV<sub>3</sub>-DV<sub>0</sub>=0H / Register Address: DH)

**Table 29 Frequency Control**

Rf 2	Rf 1	Rf 0	Feedback Resistor Value
0	0	0	Reference Value
0	0	1	0.8 x Reference Value
0	1	0	0.9 x Reference Value
0	1	1	1.1 x Reference Value
1	0	0	1.2 x Reference Value
1	0	1	0.7 x Reference Value
1	1	0	1.3 x Reference Value
1	1	1	Inhibited

## (14-22) Discharge ON/OFF

Discharge circuit is used to discharge out of the stabilizing capacitors placed on the V<sub>LCD</sub>, V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub>, V<sub>4</sub> and V<sub>OUT</sub>. Refer to "(11-4) Discharge Circuit".

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	*	*	DIS2	DIS

(Default: DIS2,DIS1=0H / Register Address: EH)

### D<sub>0</sub> (DIS)

DIS=0 : Discharge OFF  
 DIS=1 : Discharge ON (Discharge from V<sub>LCD</sub>, V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub> and V<sub>4</sub>)

### D<sub>1</sub> (DIS2)

DIS2=0 : Discharge OFF  
 DIS2=1 : Discharge ON (Discharge from V<sub>OUT</sub> through the internal resistor between V<sub>OUT</sub> and V<sub>EE</sub>)

NOTE) Resistance is 100KΩ typical.

## (14-23) Register Address

The “Register Address” instruction specifies a register address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	0	0	RA3	RA2	RA1	RA0

(Default: RA3-RA0=BH / Register Address: CH)

## (14-24) Register Read

The “Register Read” instruction reads out instruction data from the register which address is specified by the “Register Address” instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
*	*	*	*	Internal register data read			

## (14-25) Window End Column Address

The “Window End Column Address” instruction specifies the column address of the end point. Refer to “(4-2) Window Area for DDRAM Access”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	0	EX3	EX2	EX1	EX0

(Default: EX3-EX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	1	EX7	EX6	EX5	EX4

(Default: EX7-EX4=0H / Register Address: 1H)

## (14-26) Window End Row Address

The “Window End Row Address” instruction specifies the row address of the end point. Refer to “(4-2) Window Area for DDRAM Access”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	0	EY3	EY2	EY1	EY0

(Default: EY3-EY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	1	*	EY6	EY5	EY4

(Default: EY6-EY4=0H / Register Address: 3H)

## (14-27) Initial Line-reverse Address

The “Initial Line-reverse Address” instruction specifies the start line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	0	0	LS3	LS2	LS1	LS0

(Default: LS3-LS0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	0	1	*	LS6	LS5	LS4

(Default: LS6-LS4=0H / Register Address: 5H)

## (14-28) Last Line-reverse Address

The “Last Line-reverse Address” instruction specifies the end line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	LE3	LE2	LE1	LE0

(Default: LE3-LE0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	LE6	LE5	LE4

(Default: LE6-LE4=0H / Register Address: 7H)

## (14-29) Line Reverse ON/OFF

The “Line Reverse ON/OFF” instruction enables the line-reverse display, and blink function as well. Note that the line reverse display cannot be used for entire display area. In this case, use the reverse display function by the D<sub>3</sub> (REV) bit of the “Display Control (2)” instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	*	*	BT	LREV

(Default: BT,LREV=0H / Register Address: 8H)

### D<sub>0</sub> (LREV)

- LREV =0 : Line Reverse OFF (Normal)
- LREV =1 : Line Reverse ON

### D<sub>1</sub> (BT)

- BT =0 : No Blink
- BT =1 : Blink once every 32 frames

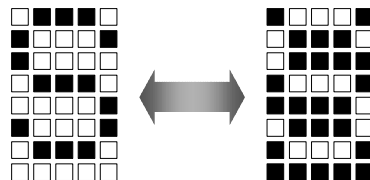


Fig 20 On-screen Image in Using Line-reverse Display and Blink Function

### (14-30) Upper/Lower Palette Select

The "Upper/Lower Palette Select" instruction selects either upper or lower palette register.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	*	*	PS

(Default: PS=0 / Register Address: 9H)

#### D<sub>0</sub> (PS)

- PS=0 : Lower Palettes (PA00, PA01, PA02, PA03, ..., PC74)
- PS=1 : Upper Palettes (PA80, PA81, PA82, PA83, ..., PC154)

### (14-31) PWM Control

The "PWM control" instruction selects PWM type, as shown in Fig 21.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PWMS	PWMA	PWMB	PWMC

(Default: PWMS,PWMA,PWMB,PWMC=0H / Register Address: AH)

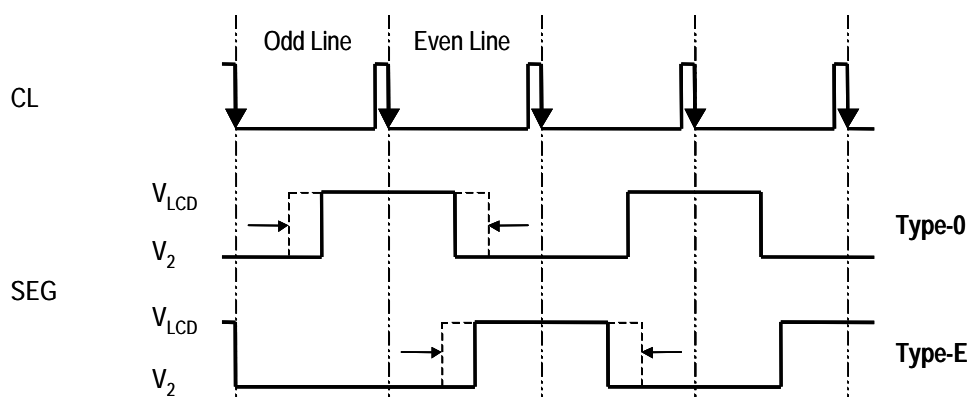
#### D<sub>3</sub> (PWMS)

- PWMS=0 : Type 1
- PWMS=1 : Type 2

#### D<sub>2</sub> (PWMA), D<sub>1</sub> (PWMB), D<sub>0</sub> (PWMC)

- PWMZ=0 (Z=A, B and C): Type 1-O
- PWMZ=1 (Z=A, B and C): Type 1-E

#### PWM Type 1 (PWMS=0)



#### PWM Type 2 (PWMS=1)

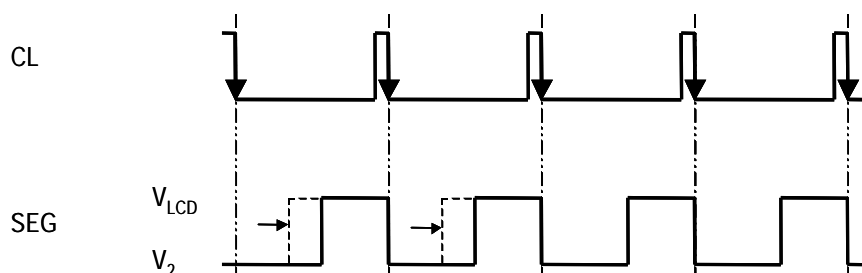


Fig 21 PWM Control

## (15) PARTIAL DISPLAY FUNCTION

The partial display function activates specified area on an LCD screen, or equivalently, common drivers are simply scanning this specified area. This function allows LCD modules to work in a minimum duty cycle ratio to minimize power consumption. The partial display function is carried out by the combination of the “Duty Cycle Ratio”, “LCD Bias Ratio”, “Boost Level” and “EVR Control” instructions. For more information, refer to “(14-11) Duty Cycle Ratio”, “(14-12) Boost Level”, “(14-13) LCD Bias Ratio” and “(14-20) EVR Control”. Typical setting sequence is shown in “(18-4) Partial Display Sequence”.

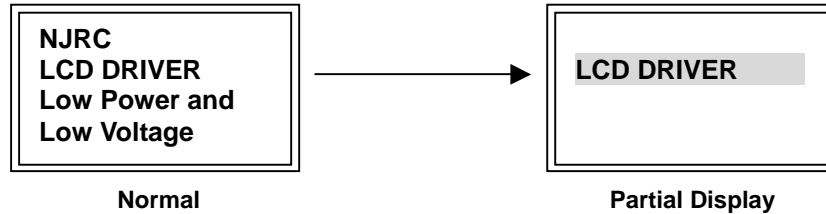


Fig 22 On-screen Image in Using Partial Display Function

## (16) SWAP FUNCTION

The swap function switches the palettes  $A_j$  and the palettes  $C_j$  ( $j=0-15$ ), and is controlled by the  $D_1$  (SWAP) bit of the “Display Control (2)” instruction. This function reduces the restrictions on the IC position of an LCD module. Fig 23 “Overview of Swap Function” illustrates general outlines of internal operations, and (16-1-1) through (16-1-4) show each configuration on a mode-by-mode basis.

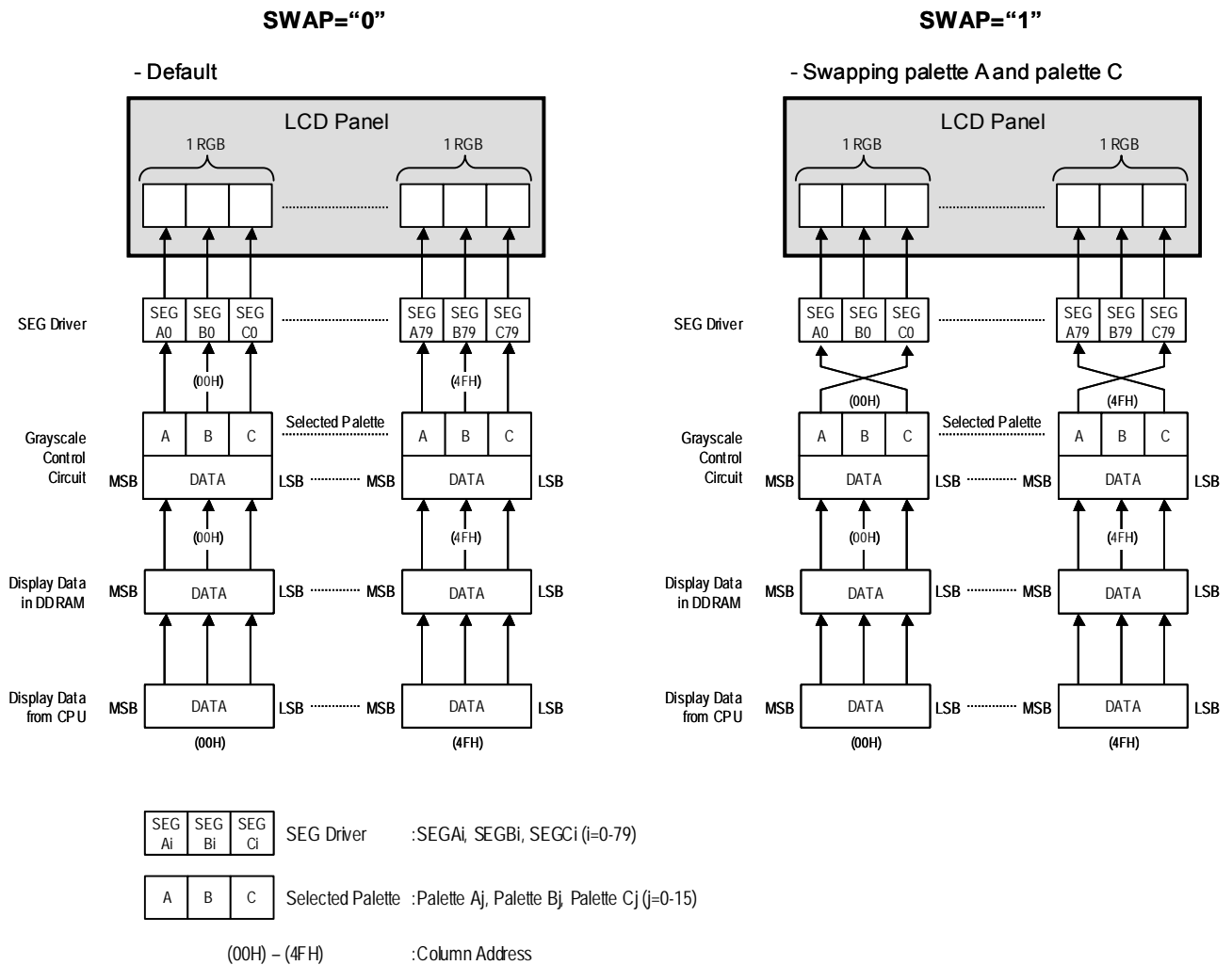


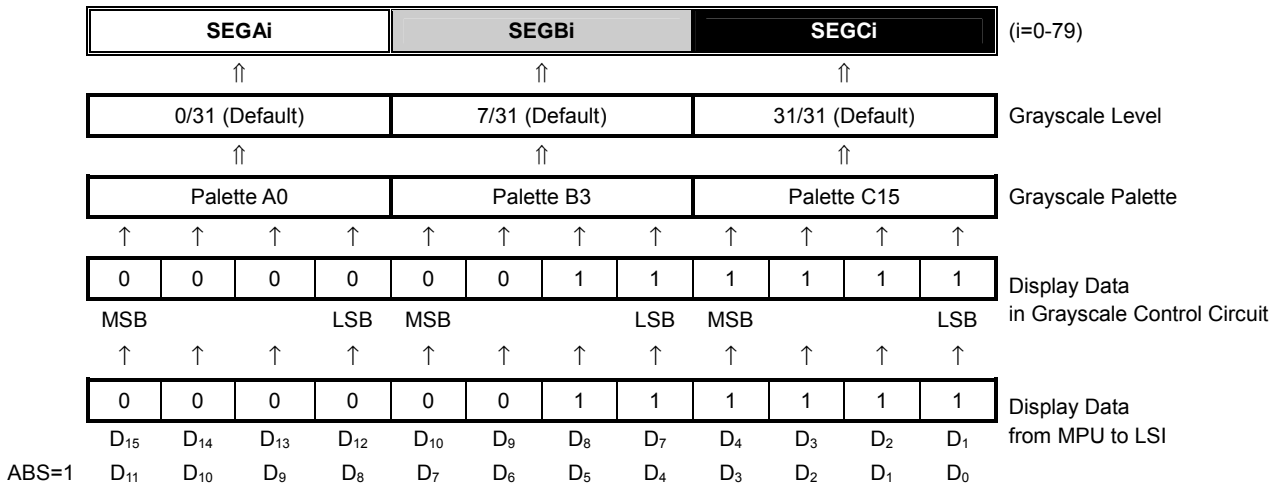
Fig 23 Overview of SWAP Function



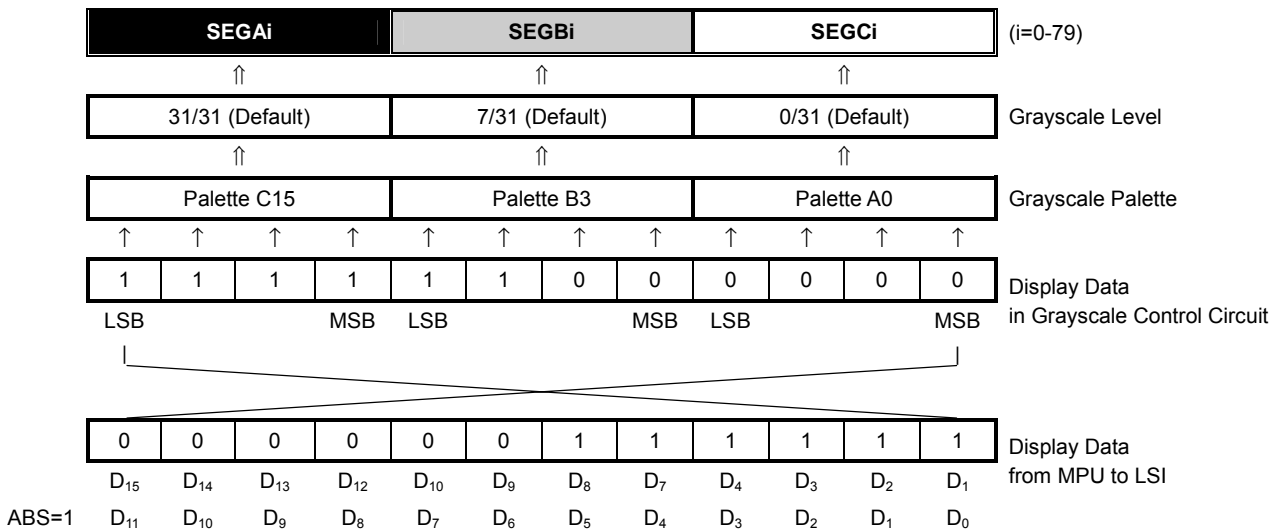
## (16-1) Swap Function in Variable 16-grayscale Mode

### 16-bit Bus Length

**SWAP=0**



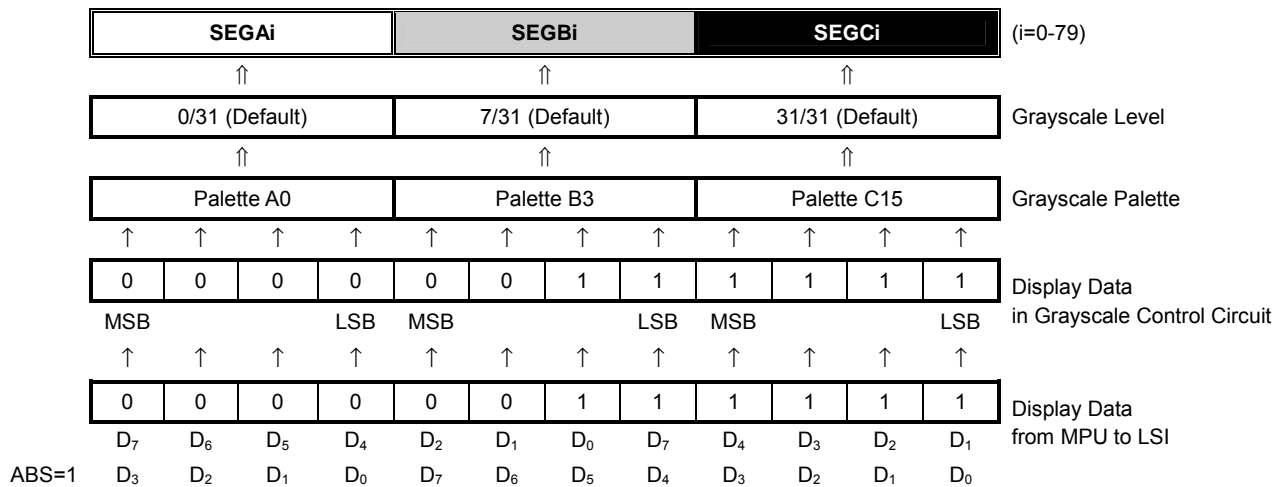
**SWAP=1**



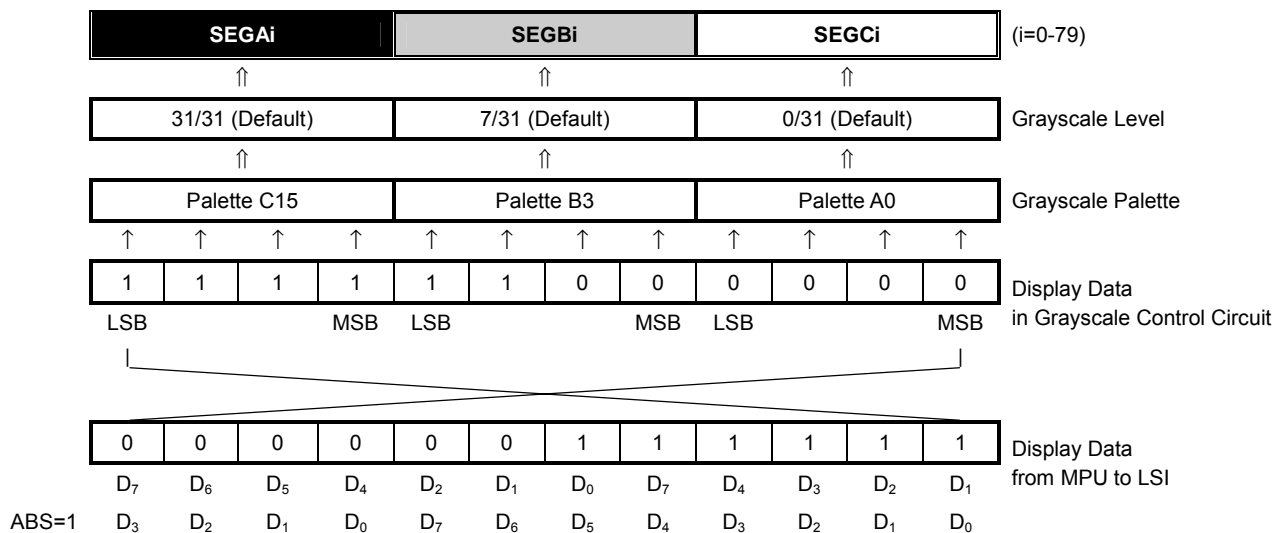
NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".

## 8-bit Bus Length

SWAP=0



SWAP=1

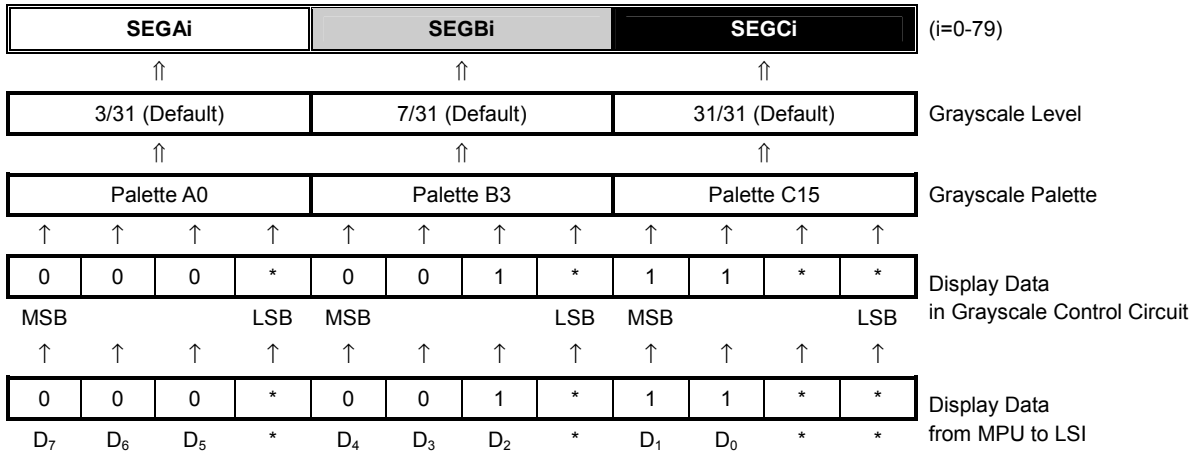


NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".

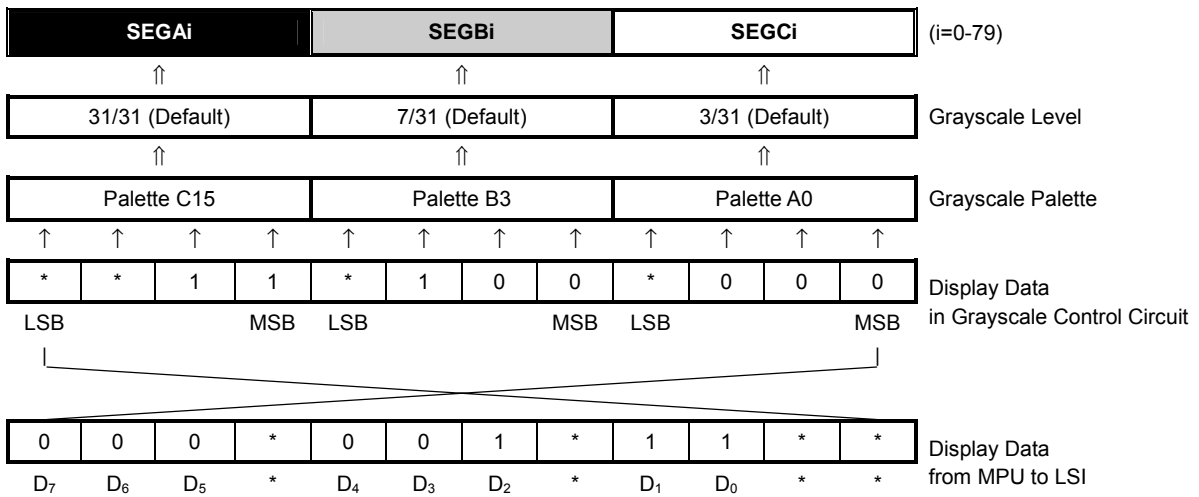
## (16-2) Swap Function in Variable 8-Grayscale Mode

### 8-bit Bus Length

**SWAP=0**



**SWAP=1**

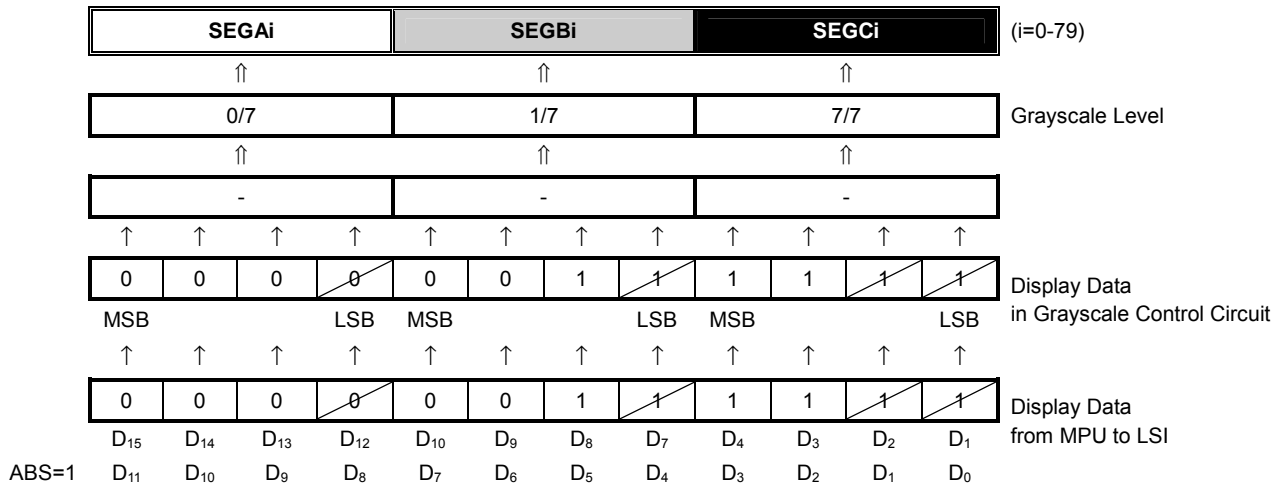


NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".

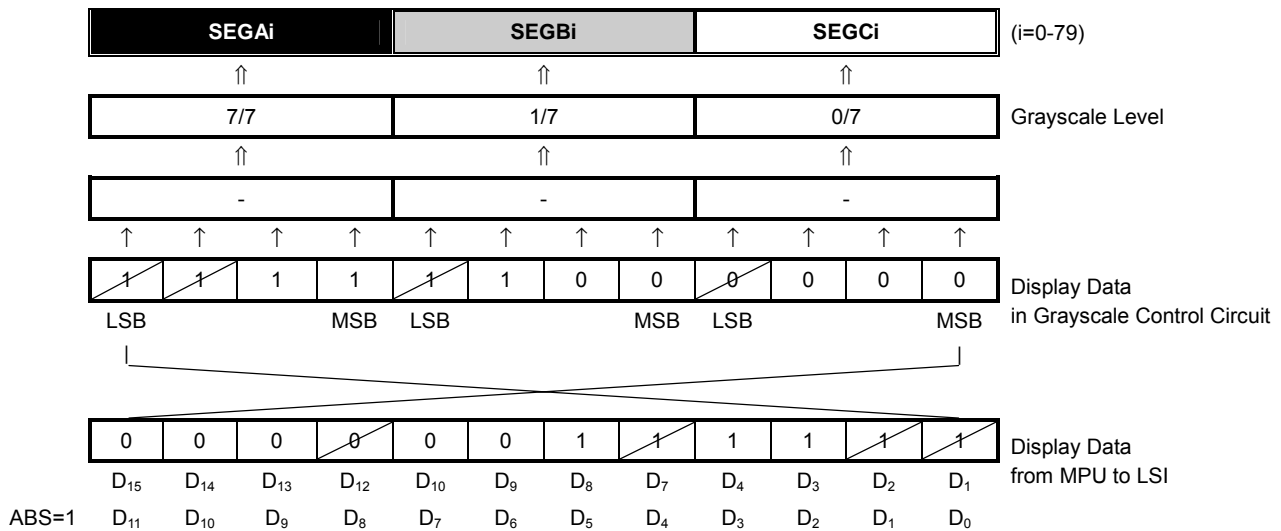
## (16-3) Swap Function in Fixed 8-grayscale Mode

### 16-bit Bus Length

SWAP=0



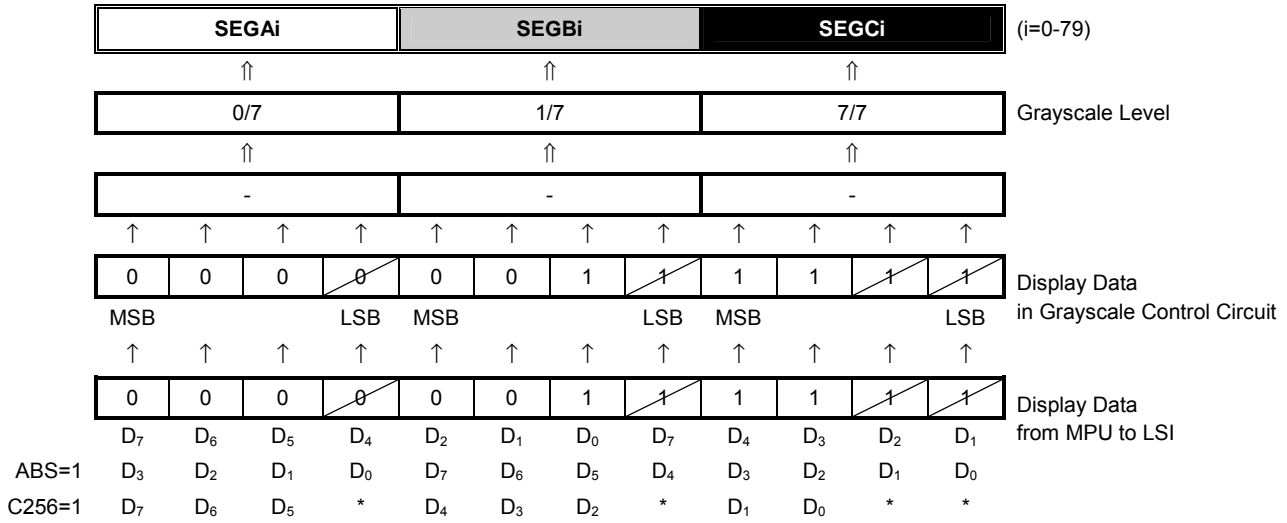
SWAP=1



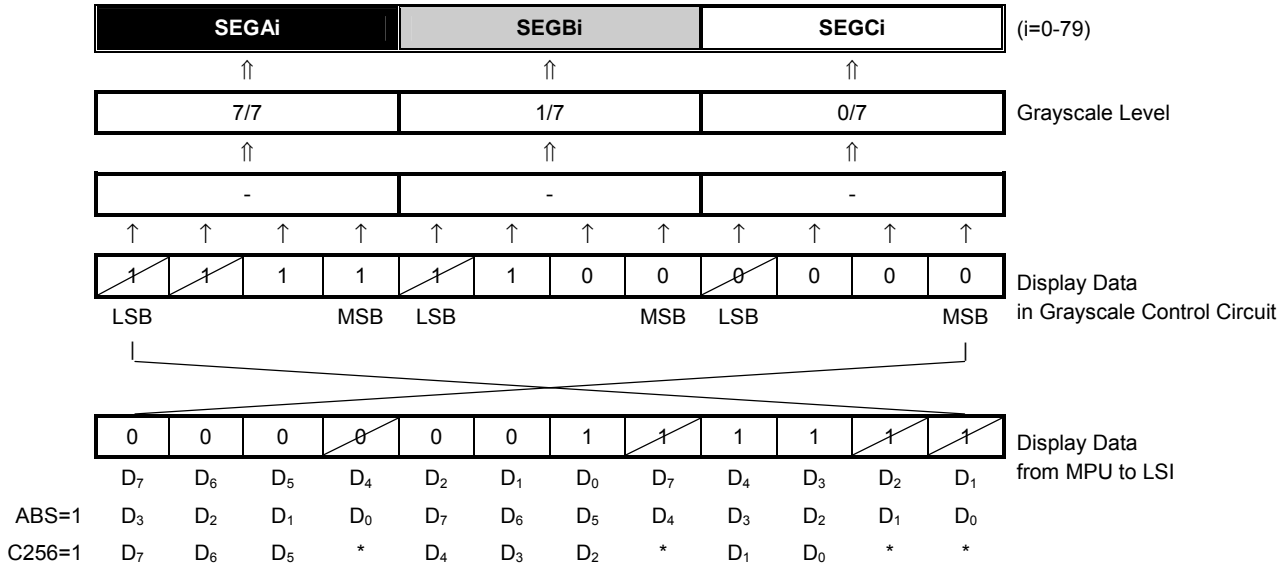
NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".  
 NOTE2) The data indicated with a slash mark (/) is invalid.

## 8-bit Bus Length

**SWAP=0**



**SWAP=1**



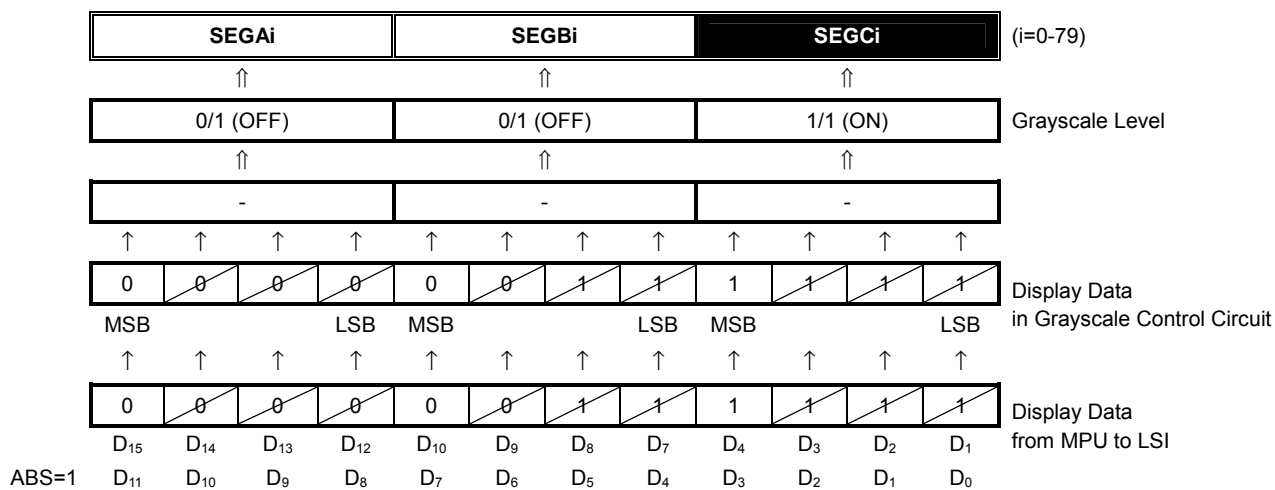
NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".

NOTE2) The data indicated with a slash mark (/) is invalid.

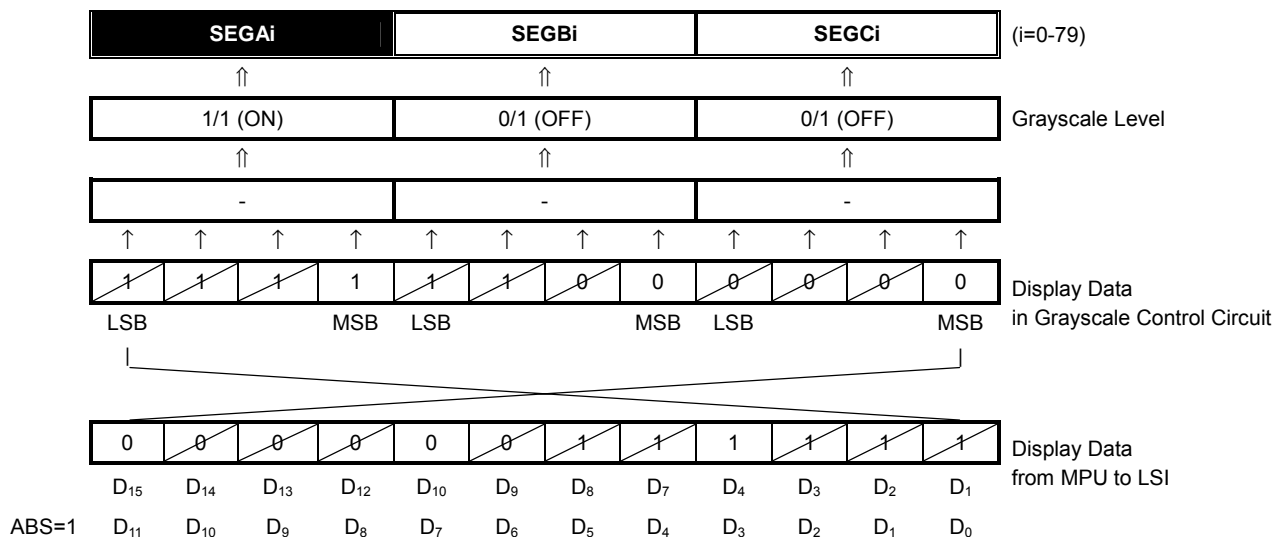
## (16-4) Swap Function in B&W Mode

### 16-bit Bus Length

SWAP=0



SWAP=1

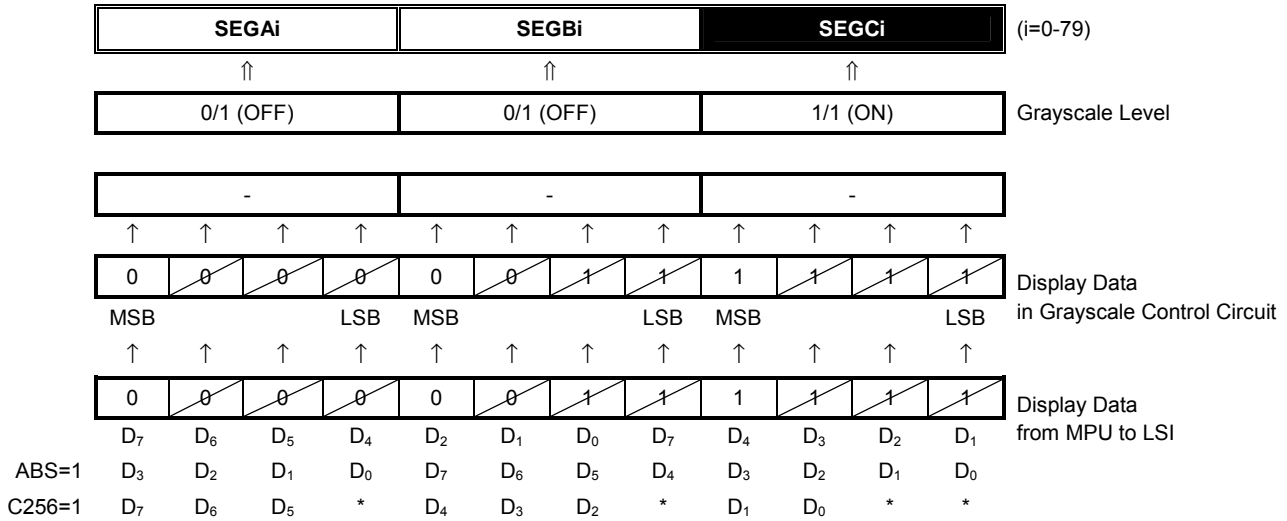


NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".

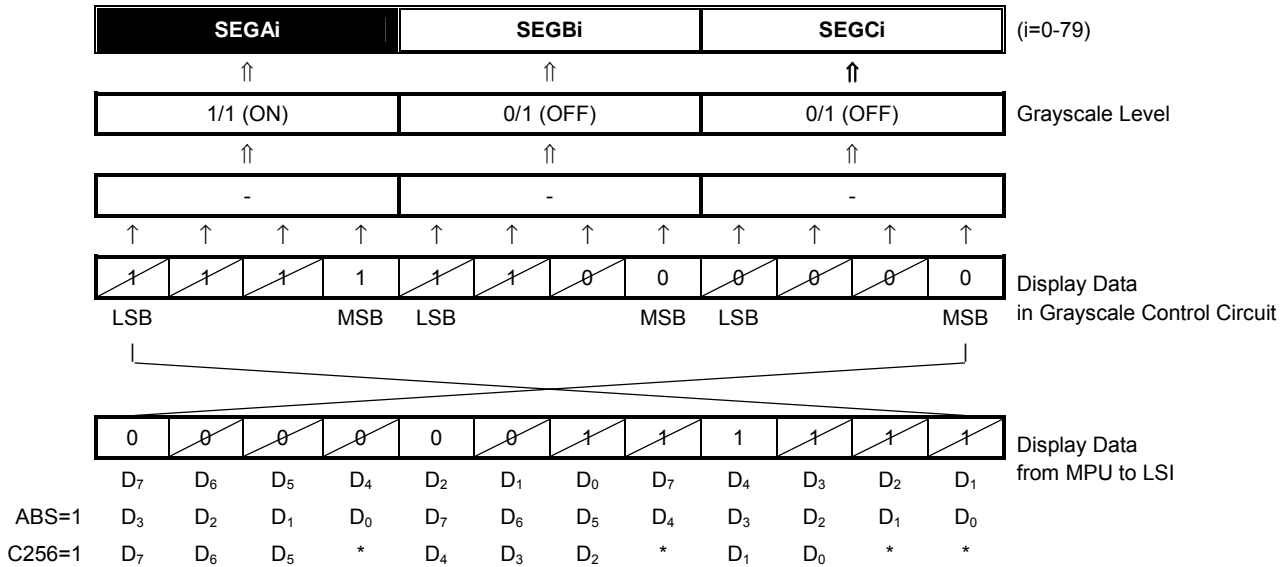
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

SWAP=0



SWAP=1



NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as “0”.  
 NOTE2) The data indicated with a slash mark (/) is invalid.

(17) RELATION BETWEEN ROW ADDRESS AND COMMON DRIVER

The relation between row address and common driver is changed by the D<sub>3</sub> (SHIFT) bit of the “Display Control (1)” and the “Duty Cycle Ratio”, “Initial Display Line” and “Initial COM” instructions.

When the “Initial Display Line” is set to (LA6:LA0=00H: Address “0”), the row address corresponding to an initial COM is “0”. However, if the “Initial Display Line” is other than “0”, the row address is shifted from “0” by just that address. For instance, when the initial display line address is (LA6:LA0=05H: Address “5”) and the initial COM is (SC3:SC0=1H), the row address on the initial COM is “5” and the initial COM is “COM<sub>4</sub>”.

(17-1) through (17-5) illustrate the examples of the relation between row address and common driver.





(17-2) SHIFT=0, Initial Display Line "0", Duty Cycle Ratio "1/17"

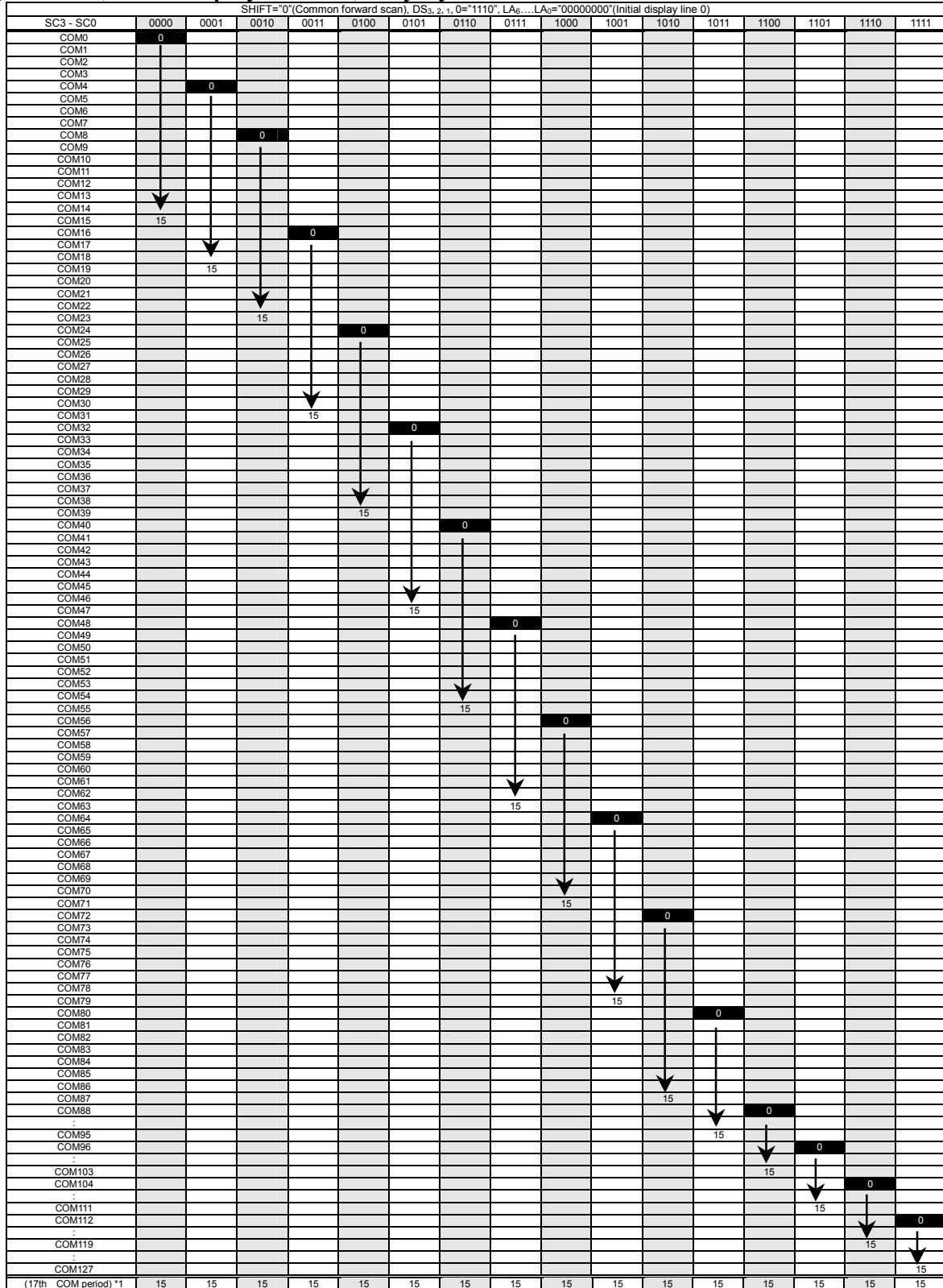


Fig 25 Relation between Row address and Common Driver (2)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

NOTE2) Segment waveforms for 17<sup>th</sup> COM timing are the same as for 16<sup>th</sup> COM timing (Row address "15").

(17-3) SHIFT=1, Initial Display Line "0", Duty Cycle Ratio "1/129"

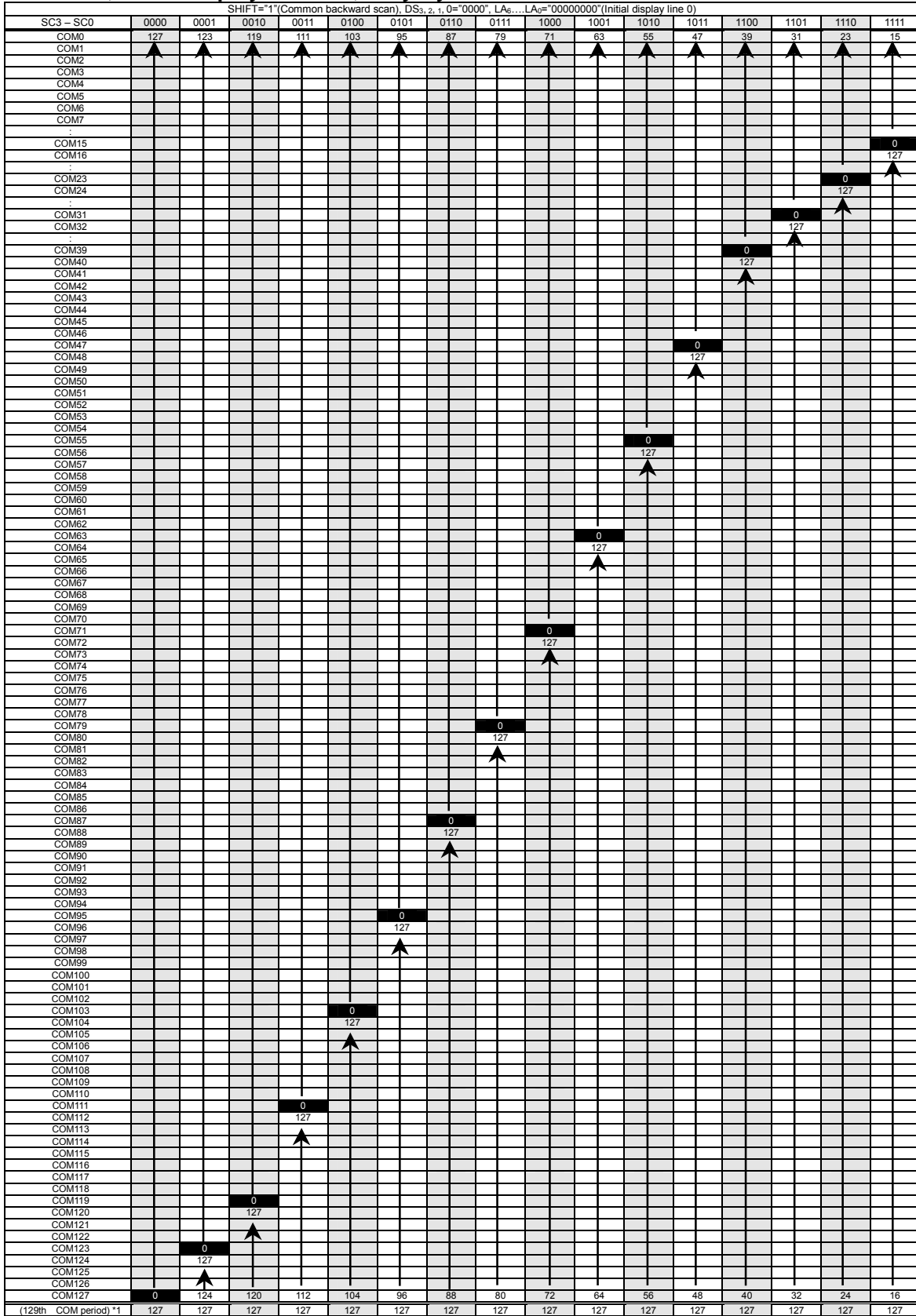
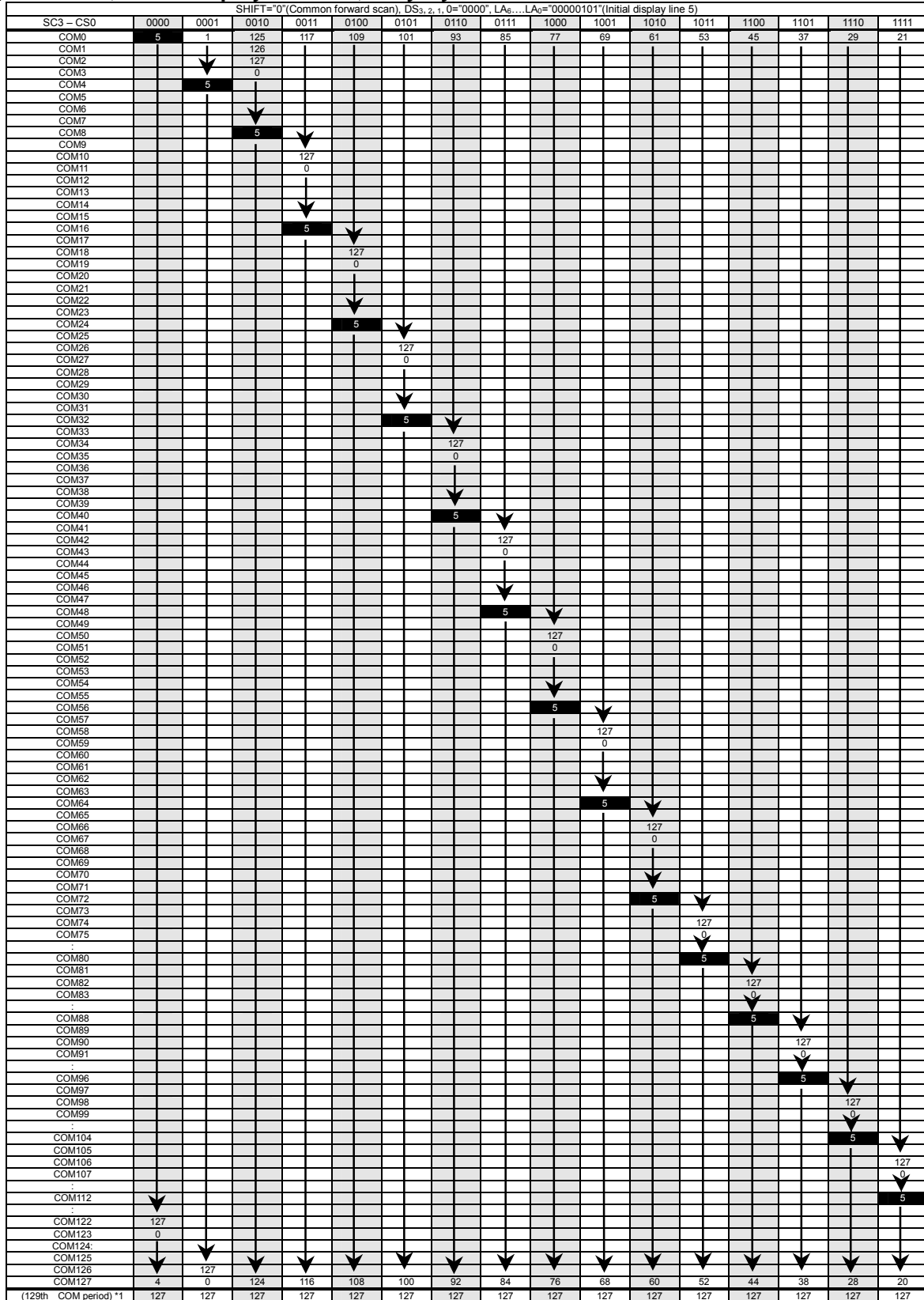


Fig 26 Relation between Row address and Common Driver (3)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

NOTE2) Segment waveforms for 129<sup>th</sup> COM timing are the same as for 128<sup>th</sup> COM timing (Row address "127").

**(17-4) SHIFT=0, Initial Display Line "5", Duty Cycle Ratio "1/129"**



**Fig 27 Relation between Row address and Common Driver (4)**

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address  
 NOTE2) Segment waveforms for 129<sup>th</sup> COM timing are the same as for 128<sup>th</sup> COM timing (Row address "127").

## (17-5) SHIFT=0, Initial Display Line "0", Duty Cycle Ratio "1/128" (Dity-1 ON)

SHIFT="0"(Common forward scan), DS<sub>3,2,1,0</sub>=0000, LA<sub>6,...</sub>LA<sub>0</sub>=00000000(Initial display line 0) DSE="1"

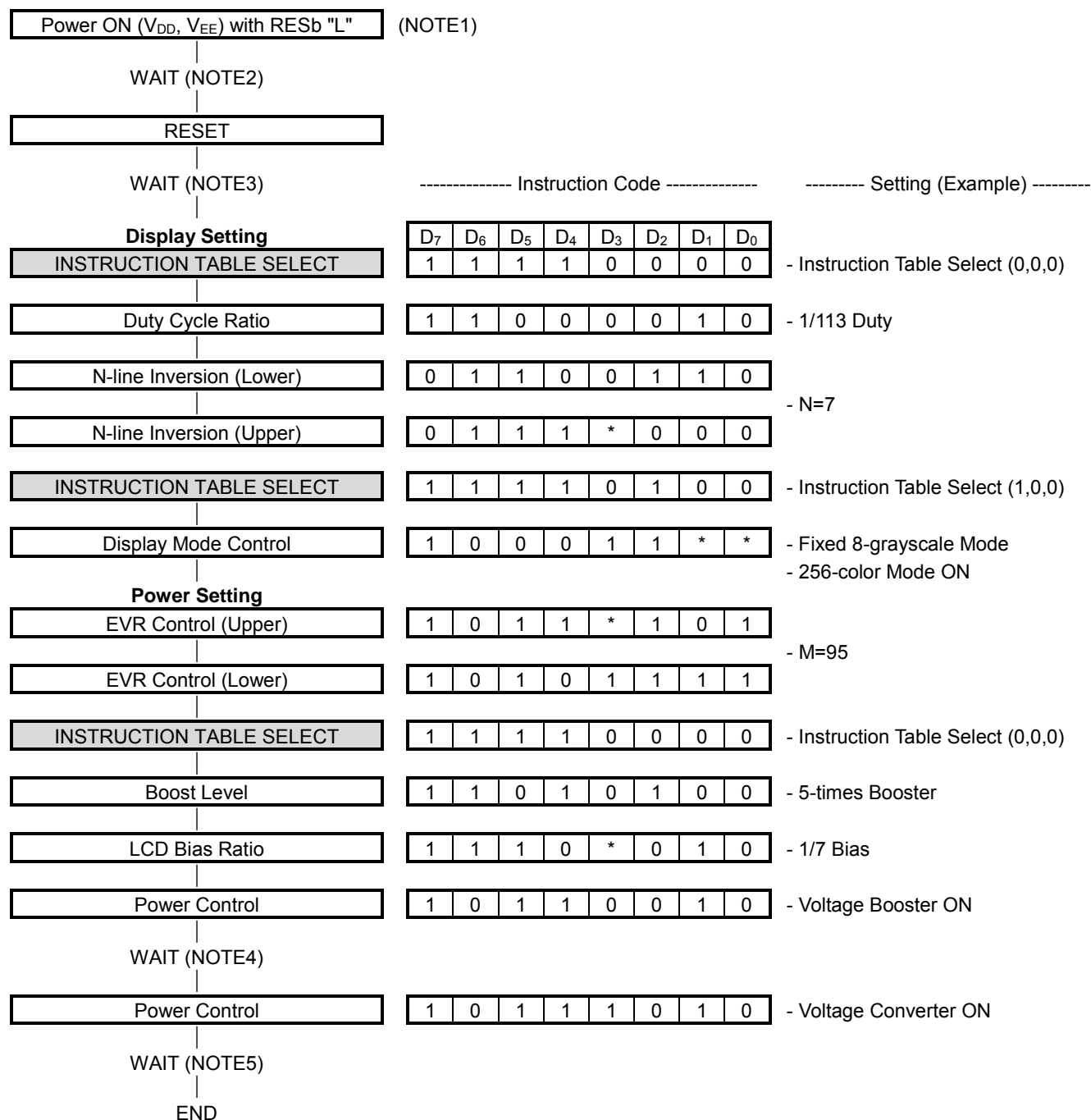
SC3-SC0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
COM0	0	124	120	112	104	96	88	80	72	64	56	48	40	32	24	16
COM1		↓														
COM2		127														
COM3		0														
COM4		↓														
COM5		127														
COM6		0														
COM7		↓														
COM8		127														
COM9		0														
COM10		↓														
COM11		127														
COM12		0														
COM13		↓														
COM14		127														
COM15		0														
COM16		↓														
COM17		127														
COM18		0														
COM19		↓														
COM20		127														
COM21		0														
COM22		↓														
COM23		127														
COM24		0														
COM25		↓														
COM26		127														
COM27		0														
COM28		↓														
COM29		127														
COM30		0														
COM31		↓														
COM32		127														
COM33		0														
COM34		↓														
COM35		127														
COM36		0														
COM37		↓														
COM38		127														
COM39		0														
COM40		↓														
COM41		127														
COM42		0														
COM43		↓														
COM44		127														
COM45		0														
COM46		↓														
COM47		127														
COM48		0														
COM49		↓														
COM50		127														
COM51		0														
COM52		↓														
COM53		127														
COM54		0														
COM55		↓														
COM56		127														
COM57		0														
COM58		↓														
COM59		127														
COM60		0														
COM61		↓														
COM62		127														
COM63		0														
COM64		↓														
COM65		127														
COM66		0														
COM67		↓														
COM68		127														
COM69		0														
COM70		↓														
COM71		127														
COM72		0														
COM73		↓														
COM74		127														
COM75		0														
COM76		↓														
COM77		127														
COM78		0														
COM79		↓														
COM80		127														
COM81		0														
COM82		↓														
COM83		127														
COM84		0														
COM85		↓														
COM86		127														
COM87		0														
COM88		↓														
COM89		127														
COM90		0														
COM91		↓														
COM92		127														
COM93		0														
COM94		↓														
COM95		127														
COM96		0														
:		↓														
COM103		127														
COM104		0														
:		↓														
COM111		127														
COM112		0														
:		↓														
COM125		127														
COM126		0														
COM127		↓														

Fig 28 Relation between Row address and Common Driver (5)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

## (18) TYPICAL INSTRUCTION SEQUENCES

### (18-1) Initialization Sequence in Using Internal LCD Power Supply



NOTE1) If different power sources are applied to the  $V_{DD}$  and the  $V_{EE}$ , turn on the  $V_{DD}$  first.

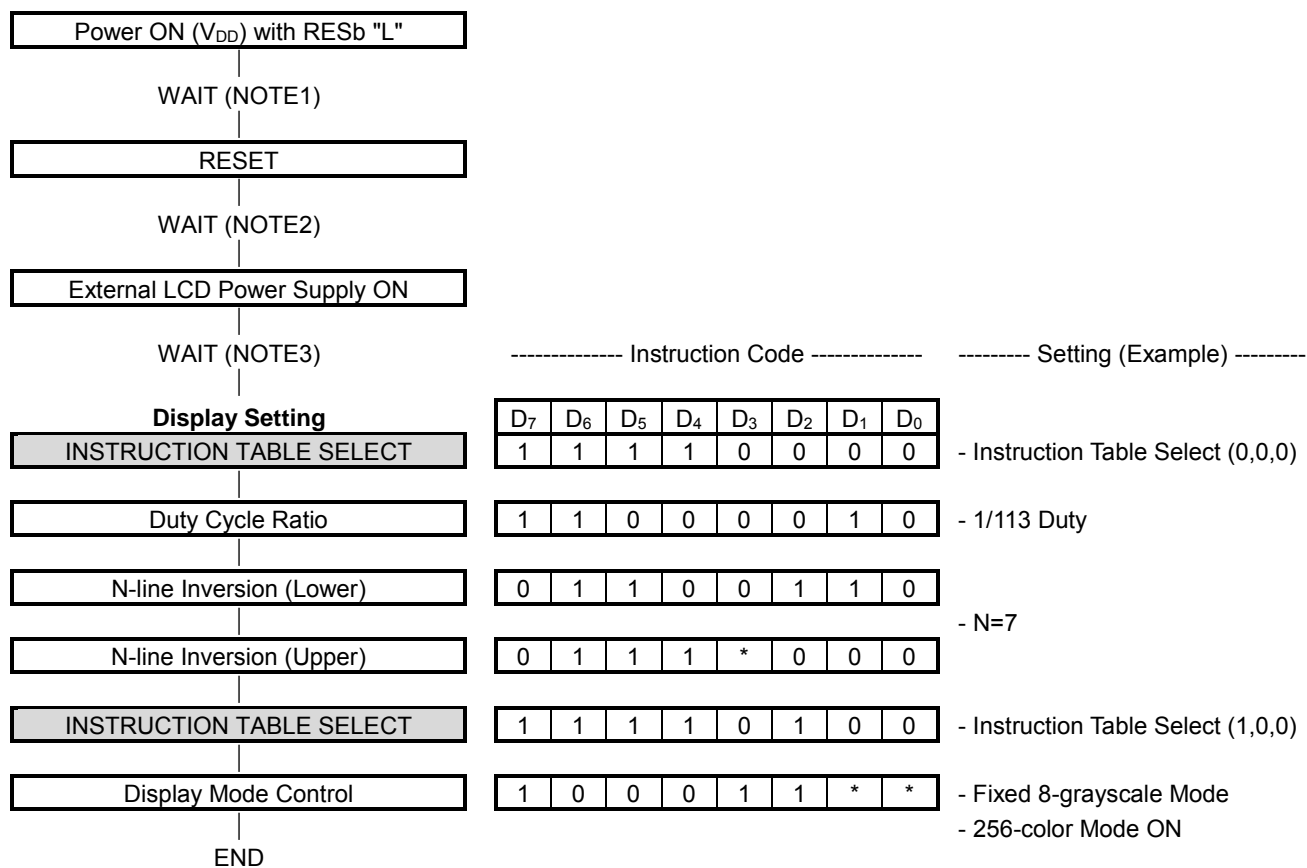
NOTE2) Wait until the  $V_{DD}$  and  $V_{EE}$  are stabilized.

NOTE3) Wait 10 [us] or more.

NOTE4) Wait until the  $V_{OUT}$  is stabilized.

NOTE5) Wait until the  $V_{LCD}$  and  $V_1$ - $V_4$  are stabilized.

## (18-2) Initialization Sequence in Using External LCD Power Supply

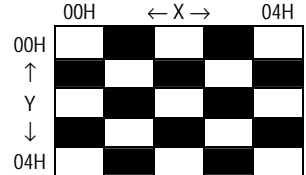
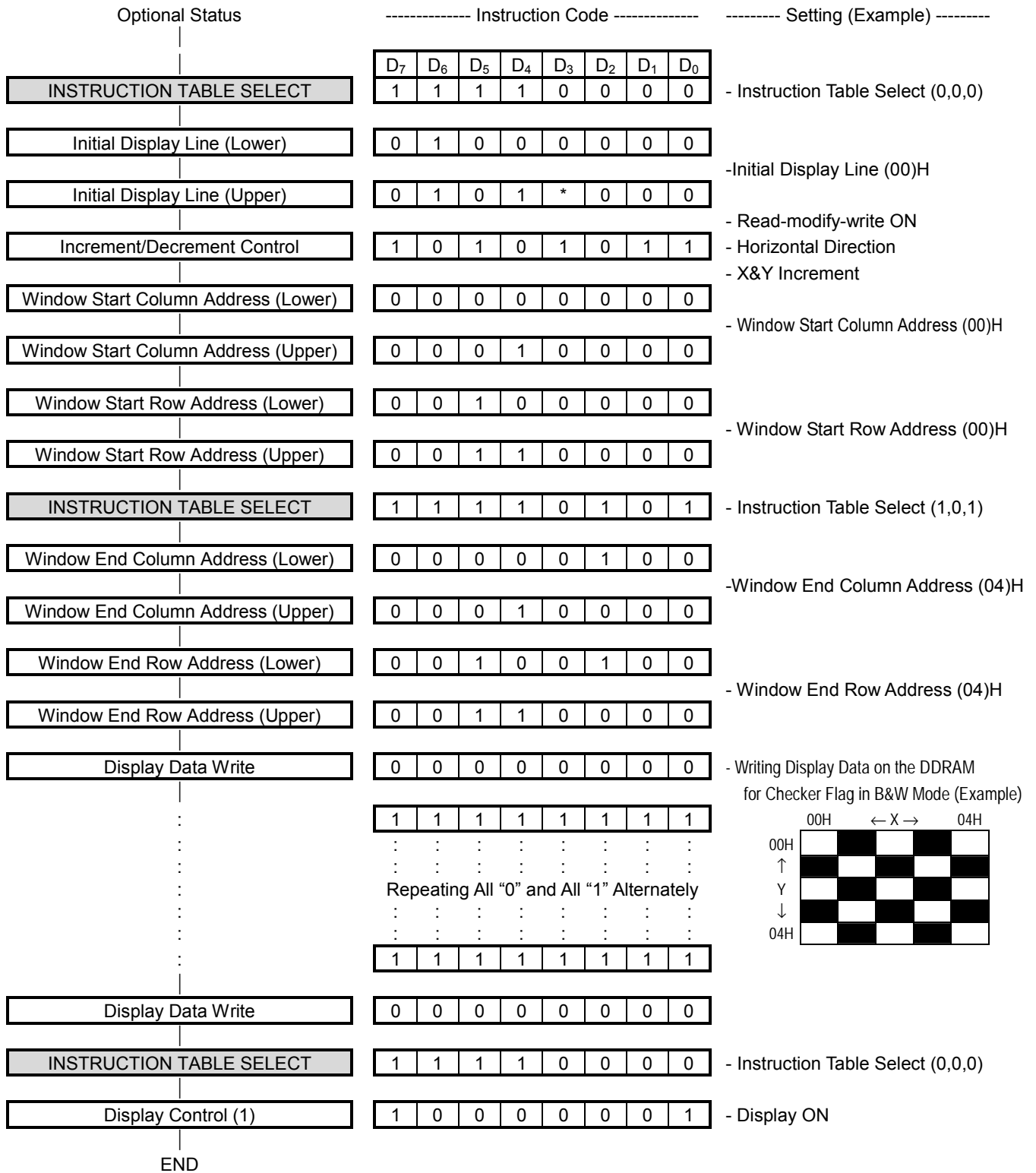


NOTE1) Wait until the  $V_{DD}$  is stabilized.

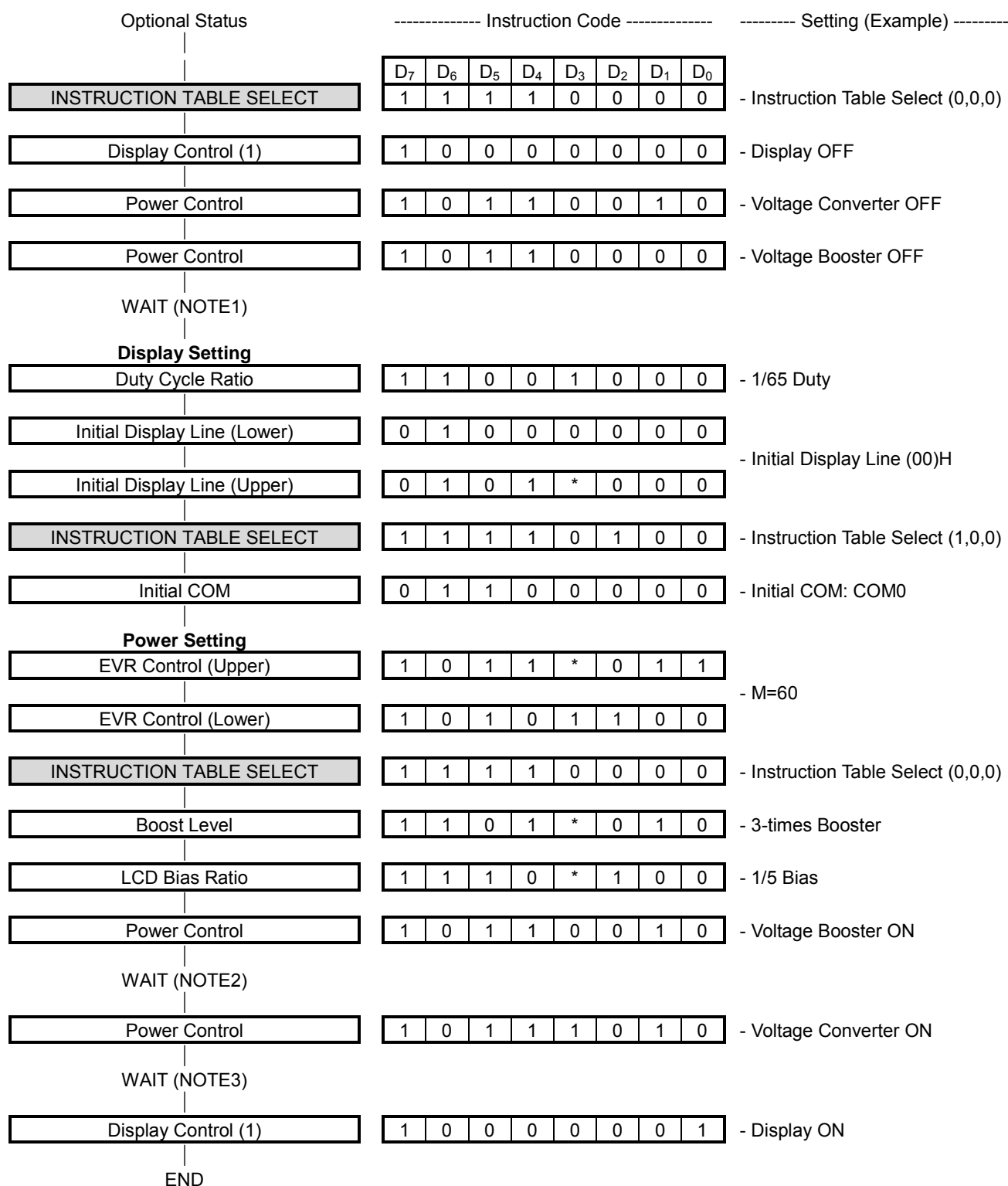
NOTE2) Wait 10 [us] or more.

NOTE3) Wait until the external LCD power supply ( $V_{OUT}$ ,  $V_{LCD}$ ,  $V_1$ - $V_4$ ) are stabilized.

## (18-3) Display Data Write Sequence



## (18-4) Partial Display Sequence



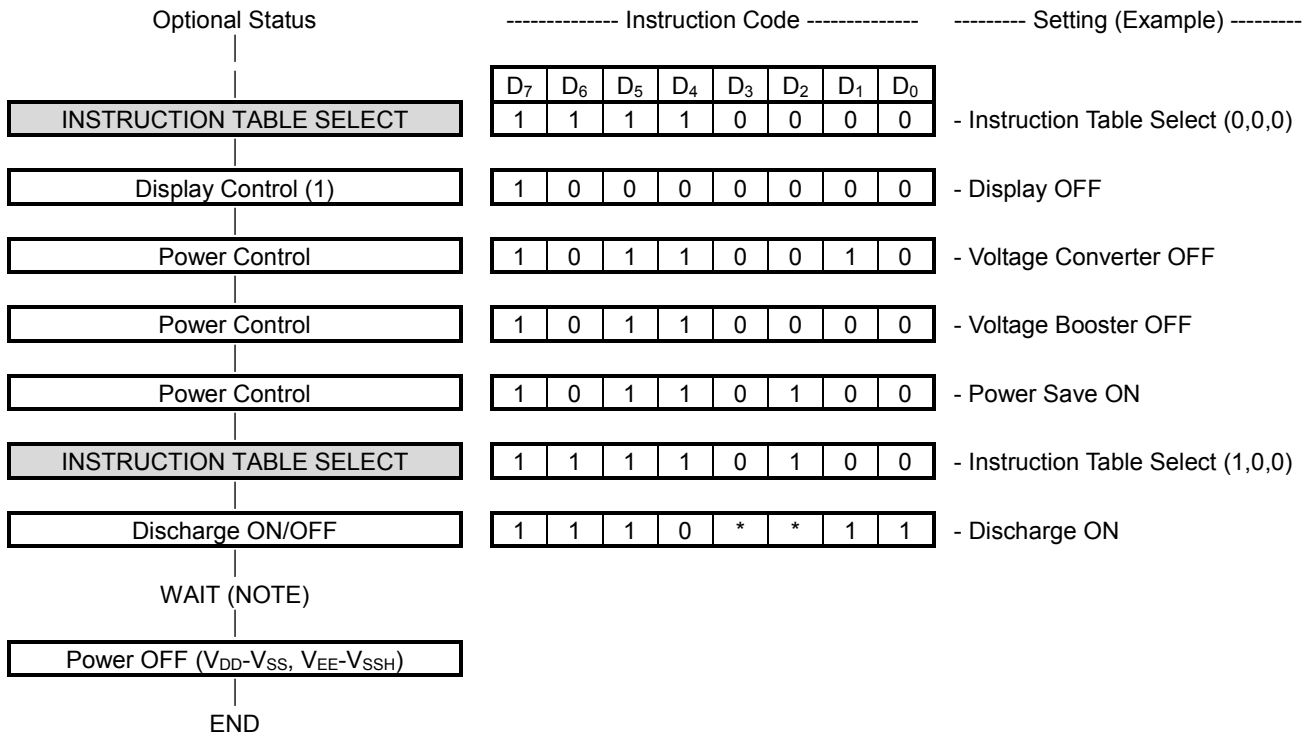
NOTE1) Wait until the voltage booster is completely turned off. Make sure what is the wait time in the particular application.

NOTE2) Wait until the  $V_{OUT}$  is stabilized.

NOTE3) Wait until the  $V_{LCD}$  and  $V_1$ - $V_4$  are stabilized.



## (18-5) Power OFF Sequence



NOTE) Wait until the Discharge is completed.

## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	$V_{DD}$	$V_{SS}=0V$ $V_{SSH}=0V$ $T_a = +25^{\circ}C$	$V_{DD}$	-0.3 to +4.0	V
Supply Voltage (2)	$V_{EE}$		$V_{EE}$	-0.3 to +4.0	V
Supply Voltage (3)	$V_{OUT}$		$V_{OUT}$	-0.3 to +20.0	V
Supply Voltage (4)	$V_{REG}$		$V_{REG}$	-0.3 to +20.0	V
Supply Voltage (5)	$V_{LCD}$		$V_{LCD}$	-0.3 to +20.0	V
Supply Voltage (6)	$V_1, V_2, V_3, V_4$		$V_1, V_2, V_3, V_4$	-0.3 to $V_{LCD} + 0.3$	V
Input Voltage	$V_I$		*1	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	$T_{stg}$			-45 to +125	$^{\circ}C$

NOTE1)  $D_0$  to  $D_{15}$ , CSb, RS, RDb, WRb, OSC1, RESb, TEST1, and TEST2

NOTE2) To stabilize the LSI operation, place decoupling capacitors between  $V_{DD}$  and  $V_{SS}$  and between  $V_{EE}$  and  $V_{SSH}$ .

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	$V_{DD1}$	$V_{DD}$	1.7		3.3	V	1
	$V_{DD2}$		2.4		3.3	V	2
		$V_{EE}$	2.4		3.3	V	3
Operating Voltage	$V_{LCD}$	$V_{LCD}$	5		18.0	V	4
	$V_{OUT}$	$V_{OUT}$			18.0	V	
	$V_{REG}$	$V_{REG}$			$V_{OUT} \times 0.9$	V	
	$V_{REF}$	$V_{REF}$	2.1		3.3	V	5
Operating Temperature	$T_{opr}$		-30		85	$^{\circ}C$	

NOTE1) Applied to the condition when the reference voltage generator is not used.

NOTE2) Applied to the condition when the reference voltage generator is used.

NOTE3) Applied to the condition when the voltage booster is used.

NOTE4) The following relation among the LCD bias voltages must be maintained.

$$V_{SSH} < V_4 < V_3 < V_2 < V_1 < V_{LCD} < V_{OUT}$$

NOTE5) Relation:  $V_{REF} < V_{EE}$  must be maintained.

## DC CHARACTERISTICS

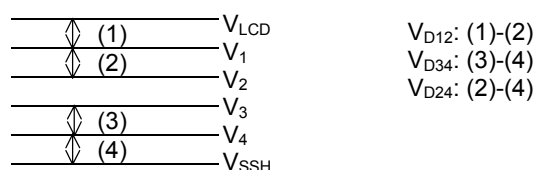
$V_{SS}=0V, V_{SSH}=0V, V_{DD}=+1.7$  to  $+3.3V, T_a=-30$  to  $+85^\circ C$

PARAMETER	SYM BOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE	
"H" Level Input Voltage	$V_{IH}$		$0.8 V_{DD}$		$V_{DD}$	V	1	
"L" Level Input Voltage	$V_{IL}$		0		$0.2V_{DD}$	V	1	
"H" Level Output Voltage	$V_{OH1}$	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$			V	2	
"L" Level Output Voltage	$V_{OL1}$	$I_{OL} = 0.4mA$			0.4	V	2	
"H" Level Output Voltage	$V_{OH2}$	$I_{OH} = -0.1mA$	$V_{DD} - 0.4$			V	3	
"L" Level Output Voltage	$V_{OL2}$	$I_{OL} = 0.1mA$			0.4	V	3	
Input Leakage Current	$I_{LI}$	$V_i = V_{SS}$ or $V_{DD}$	-10		10	$\mu A$	4	
Output Leakage Current	$I_{LO}$	$V_i = V_{SS}$ or $V_{DD}$	-10		10	$\mu A$	5	
Driver ON-resistance	$R_{ON1}$	$ \Delta V_{ON}  = 0.5V$	$V_{LCD} = 10V$	1	2	k $\Omega$	6	
			$V_{LCD} = 6V$		2			4
Stand-by Current	$I_{STB}$	$C_{Sb}=V_{DD},$ $T_a=25^\circ C$	$V_{DD} = 3V$		15	$\mu A$	7	
Oscillation Frequency Using Internal Resistor	$f_{OSC1}$	$V_{DD} = 3V$ $T_a = 25^\circ C$		490	600	710	kHz	8
	$f_{OSC2}$			110	135.5	160		9
	$f_{OSC3}$			15.9	19.4	22.9		10
Oscillation Frequency Using External Resistor	$f_{r1}$	$R_f=15k\Omega$			575	kHz	11	
	$f_{r2}$	$R_f=68k\Omega$			135			
	$f_{r3}$	$R_f=510k\Omega$			19.6			
Voltage Booster Output Voltage	$V_{OUT}$	N-time boost (N=2 to 6) $RL = 500k\Omega (V_{OUT} - V_{SSH})$	$(N \times V_{EE})$ $\times 0.95$			V	12	
Operating Current (1)	$I_{DD1}$	$V_{DD} = 3V,$ 6-time boost All pixels ON		760	1140	$\mu A$	13	
Operating Current (2)	$I_{DD2}$	$V_{DD} = 3V,$ 6-time boost Checker flag display		930	1400			
Operating Current (3)	$I_{DD3}$	$V_{DD} = 3V,$ 5-time boost All pixels ON		520	780			
Operating Current (4)	$I_{DD4}$	$V_{DD} = 3V,$ 5-time boost Checker flag display		650	980			
Operating Current (5)	$I_{DD5}$	$V_{DD} = 3V,$ 4-time boost All pixels ON		360	540			
Operating Current (6)	$I_{DD6}$	$V_{DD} = 3V,$ 4-time boost Checker flag display		450	680			
$V_{BA}$ Output Voltage	$V_{BA}$	$V_{EE} = 2.4$ to $3.3V$	$(0.9 V_{EE})$ $\times 0.98$	$0.9 V_{EE}$	$(0.9 V_{EE})$ $\times 1.02$	V	14	
$V_{REG}$ Output Voltage	$V_{REG}$	$V_{EE} = 2.4$ to $3.3V$ $V_{REF} = 0.9 \times V_{EE}$ N-time boost (N=2 to 6)	$(V_{REF} \times N)$ $\times 0.97$	$(V_{REF} \times N)$	$(V_{REF} \times N)$ $\times 1.03$	V	15	
LCD Bias Voltages	$V_2$		-100	0	+100	mV	16	
	$V_3$		-100	0	+100			
	$V_{D12}$		-30	0	+30			
	$V_{D34}$		-30	0	+30			
	$V_{D24}$		-30	0	+30			

## ■ OSCILLATION FREQUENCY AND FRAME FREQUENCY

OSCILLATOR /EXTERNAL CLOCK	SYM BOL	DISPLAY MODE	FRAME FREQUENCY (FLM)			
			DUTY CYCLE RATIO (1/D) <DSE=0>			
			1/129 to 1/81	1/73 to 1/41	1/33 to 1/25	1/17
Using Internal Oscillator	f <sub>OSC1</sub>	Variable 8-/16-level Grayscale Mode	f <sub>OSC</sub> / (62xD)	f <sub>OSC</sub> / (62xDx2)	f <sub>OSC</sub> / (62xDx4)	f <sub>OSC</sub> / (62xDx8)
	f <sub>OSC2</sub>	Fixed 8-level Grayscale Mode	f <sub>OSC</sub> / (14xD)	f <sub>OSC</sub> / (14xDx2)	f <sub>OSC</sub> / (14xDx4)	f <sub>OSC</sub> / (14xDx8)
	f <sub>OSC3</sub>	B&W Mode	f <sub>OSC</sub> / (2xD)	f <sub>OSC</sub> / (2xDx2)	f <sub>OSC</sub> / (2xDx4)	f <sub>OSC</sub> / (2xDx8)
Using External Clock	f <sub>CK1</sub>	Variable 8-/16-level Grayscale Mode	f <sub>CK</sub> / (62xD)	f <sub>CK</sub> / (62xDx2)	f <sub>CK</sub> / (62xDx4)	f <sub>CK</sub> / (62xDx8)
	f <sub>CK2</sub>	Fixed 8-level Grayscale Mode	f <sub>CK</sub> / (14xD)	f <sub>CK</sub> / (14xDx2)	f <sub>CK</sub> / (14xDx4)	f <sub>CK</sub> / (14xDx8)
	f <sub>CK3</sub>	B&W Mode	f <sub>CK</sub> / (2xD)	f <sub>CK</sub> / (2xDx2)	f <sub>CK</sub> / (2xDx4)	f <sub>CK</sub> / (2xDx8)

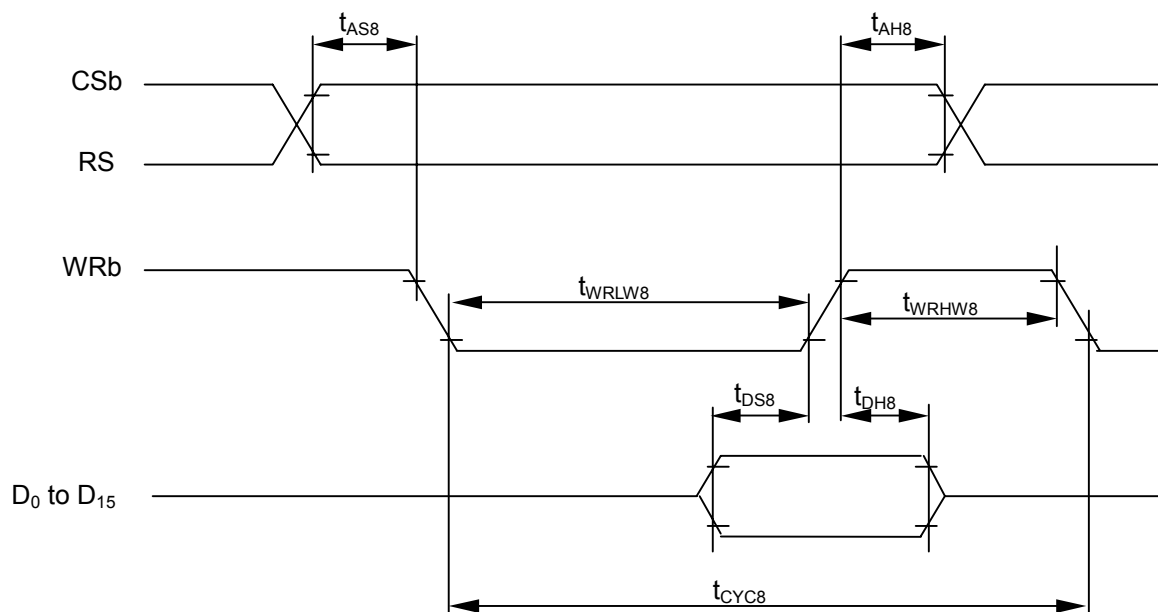
- NOTE1) D<sub>0</sub>-D<sub>15</sub>, CSb, RS, RDb, WRb, P/S, SEL68 and RESb
- NOTE2) D<sub>0</sub>-D<sub>15</sub>
- NOTE3) CL, FLM, FR and CLK
- NOTE4) CSb, RS, SEL68, RDb, WRb, P/S, RESb and OSC1
- NOTE5) D<sub>0</sub>-D<sub>15</sub> in high impedance
- NOTE6) SEGA<sub>0</sub>-SEGA<sub>79</sub>, SEGB<sub>0</sub>-SEGB<sub>79</sub>, SEGC<sub>0</sub>-SEGC<sub>79</sub> and COM<sub>0</sub>-COM<sub>127</sub>  
 This parameter defines the resistance between each COM/SEG and each LCD bias (V<sub>LCD</sub>, V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub> and V<sub>4</sub>).  
 - 0.5V Difference / 1/9 LCD Bias
- NOTE7) V<sub>DD</sub>  
 Oscillator is halted.  
 - CSb=1 (Disabled) / No-load on COM/SEG
- NOTE8) CLK  
 This parameter defines the oscillation frequency by using the internal resistor, in the Variable grayscale mode.  
 - (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE9) CLK  
 This parameter defines the oscillation frequency by using the internal resistor, in the 8-level fixed grayscale mode.  
 - (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE10) CLK  
 This parameter defines the oscillation frequency by using the internal resistor, in the B&W mode.  
 - (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE11) OSC2  
 - V<sub>DD</sub>=3V / Ta=25°C
- NOTE12) V<sub>OUT</sub>  
 This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.  
 - V<sub>EE</sub>=2.4V to 3.3V / EVR= (1,1,1,1,1,1,1) / 1/5 to 1/12 LCD Bias / 1/129 Duty Cycle / No-load on COM/SEG /  
 RL=500kΩ between V<sub>OUT</sub> and V<sub>SSH</sub> / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1"
- NOTE13) V<sub>SS</sub>, V<sub>SSH</sub>  
 This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.  
 - EVR= (1,1,1,1,1,1,1) / All Pixels ON or Checker Flag Display / No-load on COM/SEG / No-access from MPU /  
 V<sub>DD</sub>=V<sub>EE</sub> / V<sub>REF</sub>=0.9V<sub>EE</sub> / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1" / NLIN="0" / 1/129 Duty cycle /  
 Ta=25°C
- NOTE14) V<sub>BA</sub>  
 - V<sub>BA</sub>=V<sub>REF</sub> / Boost Level (N)="1", / DCON="0" / V<sub>OUT</sub>=13.5V
- NOTE15) V<sub>REG</sub>  
 - V<sub>EE</sub>=2.4V to 3.3V / V<sub>REF</sub>=0.9V<sub>EE</sub> / V<sub>OUT</sub>=18V / 1/5 to 1/12 LCD bias ratio / 1/129 duty cycle / EVR=(1,1,1,1,1,1,1) /  
 Checker flag display / No-load on COM/SEG / Boost Level (N)="2" to "6" / CA1=CA2=1.0uF / CA3=0.1uF /  
 DCON="0" / AMPON="1" / NLIN="0"
- NOTE16) V<sub>LCD</sub>, V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub> and V<sub>4</sub>  
 - V<sub>EE</sub>=3.0V / V<sub>REF</sub>=0.9V<sub>EE</sub> / V<sub>OUT</sub>=15V / 1/5 to 1/12 LCD Bias / EVR= (1,1,1,1,1,1,1) / Display OFF / No-load on  
 COM/SEG / Boost Level (N)="5" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1"



# NJU6815

## AC CHARACTERISTICS

### (1) Write Operation (Parallel Interface / 80-series MPU)



( $V_{DD}=2.5$  to  $3.3V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH8}$		0		ns	CSb
Address setup time	$t_{AS8}$		0		ns	RS
System cycle time	$t_{CYC8}$		90		ns	
Enable "L" level pulse width	$t_{WRLW8}$		35		ns	WRb
Enable "H" level pulse width	$t_{WRHW8}$		35		ns	
Data setup time	$t_{DS8}$		30		ns	D <sub>0</sub> to D <sub>15</sub>
Data hold time	$t_{DH8}$		5		ns	

( $V_{DD}=2.2$  to  $2.5V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

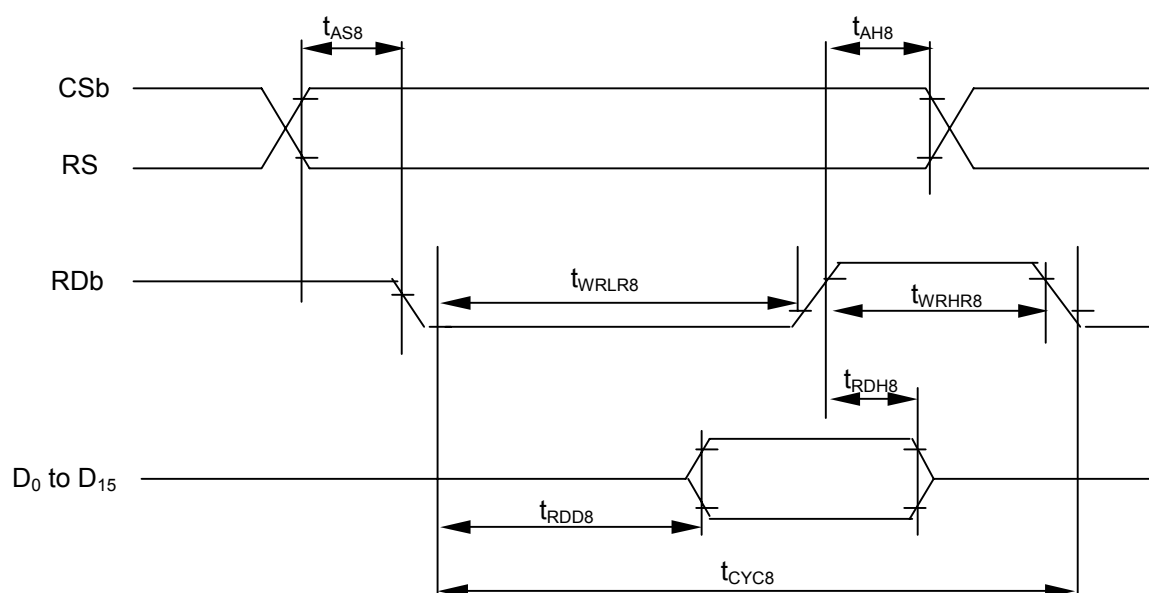
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH8}$		0		ns	CSb
Address setup time	$t_{AS8}$		0		ns	RS
System cycle time	$t_{CYC8}$		160		ns	
Enable "L" level pulse width	$t_{WRLW8}$		70		ns	WRb
Enable "H" level pulse width	$t_{WRHW8}$		70		ns	
Data setup time	$t_{DS8}$		40		ns	D <sub>0</sub> to D <sub>15</sub>
Data hold time	$t_{DH8}$		5		ns	

( $V_{DD}=1.7$  to  $2.2V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH8}$		0		ns	CSb
Address setup time	$t_{AS8}$		0		ns	RS
System cycle time	$t_{CYC8}$		180		ns	
Enable "L" level pulse width	$t_{WRLW8}$		80		ns	WRb
Enable "H" level pulse width	$t_{WRHW8}$		80		ns	
Data setup time	$t_{DS8}$		70		ns	D <sub>0</sub> to D <sub>15</sub>
Data hold time	$t_{DH8}$		10		ns	

NOTE) Each timing is specified based on 20% and 80% of  $V_{DD}$ .

## (2) Read Operation (Parallel Interface / 80-series MPU)



( $V_{DD}=2.5$  to  $3.3V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH8}$		0		ns	CSb
Address setup time	$t_{AS8}$		0		ns	RS
System cycle time	$t_{CYC8}$		180		ns	RDb
Enable "L" level pulse width	$t_{WRLR8}$		80		ns	
Enable "H" level pulse width	$t_{WRHR8}$		80		ns	
Read Data delay time	$t_{RDD8}$	CL=15pF		60	ns	D <sub>0</sub> to D <sub>15</sub>
Read Data hold time	$t_{RDH8}$		0		ns	

( $V_{DD}=2.2$  to  $2.5V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

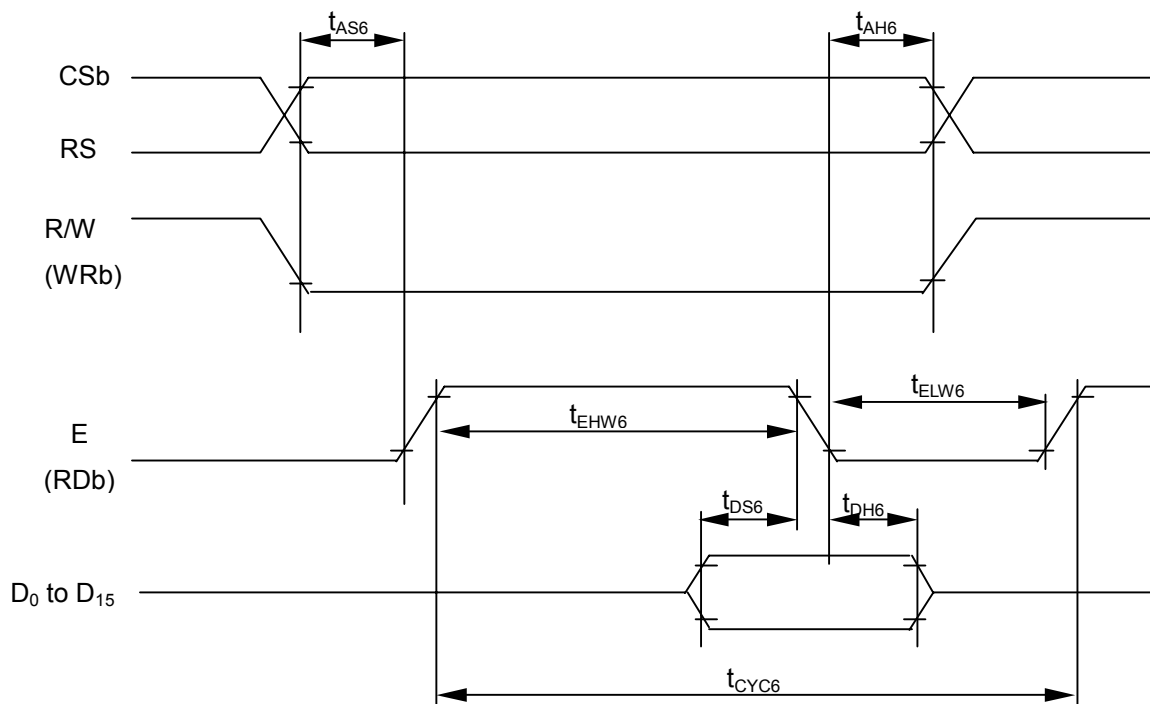
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH8}$		0		ns	CSb
Address setup time	$t_{AS8}$		0		ns	RS
System cycle time	$t_{CYC8}$		180		ns	RDb
Enable "L" level pulse width	$t_{WRLR8}$		80		ns	
Enable "H" level pulse width	$t_{WRHR8}$		80		ns	
Read Data delay time	$t_{RDD8}$	CL=15pF		60	ns	D <sub>0</sub> to D <sub>15</sub>
Read Data hold time	$t_{RDH8}$		0		ns	

( $V_{DD}=1.7$  to  $2.2V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH8}$		0		ns	CSb
Address setup time	$t_{AS8}$		0		ns	RS
System cycle time	$t_{CYC8}$		300		ns	RDb
Enable "L" level pulse width	$t_{WRLR8}$		140		ns	
Enable "H" level pulse width	$t_{WRHR8}$		140		ns	
Read Data delay time	$t_{RDD8}$	CL=15pF		130	ns	D <sub>0</sub> to D <sub>15</sub>
Read Data hold time	$t_{RDH8}$		0		ns	

NOTE) Each timing is specified based on 20% and 80% of  $V_{DD}$ .

## (3) Write Operation (Parallel Interface / 68-series MPU)



( $V_{DD}=2.5$  to  $3.3V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH6}$		0		ns	CSb
Address setup time	$t_{AS6}$		0		ns	RS
System cycle time	$t_{CYC6}$		90		ns	E
Enable "L" level pulse width	$t_{ELW6}$		35		ns	E
Enable "H" level pulse width	$t_{EHW6}$		35		ns	E
Data setup time	$t_{DS6}$		40		ns	D <sub>0</sub> to D <sub>15</sub>
Data hold time	$t_{DH6}$		5		ns	D <sub>0</sub> to D <sub>15</sub>

( $V_{DD}=2.2$  to  $2.5V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH6}$		0		ns	CSb
Address setup time	$t_{AS6}$		0		ns	RS
System cycle time	$t_{CYC6}$		160		ns	E
Enable "L" level pulse width	$t_{ELW6}$		70		ns	E
Enable "H" level pulse width	$t_{EHW6}$		70		ns	E
Data setup time	$t_{DS6}$		50		ns	D <sub>0</sub> to D <sub>15</sub>
Data hold time	$t_{DH6}$		5		ns	D <sub>0</sub> to D <sub>15</sub>

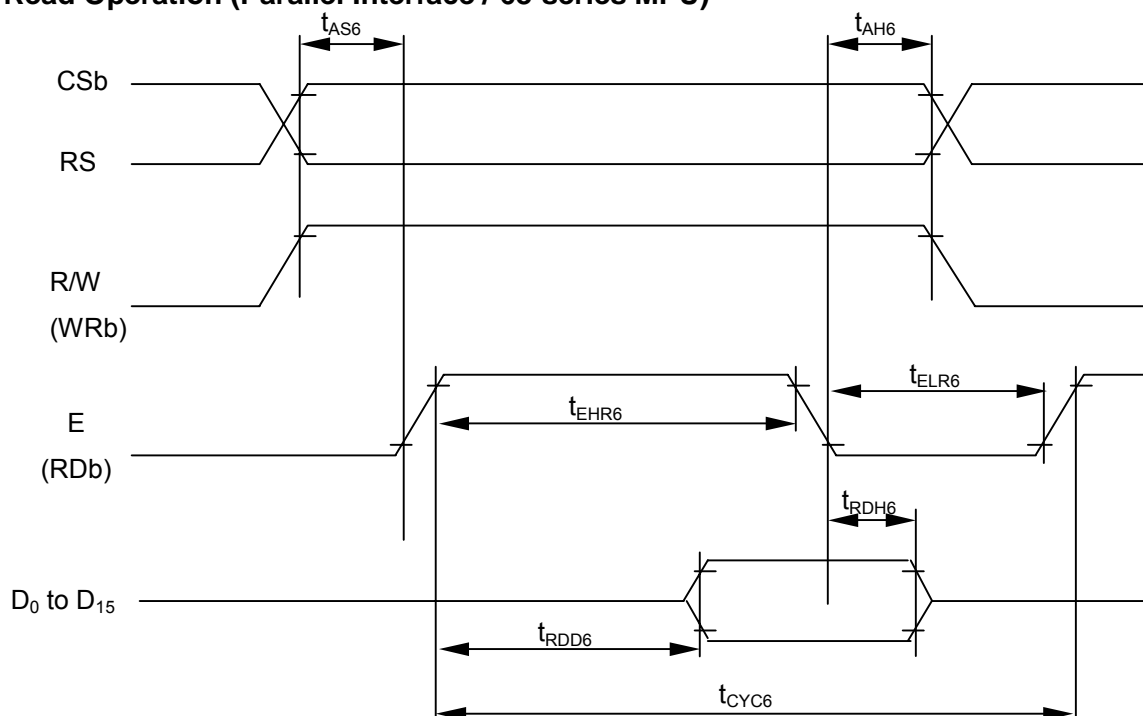
( $V_{DD}=1.7$  to  $2.2V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH6}$		0		ns	CSb
Address setup time	$t_{AS6}$		0		ns	RS
System cycle time	$t_{CYC6}$		180		ns	E
Enable "L" level pulse width	$t_{ELW6}$		80		ns	E
Enable "H" level pulse width	$t_{EHW6}$		80		ns	E
Data setup time	$t_{DS6}$		70		ns	D <sub>0</sub> to D <sub>15</sub>
Data hold time	$t_{DH6}$		10		ns	D <sub>0</sub> to D <sub>15</sub>

NOTE) Each timing is specified based on 20% and 80% of  $V_{DD}$ .



## (4) Read Operation (Parallel Interface / 68-series MPU)



( $V_{DD}=2.5$  to  $3.3V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH6}$		0		ns	CSb
Address setup time	$t_{AS6}$		0		ns	RS
System cycle time	$t_{CYC6}$		180		ns	E
Enable "L" level pulse width	$t_{ELR6}$		80		ns	
Enable "H" level pulse width	$t_{EHR6}$		80		ns	
Read Data delay time	$t_{RDD6}$	CL=15pF	0	70	ns	D <sub>0</sub> to D <sub>15</sub>
Read Data hold time	$t_{RDH6}$		0		ns	

( $V_{DD}=2.2$  to  $2.5V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

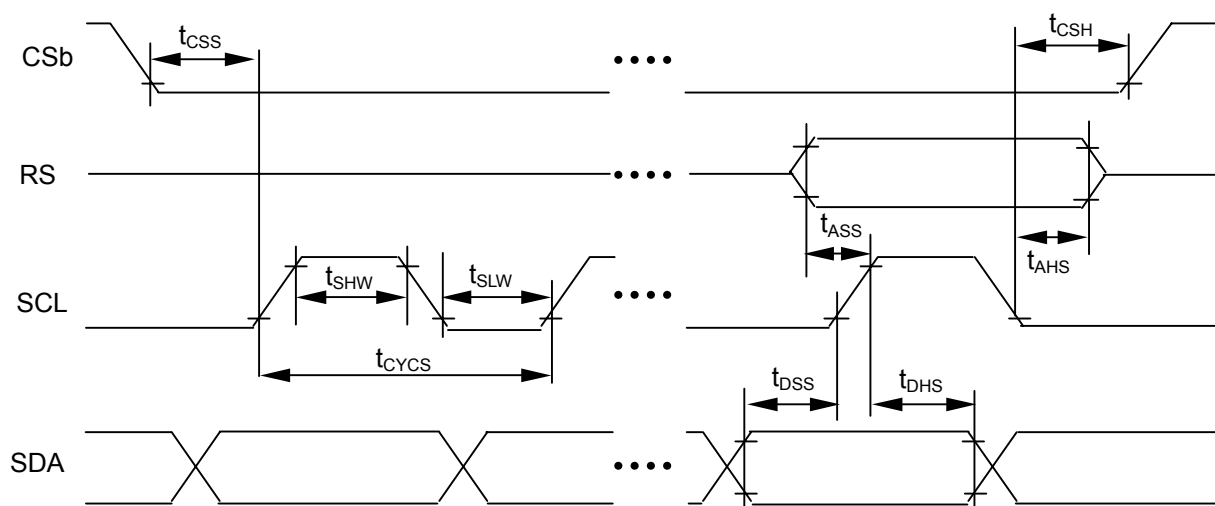
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH6}$		0		ns	CSb
Address setup time	$t_{AS6}$		0		ns	RS
System cycle time	$t_{CYC6}$		180		ns	E
Enable "L" level pulse width	$t_{ELR6}$		80		ns	
Enable "H" level pulse width	$t_{EHR6}$		80		ns	
Read Data delay time	$t_{RDD6}$	CL=15pF	0	70	ns	D <sub>0</sub> to D <sub>15</sub>
Read Data hold time	$t_{RDH6}$		0		ns	

( $V_{DD}=1.7$  to  $2.2V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	$t_{AH6}$		0		ns	CSb
Address setup time	$t_{AS6}$		0		ns	RS
System cycle time	$t_{CYC6}$		300		ns	E
Enable "L" level pulse width	$t_{ELR6}$		140		ns	
Enable "H" level pulse width	$t_{EHR6}$		140		ns	
Read Data delay time	$t_{RDD6}$	CL=15pF	0	130	ns	D <sub>0</sub> to D <sub>15</sub>
Read Data hold time	$t_{RDH6}$		0		ns	

NOTE) Each timing is specified based on 20% and 80% of  $V_{DD}$ .

## (5) Serial Interface



( $V_{DD}=2.5$  to  $3.3V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	$t_{CYCS}$		50		ns	SCL
SCL "H" level pulse width	$t_{SHW}$		20		ns	SCL
SCL "L" level pulse width	$t_{SLW}$		20		ns	SCL
Address setup time	$t_{ASS}$		20		ns	RS
Address hold time	$t_{AHS}$		20		ns	RS
Data setup time	$t_{DSS}$		20		ns	SDA
Data hold time	$t_{DHS}$		20		ns	SDA
CSb – SCL time	$t_{CSS}$		20		ns	CSb
CSb hold time	$t_{CSH}$		20		ns	CSb

( $V_{DD}=2.2$  to  $2.5V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

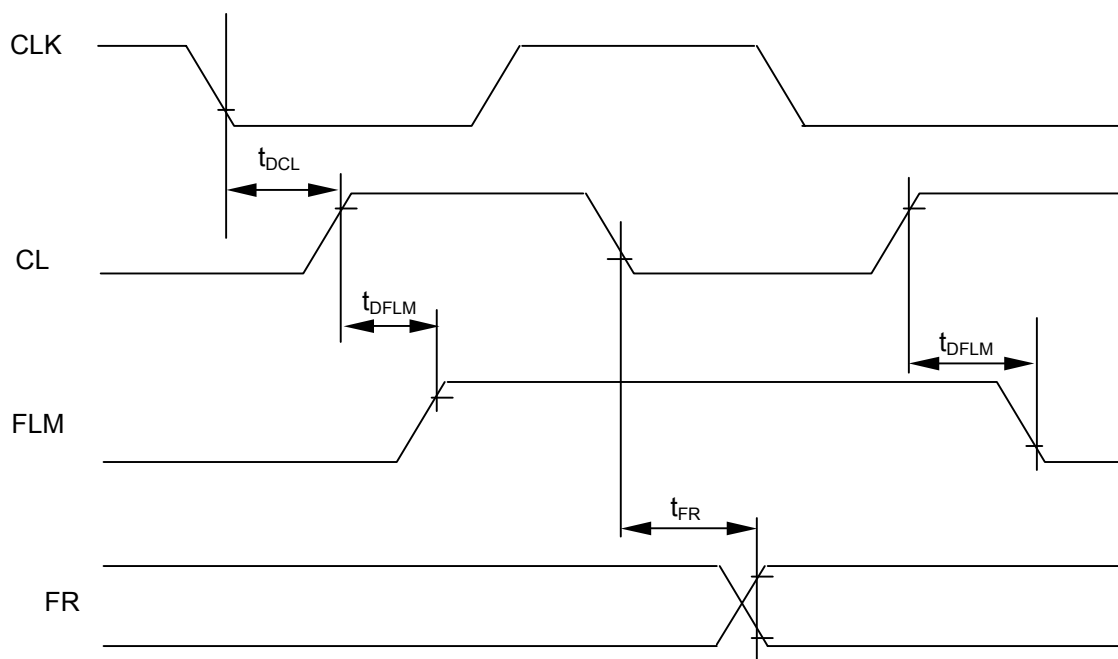
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	$t_{CYCS}$		50		ns	SCL
SCL "H" level pulse width	$t_{SHW}$		20		ns	SCL
SCL "L" level pulse width	$t_{SLW}$		20		ns	SCL
Address setup time	$t_{ASS}$		20		ns	RS
Address hold time	$t_{AHS}$		20		ns	RS
Data setup time	$t_{DSS}$		20		ns	SDA
Data hold time	$t_{DHS}$		20		ns	SDA
CSb – SCL time	$t_{CSS}$		20		ns	CSb
CSb hold time	$t_{CSH}$		20		ns	CSb

( $V_{DD}=1.7$  to  $2.2V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	$t_{CYCS}$		80		ns	SCL
SCL "H" level pulse width	$t_{SHW}$		35		ns	SCL
SCL "L" level pulse width	$t_{SLW}$		35		ns	SCL
Address setup time	$t_{ASS}$		35		ns	RS
Address hold time	$t_{AHS}$		35		ns	RS
Data setup time	$t_{DSS}$		35		ns	SDA
Data hold time	$t_{DHS}$		35		ns	SDA
CSb – SCL time	$t_{CSS}$		35		ns	CSb
CSb hold time	$t_{CSH}$		35		ns	CSb

NOTE) Each timing is specified based on 20% and 80% of  $V_{DD}$ .

## (6) Display Control Timing



Output timing

( $V_{DD}=2.4$  to  $3.3V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	$t_{DFLM}$	CL=15pF	0	500	ns	FLM
FR delay time	$t_{FR}$		0	500	ns	FR
CL delay time	$t_{DCL}$		0	200	ns	CL

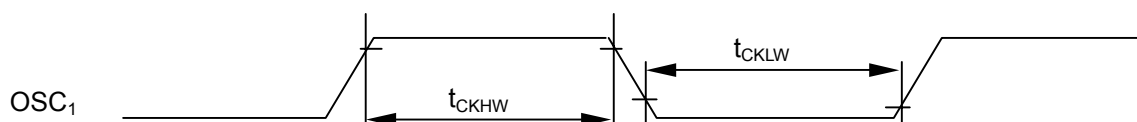
Output timing

( $V_{DD}=1.7$  to  $2.4V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	$t_{DFLM}$	CL=15pF	0	1000	ns	FLM
FR delay time	$t_{FR}$		0	1000	ns	FR
CL delay time	$t_{DCL}$		0	200	ns	CL

NOTE) Each timing is specified based on 20% and 80% of  $V_{DD}$ .

## (7) Input Clock Timing



( $V_{DD}=1.7$  to  $3.3V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC1 "H" level pulse width (1)	$t_{CKHW1}$		0.70	1.02	$\mu s$	OSC1 (NOTE2)
OSC1 "L" level pulse width (1)	$t_{CKLW1}$		0.70	1.02	$\mu s$	
OSC1 "H" level pulse width (2)	$t_{CKHW2}$		3.13	4.55	$\mu s$	OSC1 (NOTE3)
OSC1 "L" level pulse width (2)	$t_{CKLW2}$		3.13	4.55	$\mu s$	
OSC1 "H" level pulse width (3)	$t_{CKHW3}$		21.8	31.4	$\mu s$	OSC1 (NOTE4)
OSC1 "L" level pulse width (3)	$t_{CKLW3}$		21.8	31.4	$\mu s$	

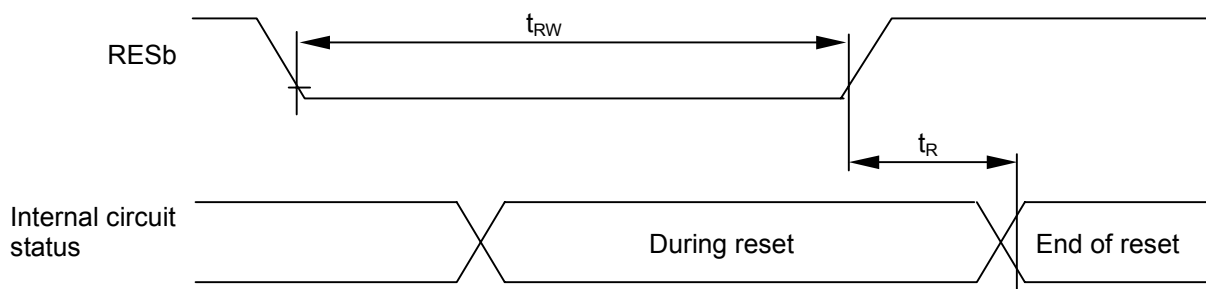
NOTE1) Each timing is specified based on 20% and 80% of  $V_{DD}$ .

NOTE2) Applied to Variable 8-/16-level grayscale mode (MON="0", PWM="0")

NOTE3) Applied to fixed 8-level grayscale mode (MON="0", PWM="1")

NOTE4) Applied to B&W mode (MON="1")

## (8) Reset Input Timing



( $V_{DD}=2.4$  to  $3.3V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	$t_R$			1.0	$\mu s$	
RESb "L" level pulse width	$t_{RW}$		10.0		$\mu s$	RESb

( $V_{DD}=1.7$  to  $2.4V$ ,  $T_a=-30$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	$t_R$			1.5	$\mu s$	
RESb "L" level pulse width	$t_{RW}$		10.0		$\mu s$	RESb

NOTE) Each timing is specified based on 20% and 80% of  $V_{DD}$ .

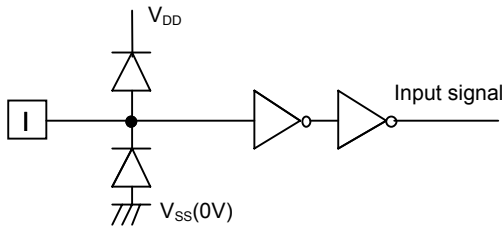
## (9) Delay Time of Gate

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Delay time of gate	$T_a=+25^{\circ}C$ , $V_{SS}=0V$ , $V_{DD}=3.0V$		10		ns

## INPUT/OUTPUT BLOCK DIAGRAMS

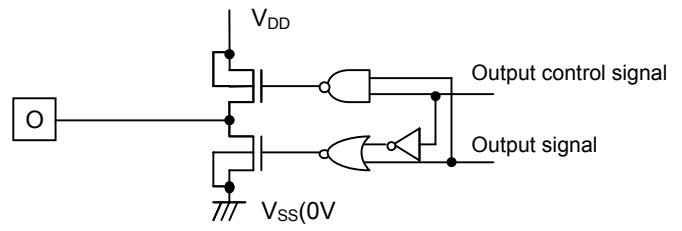
### Input Block Diagram

Terminals CSb, RS, RDb, WRb, SEL68, P/S, RESb



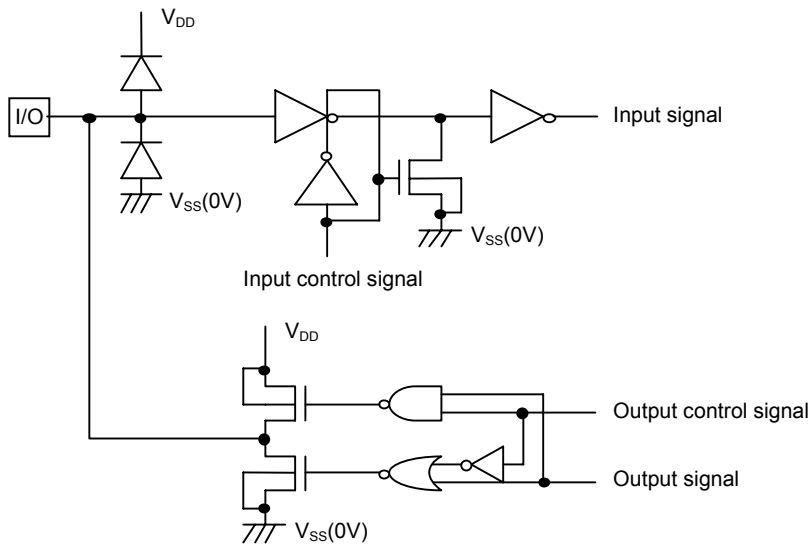
### Output Block Diagram

Terminals : FLM, CL, FR, CLK



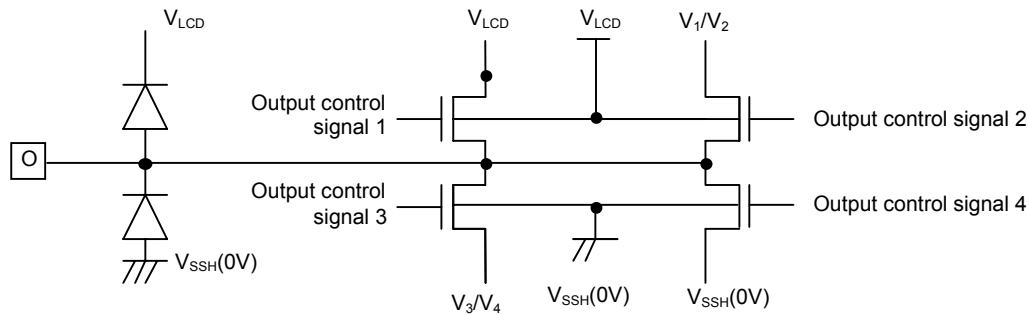
### Input/Output Block Diagram

Terminals : D<sub>0</sub> - D<sub>15</sub>



### COM/SEG Driver Block Diagram

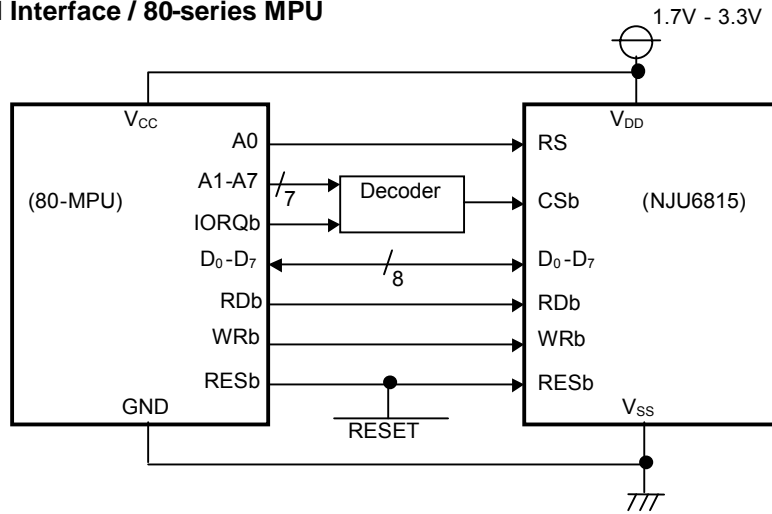
Terminals : SEGA<sub>0</sub>/B<sub>0</sub>/C<sub>0</sub> - SEGA<sub>79</sub>/B<sub>79</sub>/C<sub>79</sub>, COM<sub>0</sub> - COM<sub>127</sub>



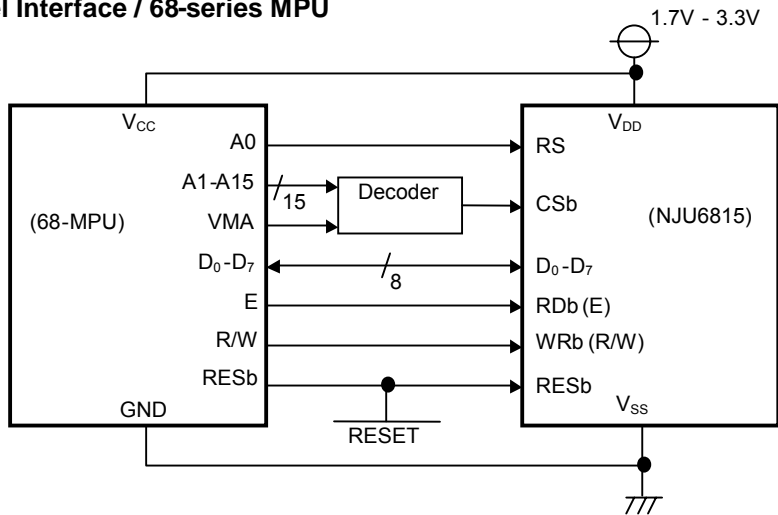
# NJU6815

## MPU CONNECTIONS

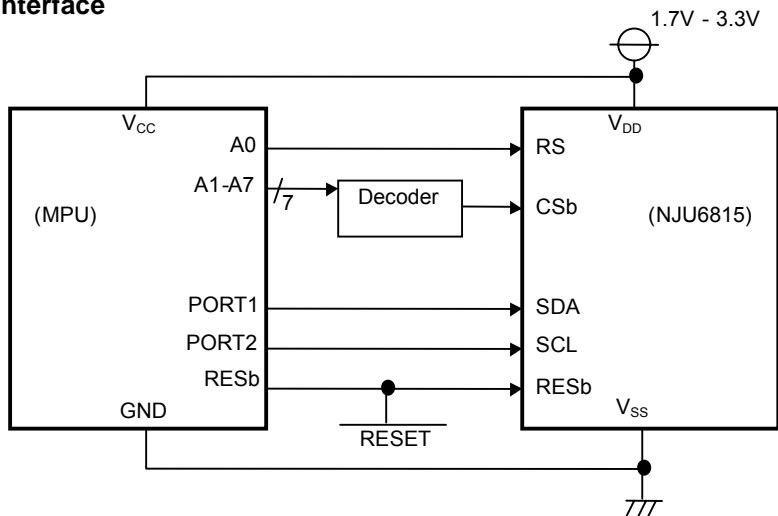
Parallel Interface / 80-series MPU



Parallel Interface / 68-series MPU



Serial Interface



**[CAUTION]**

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