

BAND PASS FILTER FOR AUDIO SPECTRUM ANALYZER DISPLAY

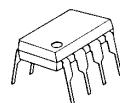
■ GENERAL DESCRIPTION

The NJU7505 is a band pass filter for audio spectrum analyzer display. It consists of high and low band pass filters, CR oscillation circuit, control circuit and DC transfer circuit.

Each band pass filter using the switched capacitor filter technology operates at the shared time by 5 bands which filter constant is switched by the internal clock. Therefore, the audio signal shared of 5 bands is output from a serial output terminal.

The 10 band version using the double by the cascade connection is prepared.

■ PACKAGE OUTLINE



NJU7505XD



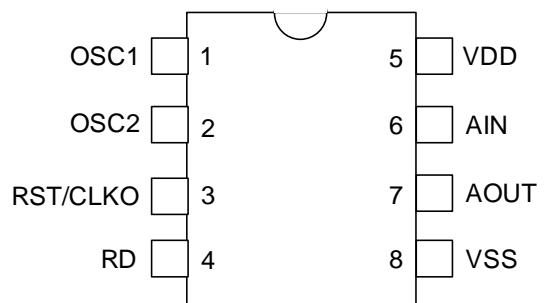
NJU7505XM

■ FEATURES

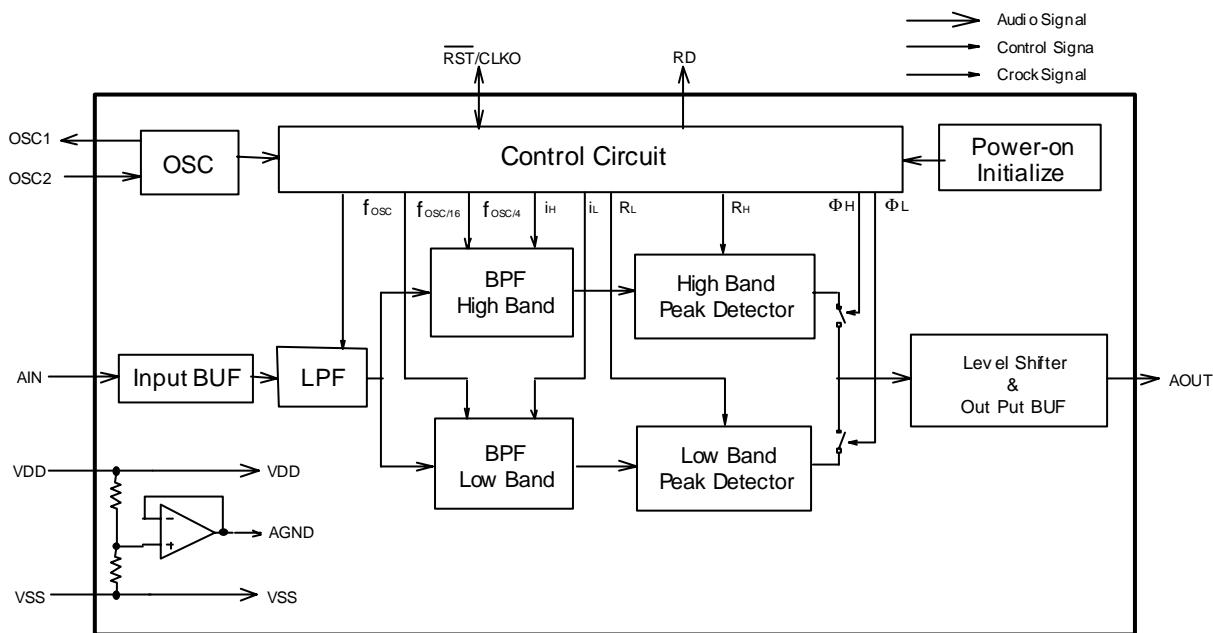
- BPF for the audio spectrum analyzer display of the 5 bands
- 10 bands extension is available by the cascade connection
(Version of A: For 5-band application by the single)
(Version of B: For 10-band application by the double)
- BPF using the switched capacitor filter technology
- CR oscillation circuit on chip
(External clock input is available)
- Power-on initialization circuit on chip
(External reset input is available)
- C-MOS Technology
- Package Outline

DIP8, DMP8

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



NJU7505

■ TERMINAL DESCRIPTION

NO.	SYMBOL	FUNCTION
1	OSC1	External Resistor connecting terminal.
2	OSC2	External Resistor connecting terminal or External clock input terminal.
3	<u>RST/CLK0</u>	Both as Reset input terminal and the clock of $(2/3) * f_{OSC}$ output terminal.
4	RD	Trigger signal for reading-out the A_{OUT} of each band output terminal.
5	V_{SS}	GND 0V
8	V_{DD}	Positive power supply +5.0 V
6	A_{OUT}	Peak voltage of each band output terminal.
7	A_{IN}	Audio signal input terminal.

■ VERSION LINEUP AND PEAK FREQUENCY

The NJU7505 prepares two version of A and B which are different of the peak frequency of each bands.

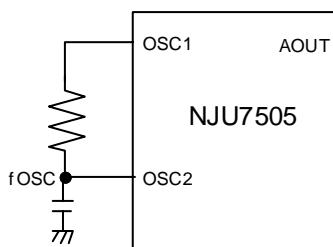
The version of A is recommended for the 5 bands application using the single and the version of B is recommended for the 10 bands using the double by the cascade connection, however, the version of A can be used for the 10 bands using the double and the version of B can be used for the 5 bands using the single.

Band	Peak Frequency (Hz)			
	Using the single		Using the double	
	Version of A	Version of B	Version of A	Version of B
f1a	12k	18k	12k	18k
f1b	-	-	8k	12k
f2a	3.5k	5.3k	3.5k	5.3k
f2b	-	-	2.3k	3.5k
f3a	1k	1.5k	1k	1.5k
f3b	-	-	670	1k
f4a	250	375	250	375
f4b	-	-	165	250
f5a	63	95	63	95
f5b	-	-	42*	63

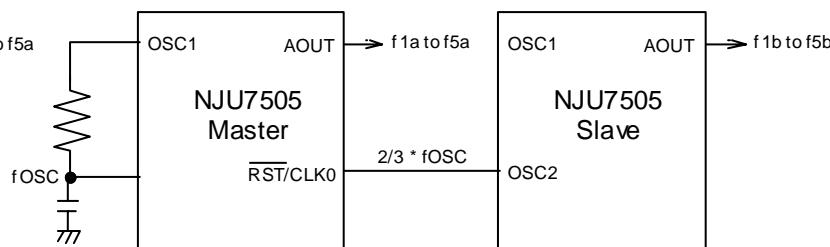
Note) The bands of f1a, f2a, ... f5a correspond to the master side and the bands of f1b, f2b, ... f5b correspond to the slave side at the cascade connection of the double.

Note) It may not be output along the expectation at the peak frequency of * marking, since the sampling time is not enough.

The example of using the single



The example of using the double



■ FUNCTIONAL DESCRIPTION

● Interface to external controller

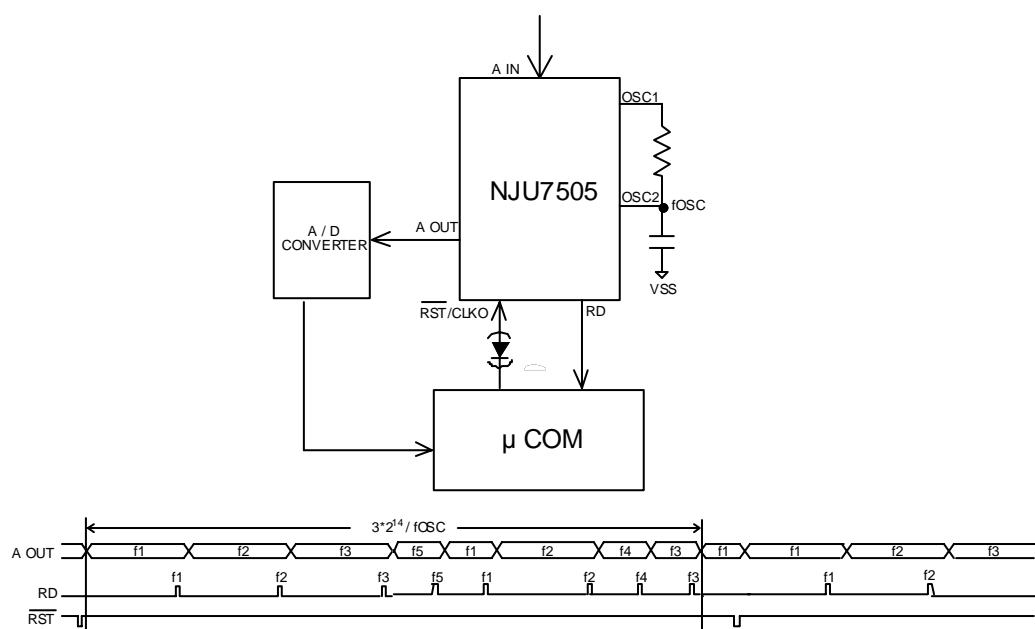
The example of the interface between the NJU7505 and the external controller is shown below;

(1) Example of the interface to the external controller (Using the single)

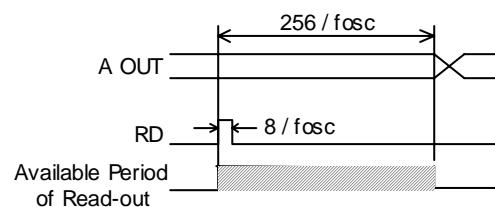
After the RST signal from the external controller is input and then the internal circuit is initialized, each band data is output as shown below timing chart;

Since the RD signal is output before each band is switched, the external controller is to count the number of the RD signal and is to recognize the status of the band and is to read the output data from the A_{OUT} terminal through the external A/D converter.

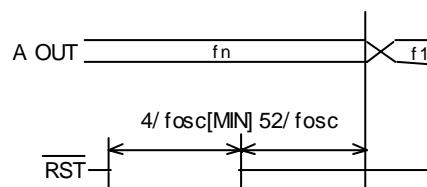
The output type of the external controller connected to the $RST/CLK0$ terminal as the \overline{RST} input should be the N-channel and open-drain type or the diode should be connected between the $RST/CLK0$ terminal and the output terminal of the external controller, so that the voltage of the $RST/CLK0$ terminal is not gotten over the V_{SS} level.



Since the RD signal is output before $256/f_{osc}$ of each band switched, the output data should be read out within the limited time as shown right;



If the \overline{RST} signal which pulse width is more than $4/f_{osc}$ is input, the internal circuit is initialized and the data of f_1 band is output from the A_{OUT} terminal after $52/f_{osc}$ of the rise edge of the \overline{RST} signal.



(2) Example of the interface to the external controller (Using the double)

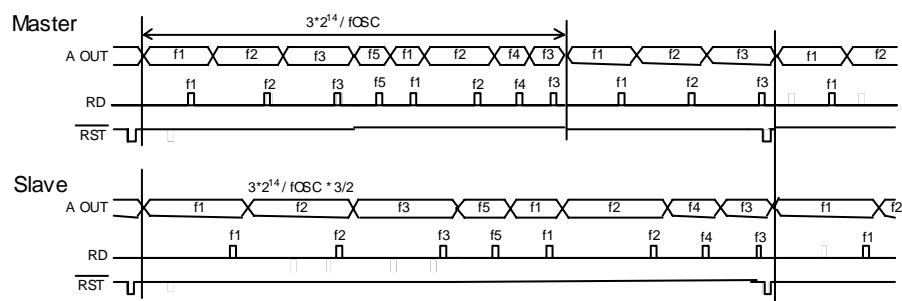
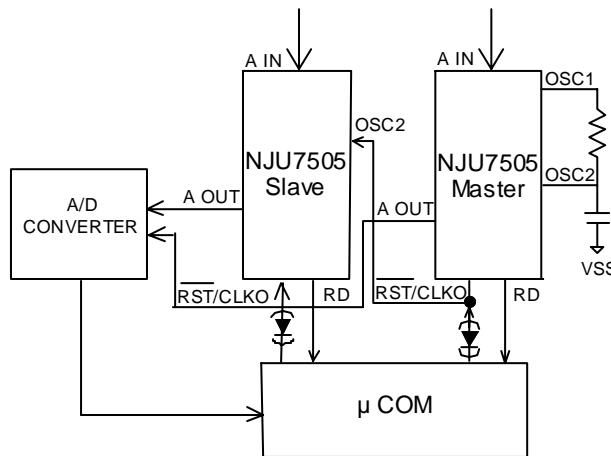
The 10 bands application is available using the cascade connection of the double NJU7505 as shown below.

After the RST signals from the external controller are input to each of the master and the slave of the NJU7505 and then each internal circuit is initialized, each band data is output as shown below timing chart;

Since the RD signals are output from the master and the slave before each band is switched, the external controller is to count the number of the RD signals and is to recognize the status of the band and is to read the output data from each A_{OUT} terminals through the external A/D converter.

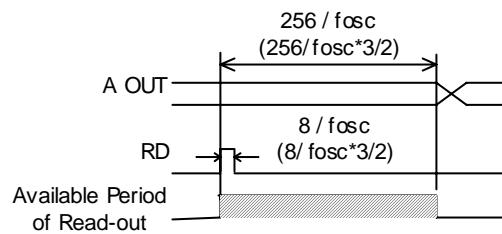
The master clock for the slave is provided with the output signal from the RST/CLK0 terminal of the master. The master clock for the slave is stopped when the RST signal is input from the external controller to the master, so that the RST/CLK0 terminal of the master is used both as the RST input of the master and the master clock for the slave.

The output type of the external controller connected to each RST/CLK0 terminal as the RST input should be the N-channel and open-drain type or the diode's should be connected between each RST/CLK0 terminal and the output terminals of the external controller, so that the voltage of each RST/CLK0 terminal is not gotten over the V_{SS} level.



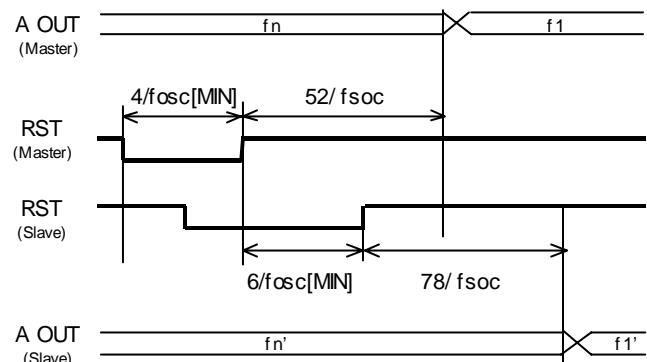
Since each RD signal of the master and the slave is output before $256/f_{osc}$ ($256/f_{osc} \times 3/2$) of each band switched, the output data should be read out within the limited time as shown right;

* The "()" is corresponded to the slave.



If the RST signal which pulse width is more than $4/f_{osc}$ is input to the master, the internal circuit is initialized and the data of f1 band is output from the A_{OUT} terminal of the master after $52/f_{osc}$ of the rise edge of the RST signal.

The RST signal for the slave should be set to "L" level while the RST signal for the master is "L" level and should keep "L" level more than $6/f_{osc}$. So the slave operates as same as the master after $78/f_{osc}$ of the rise edge of the RST signal for the slave.



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage	V _{DD}	-0.3 to +7	V	
Input Voltage	V _{IN}	-0.3 to V _{DD} +0.3	V	5
	V _{IO}	-0.3 to 0		3, 6
Output Voltage	V _{OUT}	-0.3 to V _{DD} +0.3	V	
Power Dissipation	P _D	500(DIP), 300(DMP)	mW	
Operating Temperature	T _{opr}	-30 to 85	°C	
Storage Temperature	T _{stg}	-55 to 125	°C	

Note 1) If the IC are used on condition above the absolute maximum ratings, the IC may be destroyed. Using the IC within electric characteristic conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0V.

Note 3) When the voltage of the RST/CLK0 terminal is gotten over the V_{SS} level, the diode should be connected between the RST/CLK0 terminal and the external.

Note 4) Decoupling capacitor should be connected between the V_{DD} terminal and the V_{SS} due to the stabilization of the operation.

Note 5) Applied to the A_{IN} or the OSC2 terminals.

Note 6) Applied to the RST/CLK0 terminal.

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(V_{DD}=5V, V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	CONDITITONS	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage	V _{DD}		4.5	5.0	6.0	V	
Operating Current	I _{DD}	V _{DD} TERMINAL	-	6.0	12	mA	
Input Leak Current 1	I _{IL1}	A _{IN} TERMINAL	V _{IL1} =0V	-0.1	-0.05	-0.033	mA
	I _{IH1}		V _{IH1} =5V	0.033	0.05	0.1	
Input Leak Current 2	I _{IL2}	RST/CLK0 TERMINAL	V _{IL2} =0V	-0.2	-0.1	-0.05	mA
External Clock	V _{ILC}	OSC2 TERMINAL		0	-	1.5	V
Input Voltage	V _{IHC}			3.5	-	5.0	
Output Voltage 1	V _{OL1}	RD TERMINAL	I _{OL1} =100μA	0	-	0.5	V
	V _{OH1}		I _{OH1} =-100μA	4.5	-	5.0	
Output Voltage 2	V _{OL2}	RST/CLK0 TERMINAL	I _{OL2} =100μA	0	-	0.5	V
	V _{OH2}		I _{OH2} =-5μA	4.25	4.5	4.75	
Output Offset Voltage	V _{OS}	A _{OUT} TERMINAL	A _{IN} :OPEN	-	-	300	mV
BPF Output Voltage	V _{OUT}	A _{OUT} TERMINAL Sine Wave Input f _{IN} =f1 to f5	V _{IN} =200mV _{p-p}	-	26.0	-	dB 7,8,9
				3.5	-	-	V 7,8

Note 7) This specification is tested on condition of f_{CLK}=400KHz (The external clock is input to the OSC2 terminal through the capacitor for AC coupling).

Note 8) Each input frequency of f1 to f5 is referred to the table of the " VERSION LINEUP AND PEAK FREQUENCY ".

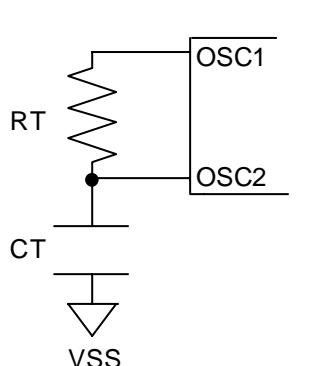
Note 9) This specification is calculated from " V_{OUT} / V_{IN} ".

■ AC CHARACTERISTICS

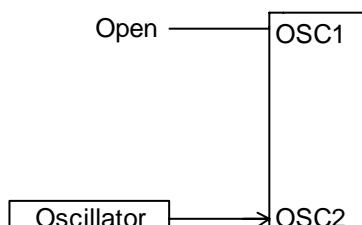
($V_{DD}=4.5$ to $6.0V$, $V_{SS}=0V$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Oscillation Clock Freq	f_{osc}	RST/CLK0 Terminal	$V_{DD}=5V$	360	400	440	KHz	10
External Clock Frequency	f_{CLK}	RST/CLK0 Terminal	$V_{ILC}=0V$ $V_{IHC}=V_{DD}$		400	800	KHz	11
RD Pulse Width	t_{PWRD}	RD Terminal	Master		$8/f_{osc}$		μs	12
			Slave		$12/f_{osc}$	c		
\overline{RST} Pulse Width	t_{PWRS}	$\overline{RST}/CLK0$ Terminal	Master	$4/f_{osc}$			μs	13
			Slave	$6/f_{osc}$				
\overline{RST} Rise/Fall Time	tr, tf	$\overline{RST}/CLK0$ Terminal				100	nA	13

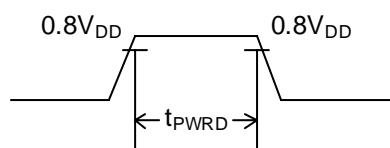
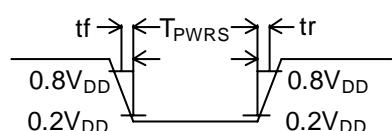
Note 10) The example for the CR Oscillation

RT: $13K\Omega(\pm 2\%)$
CT: $220pF(\pm 5\%)$ *The oscillation clock frequency is calculated from the output frequency of the $\overline{RST}/CLK0$ terminal by 3/2.

Note 11) The example for the external clock input

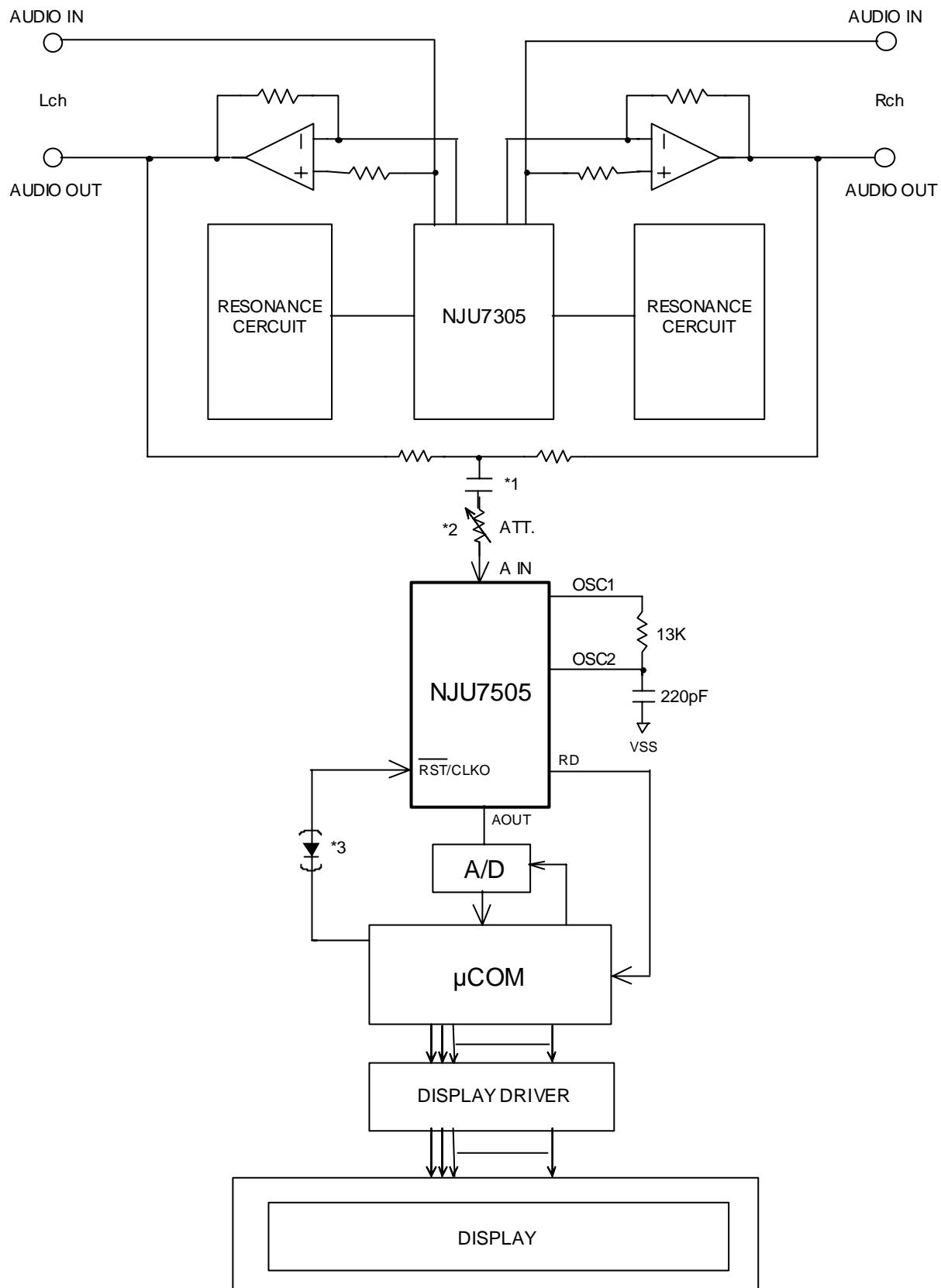
The input signal for the OSC2 terminal should be the condition of the pulse of DUTY $50\% \pm 10\%$.* The oscillation clock frequency is calculated from the output frequency of the $\overline{RST}/CLK0$ terminal by 3/2.

Note 12) The output wave form of the RD terminal.

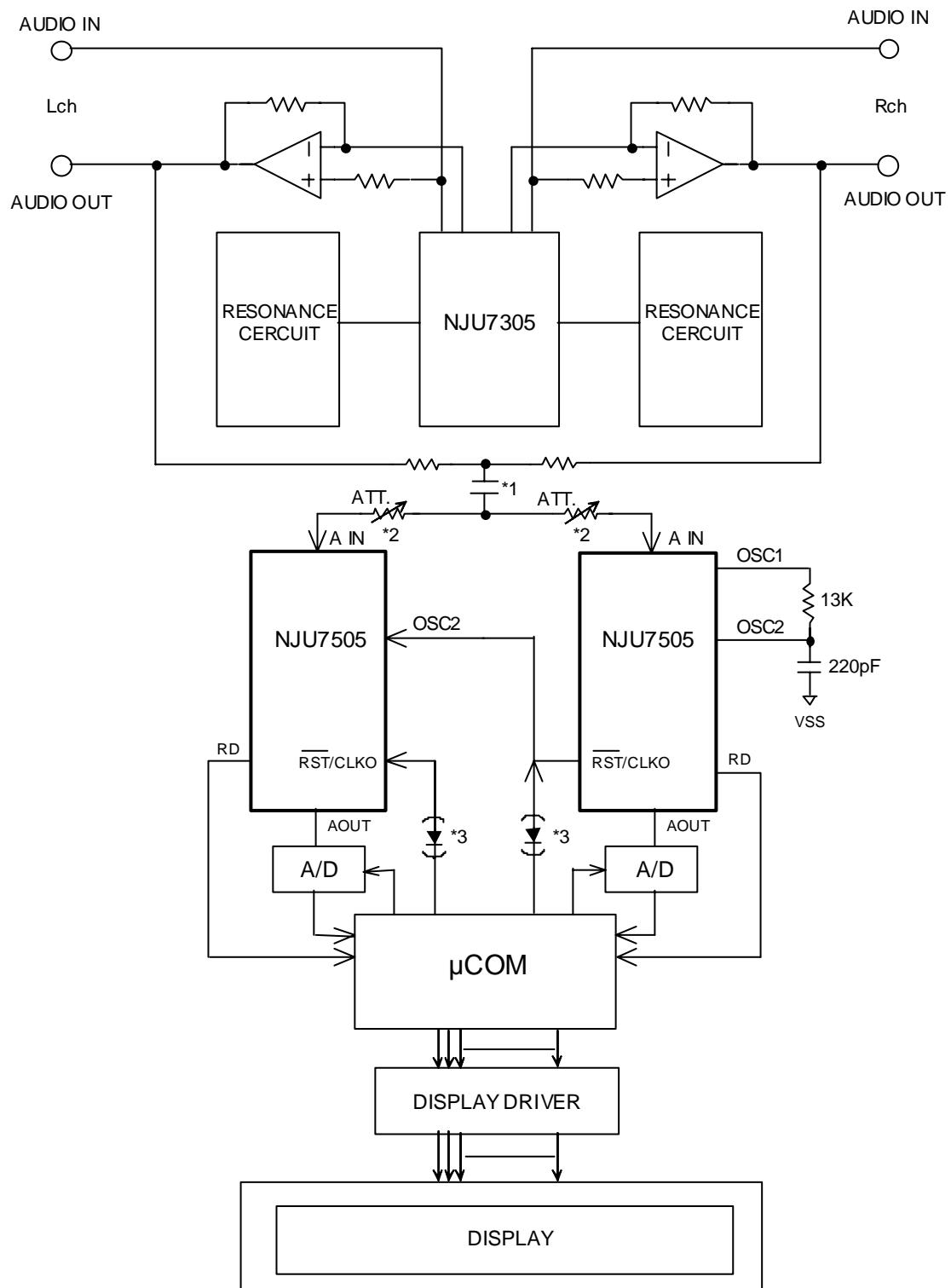
Note 13) The input wave form of the \overline{RST} terminal.

NJU7505

■ APPLICATION CIRCUIT (1)



■ APPLICATION CIRCUIT (2)



[CAUTION]
 The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights