T-50-09

M2100

ECL PROGRAMABLE CRYSTAL CONTROLLED OSCILLATORS 100 MHz to 160 MHz

M F Model 2100 Crystal Controlled Programable Oscillators is an oscillator with crystal-stability programmed by user-software to generate any frequency from 100 MHz to 160 MHz in steps as small as 4 KHz (16 bits). This effectively provides any frequency from 100 MHz to 160 MHz at tolerance of typically ±60 ppm over 0 to 85 deg. C. In addition, the frequency may be changed at any time during power-on by the user.

The frequency is selected by once inputing vectors to three registers in the M2100, and is unchanged as long as power is on. The frequency may be changed at any time during power-on, by inputting new vectors and the transition is smooth with minimal overshoot.

Uses

To replace several oscillators when only one frequency is required at a time

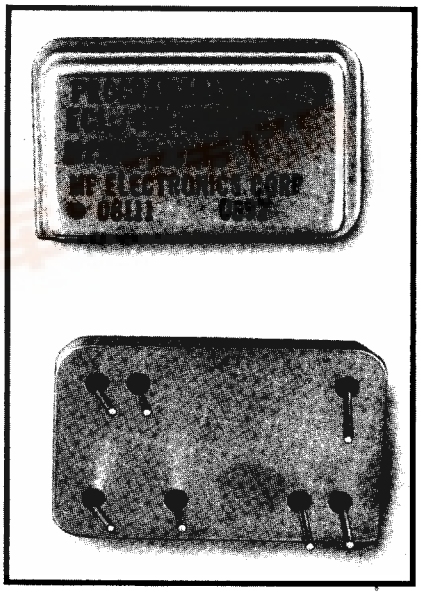
To reduce inventory requirements, since one M2100 can be used for different boards requiring different frequencies

To optimize the frequency for a system after it is assembled, instead of requiring experiments and analysis before the system is built, reducing time-to-market

To lower the clock frequency under software control for use with ATE

Highlights

- Any frequency programable from 100 MHz to 160 MHz within ±20 ppm (16 bits)
- Frequency is programmed with processor using only three inputs
- New frequency output in less than 5ms after data input
- Start frequency at power-up is free running from 80 to 120 MHz
- Operating temperature to 85 deg. C, to allow for additional heat rise in confined space
- Exceptionally low jitter
- 1000 ohm internal terminating resistor
- Data Output for Data Input verification



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Oscillator Specifications

Temperature

Operating	0 to 85 deg. C
Storage	-55 to +125 deg. C

Output Frequency Range: 100 MHz to 160 MHz

Internal Crystal Frequency: 10 MHz

	Min.	Typ.	Max.	Units
Initial Reference Crystal Accuracy		±20	±40	ppm
Crystal Accuracy, Total, all cond.		±40	±80	ppm
Allowable Freq. Step	4.0	5.0	6.25	KHz
DC Supply Voltage, VDD	4.75	5.0	5.25	Volts
Device DC Supply Current		35	70	ma
ECL Output Levels (5V input)				
"0" Level				
25 deg. C	3.20		3.43	Volts
85 deg. C	3.22		3.48	Volts
"1" Level				
25 deg. C	4.04		4.26	Volts
85 deg. C	4.11		4.36	Volts
Rise and Fall Times (20% to 80%)		1.0	2.0	ns
Symmetry, at (V_{DD} - 1.3) volts			45/55	%

Load: 370 ohms to ground (since 1K is internal), or equivalent Thevenin Load of 50 ohms to (V_{DD}-2) volts

Connections

Pin

1. Data input for programming
2. Enable input for programming
5. Clock input for programming
7. Electrical ground
8. Output - 50 ohms to (V_{DD}-2) volts, or 370 ohms to ground or equivalent Thevenin load
9. Data Out
14. V_{DD}, +5 Volts

Case Tied to pin 7

NOTE - PINS 1, 2 AND 5 ARE CMOS INPUTS AND MUST ALWAYS BE TIED TO A LOGIC LEVEL

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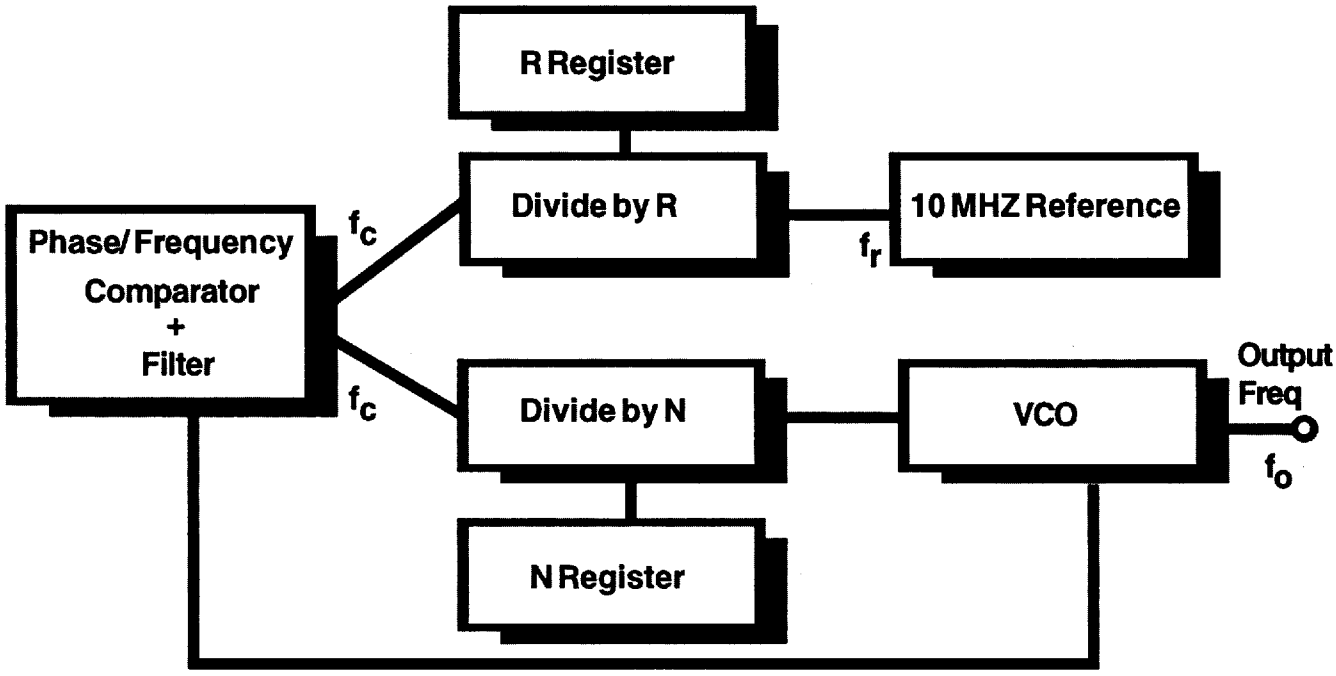
Method of Operation

The M2100 contains an internal 10 MHz crystal used as reference frequency in a synthesizer configuration.

The 10 MHz reference is divided by R with a resolution of 15 bits, to a comparison frequency, fc. It is compared to a frequency which is the Output Frequency, fo, divided by N. The Output Frequency is obtained from a VCO. The Frequency Detector, which compares the frequencies, and the filter, produce a DC voltage used to correct the VCO output frequency, until it matches N-times the comparison frequency. A lock is then produced so that the Output Frequency equals the Reference Frequency times N/R.



Output Frequency, $f_0 = f_r \bullet (N/R)$

For correct operation, R must be any integer between 2500 and 1600, resulting in the comparison frequencies fc, of 4.0 and 6.25 KHz respectively.

Likewise, for correct operation, N must be an integer which when multiplied by the comparison frequency will yield an output frequency between 100 and 160 MHz.

For example, if the f_c is 4 KHz, N should be between 25,000 and 40,000. which results in an output frequency of 100 MHz and 160 MHz respectively.

If f_c is 6.25 MHz, N should be between 16,000 and 25,600.

Controlling the Frequency

The values of N and R are controlled by input to the N and R register. In addition, a third register, C, must also be set. Once the three registers are set, the desired frequency will appear.

The registers may be set in any order, but to change frequency, it is only necessary to change either or both the R and N registers.

Description of the Registers

1) The Control (C) register requires one pre-defined byte (8 bits) required for the internal operation.

2) The Reference (R) register requires the user's choice of either 15 bits, or 3 bytes (24 bits). In the event that the 3 bytes (24 bits) are used, the first 9 bits are "don't care"

3) The Multiplication (N) register requires two bytes (16 bits).

Loading the Registers

Loading the registers is done one at a time, in any sequence. To load any register, three simultaneous inputs are required Data, Clock and Enable:

1. The Data bits, which is the number being entered into the register (in binary).

2. The Clock bits are time-related, and clock the Data bits and may be any frequency to 4 MHz.

3. The Enable signal which encompasses the Clock and Data signals.

It is the length of the Enable signal which "tells" the device which register is being loaded: one byte wide for the C register, two bytes wide for the N register, and three bytes (or 15 bits) wide for the R register.

The Data are input into the registers serially in binary, with the Most Significant Bit (MSB) first. At the same time, a Clock signal is input to the Clock pin. The Data is written to the register on the rising edge of the Clock. At the same time, an active-low Enable is applied to the ENABLE pin and it is the length of the ENABLE which determines the register which is being addressed. Data is retained in the registers over a supply range of 2.5 to 6 V, but the operation of the device is guaranteed from 4.75 to 5.25 volts.

A summary of the Data In bits is:
(MSBs are shifted in first. C0, N0 and R0 are the LSB's)

TABLE I

LENGTH OF ENABLE IN NO. OF CLOCKS	ACCESSED REGISTER	BIT NOMENCLATURE
8	C Register	C7,C6,C5...,C0
16	N Register	N15,N14,N13,.,N0
15 or 24	R Register	R14,R13,R12,.,R0

Pin Functions

Pin 1. The Data In is serial beginning with the MSB and is shifted in on the low-to-high transition of the Clock. The bit pattern is 1 byte (8 bits) long to access the C register, 2 bytes (16 bits) to access the N register, or 3 bytyes (24 bits) to access the R or reference register. Optionally, the R register can be accessed with a 15-bit transfer. The values of C, N and R registers do not change during shifting because the transfer of data to the registers is controlled by Enable.

The bit stream may be used by any of the registers, and the register to which the data goes is determined by the number of clocks and the length of the Enable. The Data In corresponds to the binary values desired for R and N.

The C register always requires the same format value of 64 in binary.

Data Intypically switches near 50% of Vdd to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. .

Pin 2. The Enable Input is used to identify and transfer the Data of Pin 1, to the desired register, C, N or R. To transfer data, Enable (which must start inactive high) is taken low. During the low state, the serial transfer is made via Data In and Clock occurs, and Enable is taken back high. The low-to-high transition on Enable transfers data to the C, N or R register, depending on the data stream length per Table 1. The switching characteristic is the same as Data In. Transitions on Enable should not be made when Clock is high.

Pin 5. The Serial Data Clock input. Low-to-high transitions on Clock shift bits available at Data in, while high-to-low transitions shift bits from Data Out. Eight clock cycls are required to access the C register, sixteen for the N register and either 15 or 24 may be used to access the R register. Clock pulses may be any frequency to 4 MHz. The switching characteristic is the same as Data In.

Pin 9. The Tristate Serial Data Output is used to verify Data In. Data Out could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be used to test integrity of the system's processor, or could be monitored at an inline QA test during board manufacture, or could be used to trouble-shoot a system.

Input Pin Requirements (Pins 1, 2, 5 and 9)

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Maximum Low Level Input Voltage	1.3			Volts
V_{IH}	Minimum High Level Input Voltage		3.1	5.5	Volts
f_{clk}	Serial Data Clock Frequency	DC		4.0	MHz
C_{in}	Maximum Input Capacitance			15	pf

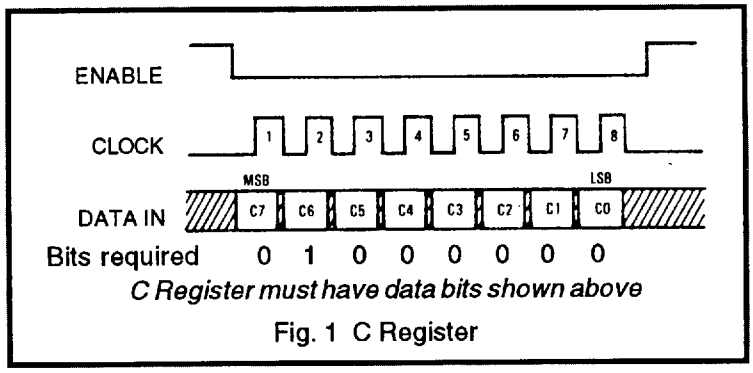


Fig. 1 C Register

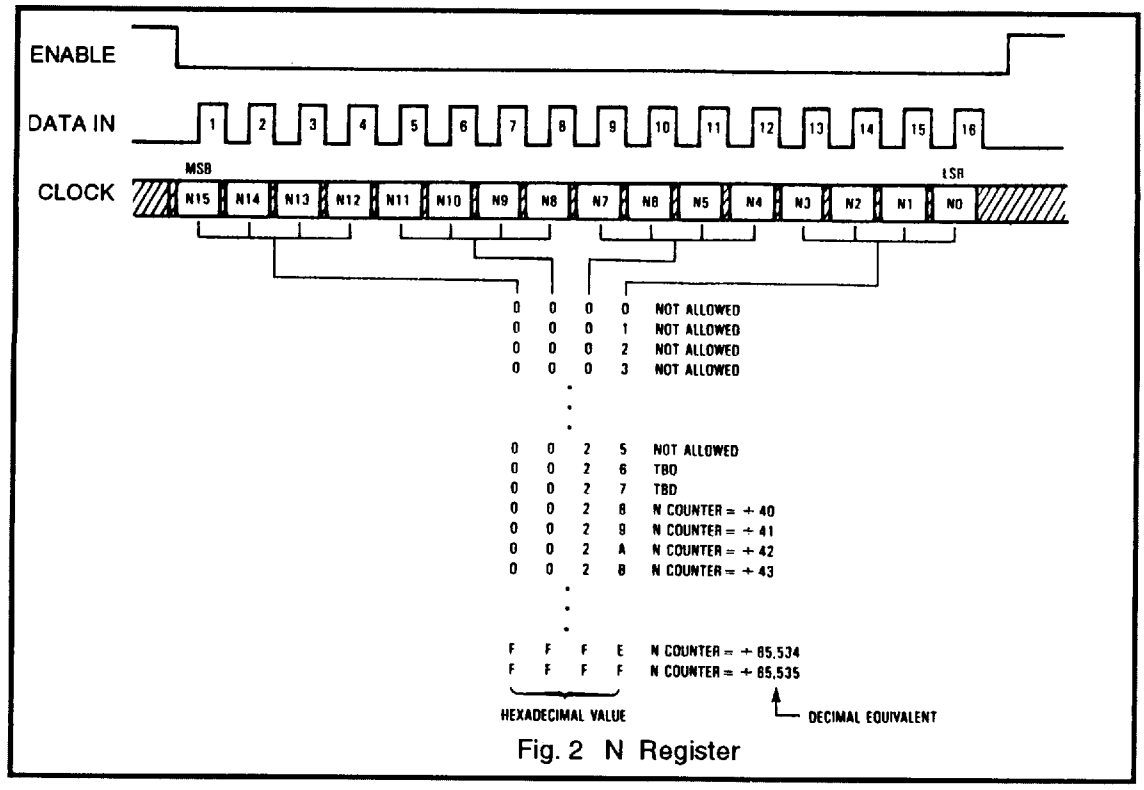


Fig. 2 N Register

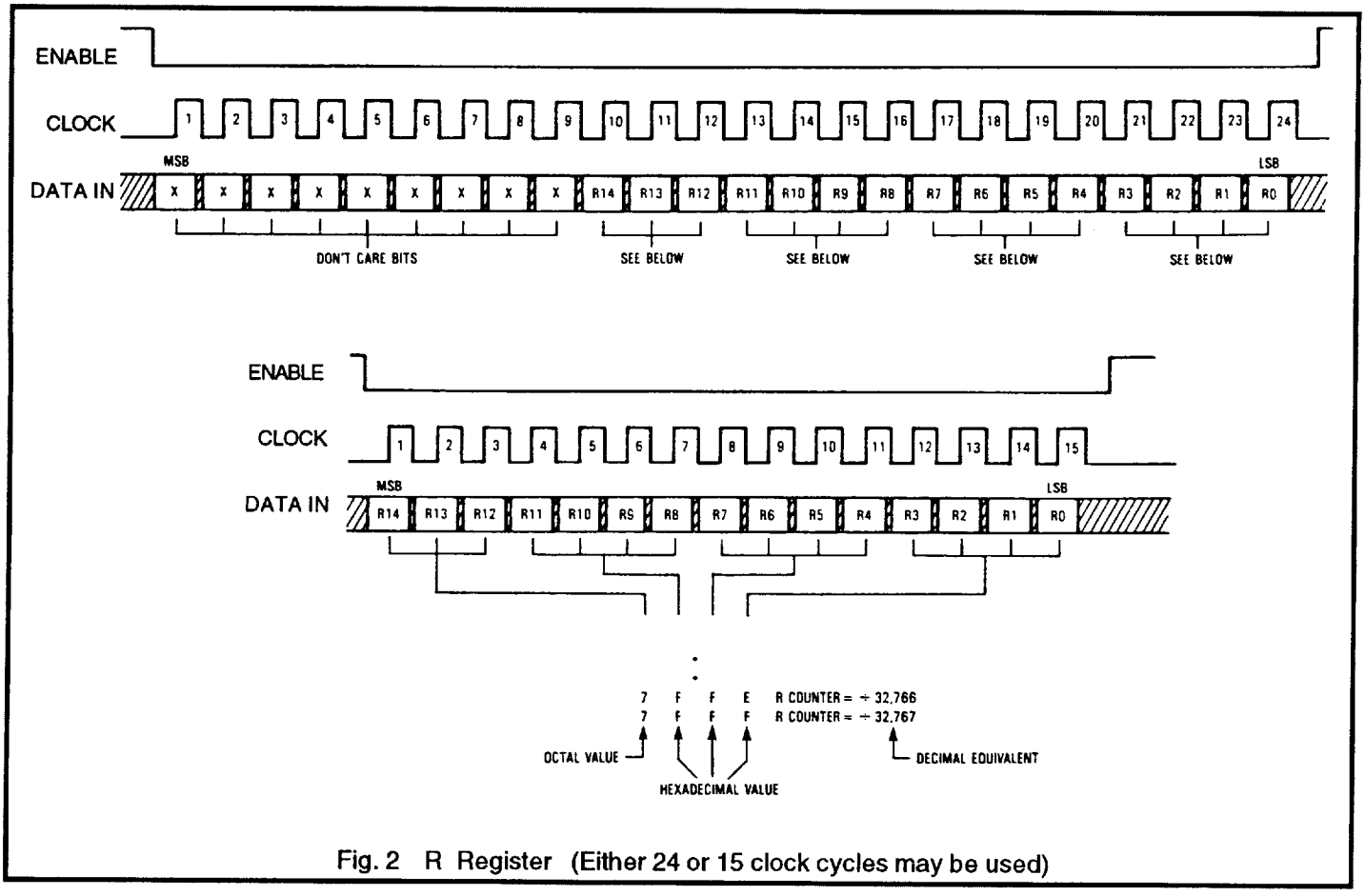


Fig. 2 R Register (Either 24 or 15 clock cycles may be used)

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Timing Requirements

(Input $t_r = t_s = 10$ns otherwise indicated)

Symbol	Parameter	Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times for Data In versus Clock	40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times for Enable versus Clock	100	ns
$t_{w(H)}$	Minimum Inactive High Pulse Width for Enable	300	ns
t_r, t_f	Maximum Input Rise and Fall Times for Clock Enable	100	microsec

Switching Waveforms

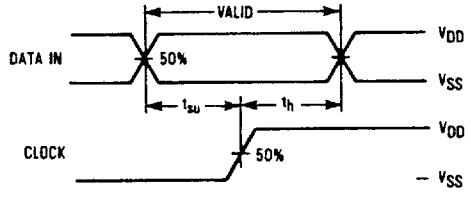

Figure 4

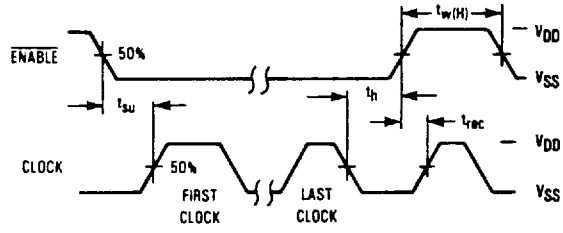

Figure 5

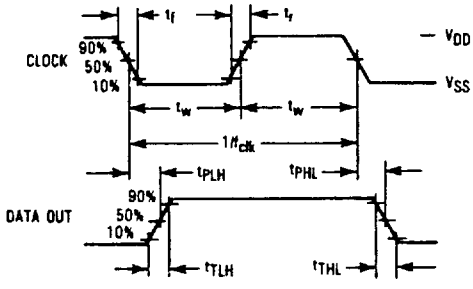

Figure 6

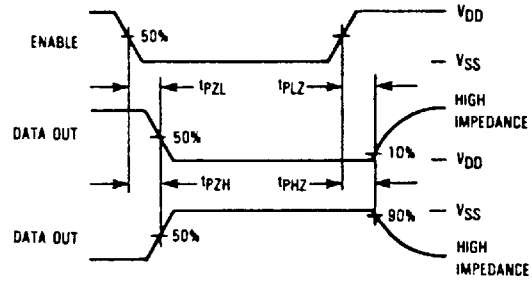

Figure 7

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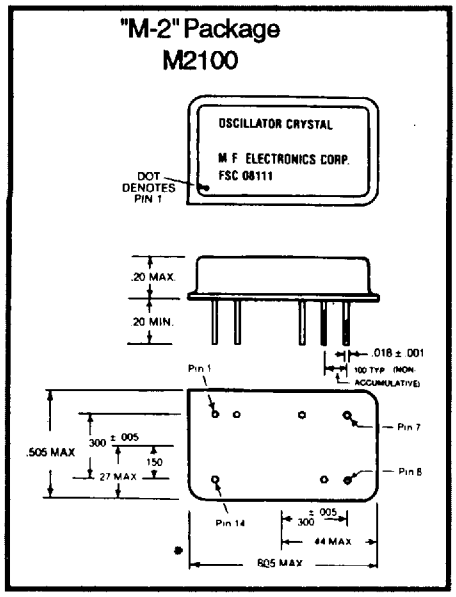

Mechanical Specifications

Gross Leak	Each unit checked at 85°C
Fine Leak	Mass spectrometer leak rate less than 2 x 108 atmos, cc/sec of helium.
Pins	Alloy 52. nickel plated with 60/40 solder coat
Bend Test	Will withstand two bends of 90° from reference
Header	Steel, with nickel plate
Case	Stainless steel, type 304, 18% chromium
Marking	Printing is black epoxy ink
Resistance to Solvents	MIL STD 202 Method 215

Enviromnental Specifications

Temperature Cycle	Not to exceed +5 ppm change when exposed to 2 hours maximum at each temperature from 0 to 120° C., with 25°C. reference.
Shock	1000 G's, 0.35 ms, 1/2 sine wave, 3 shocks in each plane
Vibration	10-2000 Hz of .06" d.a. or 20 G's, whichever is less
Humidity	Resistant to 85% R.H. at 85° C.

To Order:

Specify Part No. M2100 - 160 MHz.

Examples

1. It is desired to generate 107.352 MHz. The internal reference frequency is 10 MHz, and we may choose any comparison frequency, fc, from 4.0 to 6.25 KHz. Arbitrarily, we choose 4.0 KHz. Therefore, the R register must be 10 MHz divided by 4 KHz, or 2,500. Converting to binary, this is "9C4" in hexadecimal, or 000100111000100 (15 bits). The M register must be 107.352 MHz divided by 4 KHz, or 26,838, which becomes 0110100011010110 (16 bits) in binary.

2. It is desired to test a system which runs at 130 MHz. In order to do the test, it has been determined that the system should be tested at +/-5% of the nominal frequency. These frequencies are 123.5 and 136.5 MHz. For both (or either frequency), the comparison frequency could be 5 KHz, resulting in a value for the R register of 10 MHz divided by 5 KHz, or 2,000. For 123.5 MHz, the M register must be 123.5 MHz divided by 5 KHz or 24,700. For 136.5 MHz, the required value for the M register becomes 27,300. Either of the three frequencies is loaded by addressing the registers; when a new value of M is input (with the appropriate Clock and Enable), the frequency is changed as desired.

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