Burr-Brown Products from Texas Instruments

ADS5275 ADS5276 ADS5277

SBAS300 − JANUARY 2004

8-Channel, 10-Bit, 40/50/65MSPS ADC with Serialized LVDS Interface

FEATURES

- **Maximum Sample Rate: 40MSPS (ADS5275), 50MSPS (ADS5276), and 65MSPS (ADS5277)**
- **10-Bit Resolution**
- **No Missing Codes**
- **Power Dissipation: 768mW (ADS5275), 816mW (ADS5276), and 872mW (ADS5277)**
- **CMOS Technology**
- **Simultaneous Sample-and-Hold**
- **60.5dB SNR at 10MHz IF**
- **Serialized LVDS Outputs Meet or Exceed Requirements of ANSI TIA/EIA-644-A Standard**
- **Internal and External References**
- **3.3V Digital/Analog Supply**
- **TQFP-80 PowerPAD™ Package**

APPLICATIONS

- **Portable Ultrasound Systems**
- **Tape Drives**
- **Test Equipment**

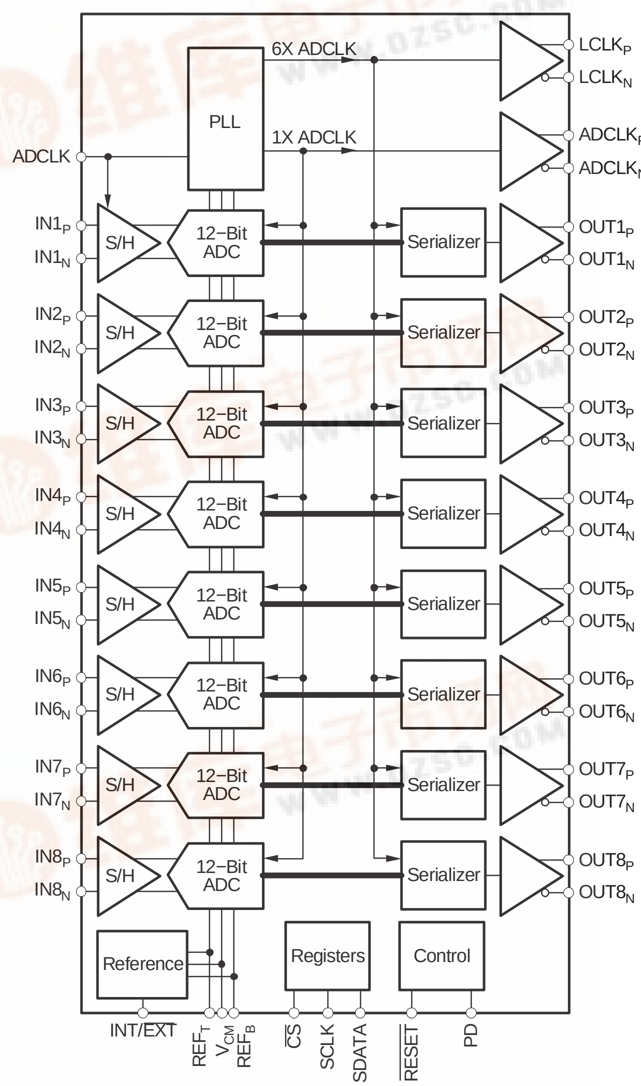
DESCRIPTION

The ADS527x are high-performance, 40MSPS, 50MSPS, and 65MSPS, 8-channel, parallel analog-to-digital converters (ADCs). Internal references are provided, simplifying system design requirements. Low power consumption allows for the highest of system integration densities. Serial LVDS (low-voltage differential signaling) outputs reduce the number of interface lines and package size.

In LVDS, an integrated phase lock loop multiplies the incoming ADC sampling clock by a factor of 6. This high-frequency LVDS clock is used in the data serialization and transmission process and is converted to an LVDS signal for transmission in parallel with the data. Providing this additional LVDS clock allows for easy delay matching. The word output of each internal ADC is serialized and transmitted either MSB or LSB first. The bit following the rising edge of the ADC clock output is the first bit of the word.

The ADS527x provide internal references, or can optionally be driven with external references. Best performance can be achieved through the internal reference mode.

The ADS527x are available in a PowerPAD TQFP-80 package and are specified over a −40°C to +85°C operating range.



PRODUCT PREVIEW

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage Range, AVDD	−0.3V to 3.8V
Supply Voltage Range, LVDD	−0.3V to 3.8V
Voltage Between AVSS and LVSS	−0.3V to 0.3V
Voltage Between AVDD and LVDD	−0.3V to 0.3V
Voltages Applied to External REF Pins	−0.3V to 2.4V
All LVDS Data and Clock Outputs	−0.3V to 2.4V
ADCLK Peak Input Current	TBD
Peak Total Input Current (all inputs)	−30mA
Operating Free-Air Temperature Range, T_A	−40°C to 85°C
Lead Temperature 1.6mm (1/16″ from case for 10s)	235°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5275	HTQFP-80	PFP	−40°C to +85°C	ADS5275IPFP	ADS5275IPFP	Tray, 96
″	″	″	″	″	ADS5275IPFPT	Tape and Reel, 250
ADS5276	HTQFP-80	PFP	−40°C to +85°C	ADS5276IPFP	ADS5276IPFP	Tray, 96
″	″	″	″	″	ADS5276IPFPT	Tape and Reel, 250
ADS5277	HTQFP-80	PFP	−40°C to +85°C	ADS5277IPFP	ADS5277IPFP	Tray, 96
″	″	″	″	″	ADS5277IPFPT	Tape and Reel, 250

(1) For the most current specification and package information, refer to our web site at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

	ADS5275			ADS5276			ADS5277			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
SUPPLIES AND REFERENCES										
Analog Supply Voltage, AVDD	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
Output Driver Supply Voltage, LVDD	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
CLOCK INPUT AND OUTPUTS										
ADCLK Input Sample Rate (low-voltage TTL), $1/t_C$	20		40	20		50	20		65	MSPS
Low Voltage Level Clock			1			1			1	V
High Voltage Level Clock			2			2			2	V
$ADCLK_P$ and $ADCLK_N$ Outputs (LVDS)	20		40	25		50	32.5		65	MHz
$LCLK_P$ and $LCLK_N$ Outputs (LVDS)(1)	120		240	120		300	120		390	MHz
Operating Free-Air Temperature, T_A	−40		+85	−40		+85	−40		+85	°C

(1) 6 × ADCLK.

REFERENCE SELECTION

MODE	INT/$\overline{\text{EXT}}$	
$2.0V_{PP}$ Internal Reference	1	Default with internal pull-up.
External Reference	0	Internal reference is powered down. Common mode of external reference should be within 50mV of V_{CM}. V_{CM} is derived from the internal bandgap voltage.

ELECTRICAL CHARACTERISTICS

T_{MIN} = −40°C, T_{MAX} = +85°C. Typical values are at T_A = 25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, −0.5dBFS, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS5275			ADS5276			ADS5277			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY												
	No Missing Codes			Assured			Assured			Assured		
DNL	Differential Nonlinearity		TBD	0.5	TBD	TBD	0.5	TBD	TBD	0.5	TBD	LSB
INL	Integral Nonlinearity		TBD	1	TBD	TBD	1	TBD	TBD	1	TBD	LSB
	Midscale Offset Error(1)		TBD		TBD	TBD		TBD	TBD		TBD	mV
	Offset Temperature Coefficient			TBD			TBD			TBD		ppm/°C
	Fixed Gain Error(2)		TBD	1.5	TBD	TBD	1.5	TBD	TBD	1.5	TBD	%FS
	Gain Temperature Coefficient			TBD			TBD			TBD		Δ%/°C
POWER SUPPLY												
I_{CC}	Total Supply Current	V_{IN} = FS, F_{IN} = 10MHz		233			247			264		mA
I(AVDD)	Analog Supply Current	V_{IN} = FS, F_{IN} = 10MHz										mA
I(LVDD)	Digital Output Driver Supply Current	V_{IN} = FS, F_{IN} = 10MHz, LVDS Into 100Ω Load										mA
	Power Dissipation			768			816			872		mW
REFERENCE VOLTAGES												
$VREF_T$	Reference Top (internal)			2.0			2.0			2.0		V
$VREF_B$	Reference Bottom (internal)			1.0			1.0			1.0		V
V_{CM}	Common-Mode Voltage			1.5			1.5			1.5		V
	V_{CM} Output Current			TBD			TBD			TBD		mA
$VREF_T$	Reference Top (external)		1.875			1.875			1.875			V
$VREF_B$	Reference Bottom (external)				1.125			1.125			1.125	V
	Reference Input Resistance(3)			TBD			TBD			TBD		Ω
ANALOG INPUT												
DC	Differential Input Resistance			1.2			1.2			1.2		kΩ
	Differential Input Capacitance			7			7			7		pF
	Analog Input Common-Mode Range			V_{CM} ± 0.05			V_{CM} ± 0.05			V_{CM} ± 0.05		V
	Differential Input Voltage Range		1.5		2.0	1.5		2.0	1.5		2.0	V_{PP}
	Voltage Overload Recovery Time	Differential Input Signal at $4V_{PP}$ Recovery to Within 1% of Code		4			4			4		CLK Cycles
	Input Bandwidth			300			300			300		MHz
DIGITAL DATA OUTPUTS												
	Data Bit Rate		240		480	300		600	390		780	MBPS
SERIAL INTERFACE												
SCLK	Serial Clock Input Frequency				20		20			20		MHz
V_{IN} LOW	Input Low Voltage		0		0.6	0		0.6	0		0.6	V
V_{IN} HIGH	Input High Voltage		2.1		VDD	2.1		VDD	2.1		VDD	V
	Input Current			TBD			TBD			TBD		μA
	Input Pin Capacitance			5			5			5		pF

(1) Offset Error is the measured deviation of the midscale transition from the ideal midscale transition.
(2) Gain Error is the difference between the nominal and actual offset point on the transfer function after the offset error has been corrected to zero. The gain point is the mid-step value when the digital output is full-scale.
(3) Average switching current drawn from external reference. DC component of current is internally generated even in external reference mode.

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AC CHARACTERISTICS

T_{MIN} = −40°C, T_{MAX} = +85°C. Typical values are at T_A = 25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, −0.5dBFS, internal voltage reference, and $2V_{PP}$ differential input, unless otherwise noted.

PARAMETER		CONDITIONS	ADS5275			ADS5276			ADS5277			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS												
SFDR	Spurious-Free Dynamic Range	f_{IN} = 1MHz		80			80			80		dBc
		f_{IN} = 5MHz	TBD	80		TBD	80		TBD	80		dBc
		f_{IN} = 10MHz		80			80			80		dBc
		f_{IN} = 20MHz		80			80			80		dBc
HD_2	2nd-Order Harmonic Distortion	f_{IN} = 1MHz		85			85			82		dBc
		f_{IN} = 5MHz	TBD	85		TBD	85		TBD	82		dBc
		f_{IN} = 10MHz		85			85			TBD		dBc
		f_{IN} = 20MHz		85			82			TBD		dBc
HD_3	3rd-Order Harmonic Distortion	f_{IN} = 1MHz		80			80			77		dBc
		f_{IN} = 5MHz	TBD	80		TBD	80		TBD	77		dBc
		f_{IN} = 10MHz		80			80			TBD		dBc
		f_{IN} = 20MHz		80			79			TBD		dBc
SNR	Signal-to-Noise Ratio	f_{IN} = 1MHz		60.5			60.5			60.5		dBFS
		f_{IN} = 5MHz	TBD	60.5		TBD	60.5		TBD	60.5		dBFS
		f_{IN} = 10MHz		60.5			60.5			60.5		dBFS
		f_{IN} = 20MHz		60.5			60.5			60.5		dBFS
SINAD	Signal-to-Noise and Distortion	f_{IN} = 1MHz		60			60			60		dBFS
		f_{IN} = 5MHz	TBD	60		TBD	60		TBD	60		dBFS
		f_{IN} = 10MHz		60			60			60		dBFS
		f_{IN} = 20MHz		60			60			59		dBFS
ENOB	Effective Number of Bits	f_{IN} = 10MHz		9.7			9.7			9.7		Bits
Crosstalk		Signal Applied to 7 Channels, Measurement Taken on the Channel with No Input Signal		−85			−85			−85		dBc

LVDS DIGITAL DATA AND CLOCK OUTPUTS

Test conditions at I_O = 3.5mA, R_{LOAD} = 100Ω, and C_{LOAD} = 9pF. All LVDS specifications are characterized but not tested.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DC SPECIFICATIONS						
V_{OH}	Output Voltage High, OUT_P or OUT_N	R_{LOAD} = 100Ω ± 1%; See LVDS Diagram, Page 7		1340	1475	mV
V_{OL}	Output Voltage Low, OUT_P or OUT_N	R_{LOAD} = 100Ω ± 1%	925	1038		mV
$\|V_{OD}\|$	Output Differential Voltage	R_{LOAD} = 100Ω ± 1%	325	350	375	mV
V_{OS}	Output Offset Voltage	R_{LOAD} = 100Ω ± 1%; See LVDS Diagram, Page 7	1.125	1.250	1.275	V
R_O	Output Impedance, Single-Ended	V_{CM} = 1.0V and 1.4V		TBD		Ω
ΔR_O	Mismatch Between OUT_N and OUT_P	V_{CM} = 1.0V and 1.4V			TBD	%
C_O	Output Capacitance	V_{CM} = 1.0V and 1.4V	3	4	5	pF
$\|\Delta V_{OD}\|$	Change in $\|V_{OD}\|$ Between 0 and 1	R_{LOAD} = 100Ω ± 1%			25	mV
ΔV_{OS}	Change Between 0 and 1	R_{LOAD} = 100Ω ± 1%			25	mV
$ISOUT_P$, $ISOUT_N$	Output Short-Circuit Current	Drivers Shorted to Ground			40	mA
$ISOUT_{NP}$	Output Current	Drivers Shorted Together			12	mA
$\|I_{XN}\|$, $\|I_{XP}\|$	Power-Off Output Leakage	V_{CC} = 0V			10	mA
DRIVER AC SPECIFICATIONS						
Clock	Clock Signal Duty Cycle	6 × ADCLK	45	50	55	%
t_{SKEW1}	$\|tp_{HLP} - tp_{LHN}\|$ or $\|tp_{HLN} - tp_{LHP}\|$, Differential Skew	Any Differential Pair on Package(1)			50	ps
t_{SKEW2}	$\|tp_{DIFF[X]} - tp_{DIFF[Y]}\|$, Channel-to-Channel Skew(3)	Any Two Signals on Package(2)			100	ps
t_{RISE}/t_{FALL}	V_{OD} Rise Time or V_{OD} Fall Time	Z_{LOAD} = 100Ω, C_I = 9pF, I_O = 2.5mA		400		
		Z_{LOAD} = 100Ω, C_I = 9pF, I_O = 3.5mA		250		ps
		Z_{LOAD} = 100Ω, C_I = 9pF, I_O = 4.5mA		200		ps
		Z_{LOAD} = 100Ω, C_I = 9pF, I_O = 6mA		150		ps

(1) Skew measurements are made at the 50% point of the transition.
(2) Skew measurements made at 0V differential (that is, the crossing of single-ended signals).
(3) Where x is any one of the parallel channels and y is any other channel.

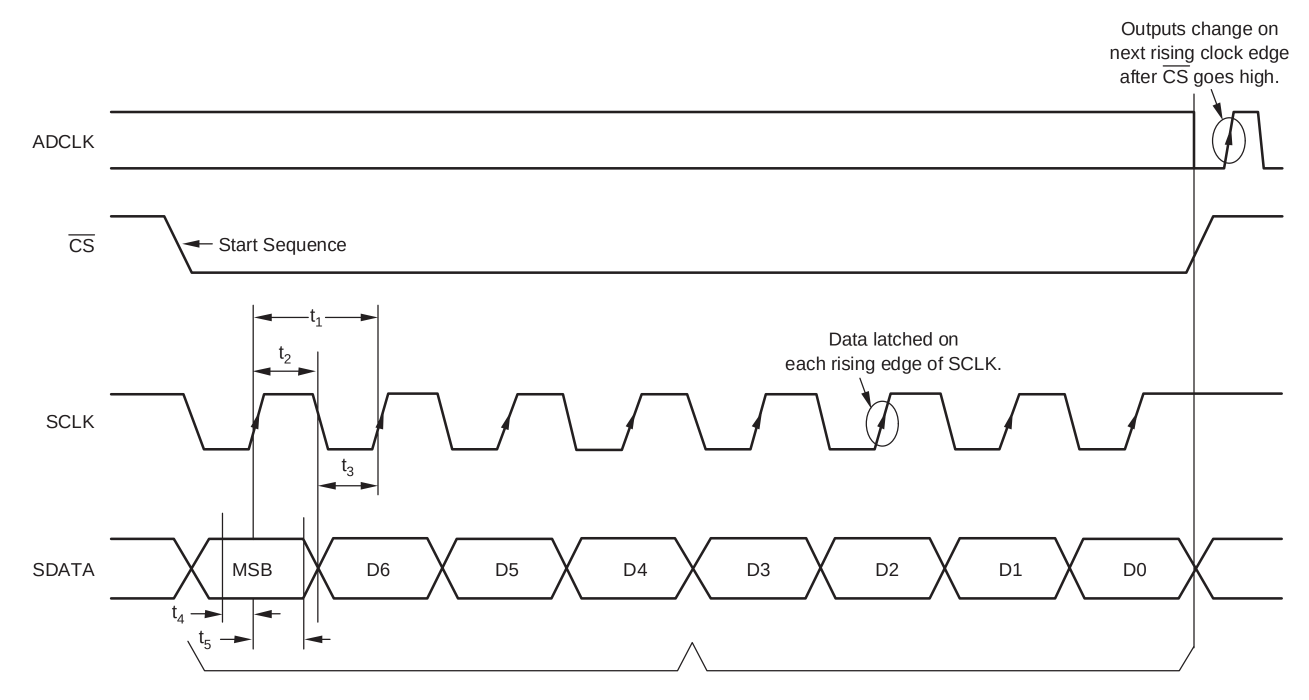
SWITCHING CHARACTERISTICS

T_{MIN} = −40°C, T_{MAX} = +85°C. Typical values are at T_A = 25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, −0.5dBFS, internal voltage reference, and $2V_{PP}$ differential input, unless otherwise noted.

PARAMETER		CONDITIONS	ADS5275			ADS5276			ADS5277			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING SPECIFICATIONS												
	t_{SAMPLE}		25		50	20		50	15		50	ns
$t_D(A)$	Aperture Delay			120			120			120		ps
	Aperture Jitter (uncertainty)			1			1			1		ps
t_D(pipeline)	Latency			6.5			6.5			6.5		cycles
t_{PROP}	Propagation Delay			13			13			13		ns

SERIAL INTERFACE TIMING

Data is shifted in MSB first.



PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	Serial CLK Period	50			ns
t_2	Serial CLK High Time	13			ns
t_3	Serial CLK Low Time	13			ns
t_4	Data Setup Time	5			ns
t_5	Data Hold Time	5			ns

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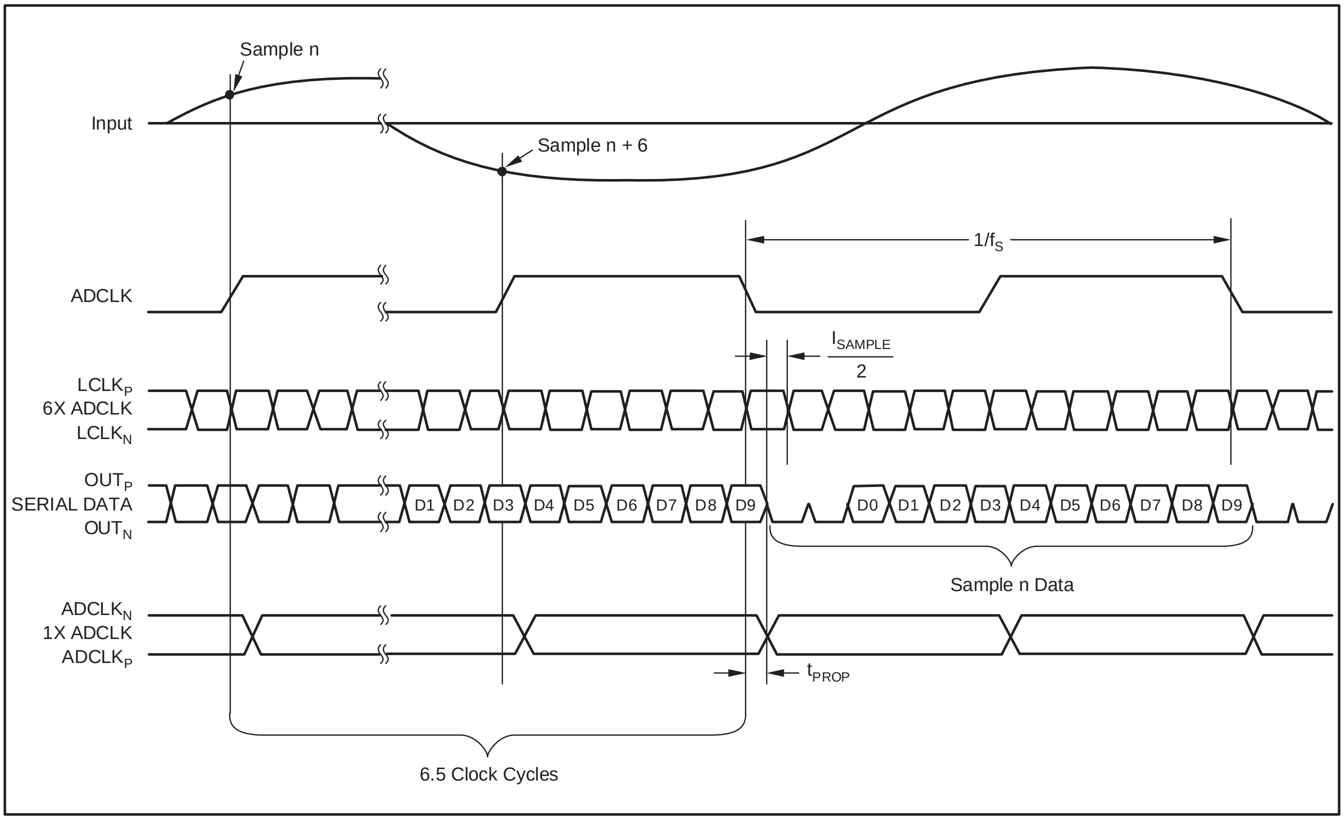
SERIAL INTERFACE TIMING

ADDRESS				DATA				DESCRIPTION	REMARKS
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
0	0	0	0					**0. LVDS BUFFERS**	Patterns Get Reversed in MSB First Mode of LVDS
				0	0			Normal ADC Output	
				0	1			Deskew Pattern	
				1	0			Sync Pattern	
				1	1			Custom Pattern	
						0	0	Output Current in LVDS = 3.5mA	
						0	1	Output Current in LVDS = 2.5mA	
						1	0	Output Current in LVDS = 4.5mA	
						1	1	Output Current in LVDS = 6.0mA	
0	0	0	1					**1. LSB/MSB MODE**	
				D3	**D2**	**D1**	**D0**		
				0	X	X	1	2X LVDS Clock Output Current	
				0	0	X	X	LSB Mode	
				0	1	X	X	MSB Mode	
0	0	1	0					**2. POWER-DOWN ADC CHANNELS**	
				D3	**D2**	**D1**	**D0**		
				X	X	X	X	Power-Down Channels 1 to 4; D3 is for Channel 4 and D0 for Channel 1	Example: 1010 Powers Down Channels 4 and 2 and Keeps Channels 1 and 3 Alive
0	0	1	1					**3. POWER-DOWN ADC CHANNELS**	
				D3	**D2**	**D1**	**D0**		
				X	X	X	X	Power-Down Channels 5 to 8; D3 is for Channel 8 and D0 for Channel 5	
								CUSTOM PATTERN (registers 4-6)	
				D3	**D2**	**D1**	**D0**		
0	1	0	0	MSB	X	X	X		
0	1	0	1	X	X	X	X	Bits for Custom Pattern	
0	1	1	0	X	X	X	LSB		

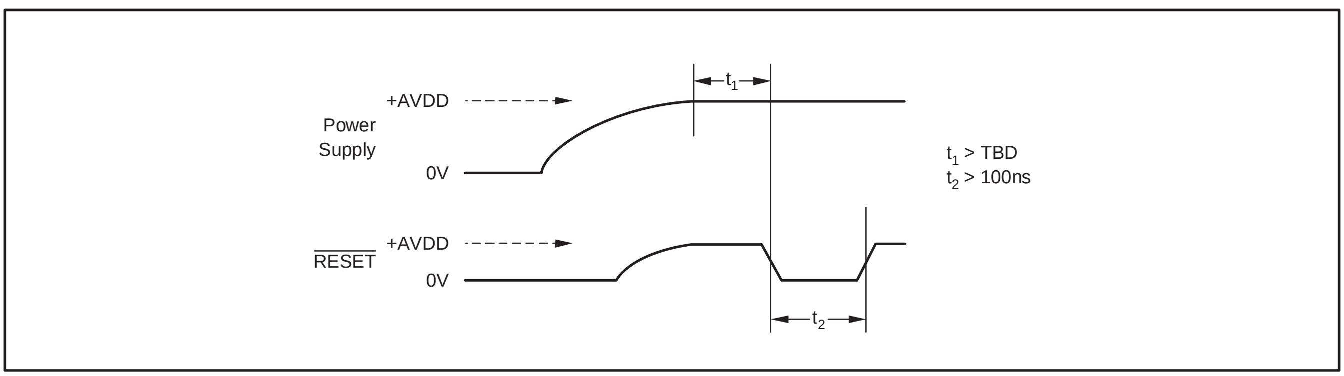
TEST PATTERNS(1)	
Deskew	101010101010
Sync	000000111111
Custom	Any 10-bit pattern that is defined in the custom pattern registers 4 to 6.

(1) Default is LSB first. If MSB is selected the above patterns will be reversed.

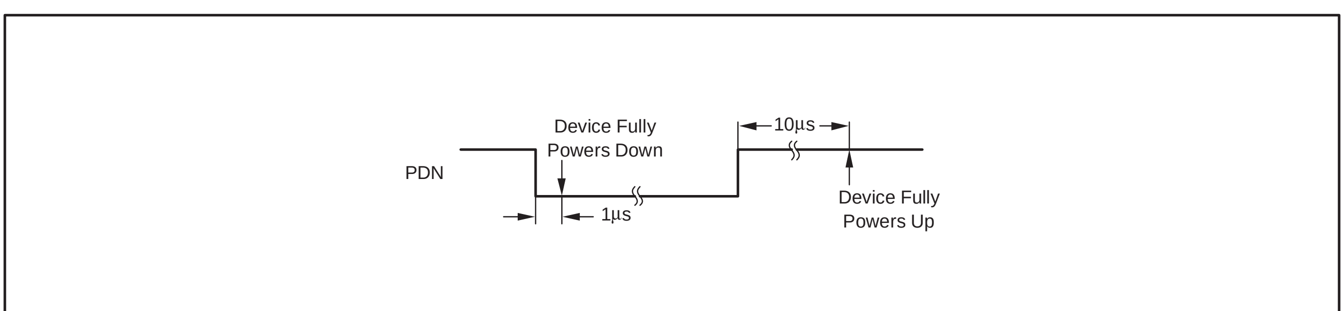
LVDS TIMING DIAGRAM (PER ADC CHANNEL)



RESET TIMING

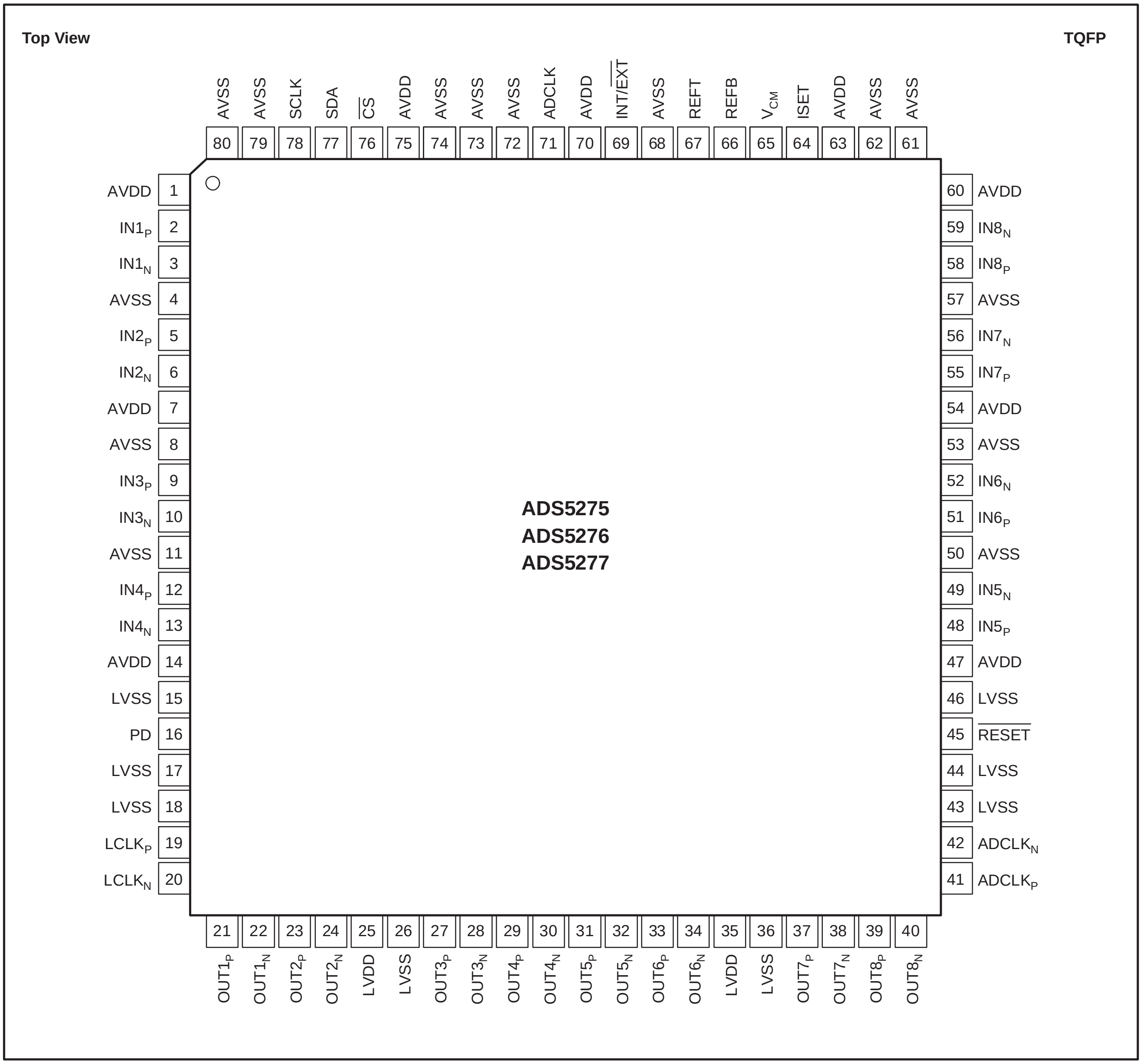


POWER-DOWN TIMING



PRODUCT PREVIEW

PIN CONFIGURATION



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PIN DESCRIPTIONS

NAME	PIN #	NUMBER OF PINS	I/O	DESCRIPTION
AVDD	1, 7, 14, 47, 54, 60, 63, 70, 75	8	I	Analog Power Supply
AVSS	4, 8, 11, 50, 53, 57, 61, 62, 68, 72-74, 79, 80	14	I	Analog Ground
LVDD	25, 35	2	I	LVDS Power Supply
LVSS	15, 17, 18, 26, 36, 43, 44, 46	8	I	LVDS Ground
$IN1_P$	2	1	I	Channel 1 Differential Analog Input High
$IN1_N$	3	1	I	Channel 1 Differential Analog Input Low
$IN2_P$	5	1	I	Channel 2 Differential Analog Input High
$IN2_N$	6	1	I	Channel 2 Differential Analog Input Low
$IN3_P$	9	1	I	Channel 3 Differential Analog Input High
$IN3_N$	10	1	I	Channel 3 Differential Analog Input Low
$IN4_P$	12	1	I	Channel 4 Differential Analog Input High
$IN4_N$	13	1	I	Channel 4 Differential Analog Input Low
$IN5_P$	48	1	I	Channel 5 Differential Analog Input High
$IN5_N$	49	1	I	Channel 5 Differential Analog Input Low
$IN6_P$	51	1	I	Channel 6 Differential Analog Input High
$IN6_N$	52	1	I	Channel 6 Differential Analog Input Low
$IN7_P$	55	1	I	Channel 7 Differential Analog Input High
$IN7_N$	56	1	I	Channel 7 Differential Analog Input Low
$IN8_P$	58	1	I	Channel 8 Differential Analog Input High
$IN8_N$	59	1	I	Channel 8 Differential Analog Input Low
REFT	67	1	I/O	Reference Top Voltage
REFB	66	1	I/O	Reference Bottom Voltage
V_{CM}	65	1	O	Common-Mode Output Voltage
INT/$\overline{EXT}$	69	1	I	Internal/External Reference Select; 0 = External, 1 = Internal
PD	16	1	I	Power-Down; 0 = Normal, 1 = Power-Down
$LCLK_P$	19	1	O	Positive LVDS Clock
$LCLK_N$	20	1	O	Negative LVDS Clock
ADCLK	71	1	I	Data Converter Clock Input
$OUT1_P$	21	1	O	Channel 1 Positive LVDS Data Output
$OUT1_N$	22	1	O	Channel 1 Negative LVDS Data Output
$OUT2_P$	23	1	O	Channel 2 Positive LVDS Data Output
$OUT2_N$	24	1	O	Channel 2 Negative LVDS Data Output
$OUT3_P$	27	1	O	Channel 3 Positive LVDS Data Output
$OUT3_N$	28	1	O	Channel 3 Negative LVDS Data Output
$OUT4_P$	29	1	O	Channel 4 Positive LVDS Data Output
$OUT4_N$	30	1	O	Channel 4 Negative LVDS Data Output
$OUT5_P$	31	1	O	Channel 5 Positive LVDS Data Output
$OUT5_N$	32	1	O	Channel 5 Negative LVDS Data Output
$OUT6_P$	33	1	O	Channel 6 Positive LVDS Data Output
$OUT6_N$	34	1	O	Channel 6 Negative LVDS Data Output
$OUT7_P$	37	1	O	Channel 7 Positive LVDS Data Output
$OUT7_N$	38	1	O	Channel 7 Negative LVDS Data Output
$OUT8_P$	39	1	O	Channel 8 Positive LVDS Data Output
$OUT8_N$	40	1	O	Channel 8 Negative LVDS Data Output
$ADCLK_P$	41	1	O	Positive LVDS ADC Clock Output
$ADCLK_N$	42	1	O	Negative LVDS ADC Clock Output
ISET	64	1	I/O	Bias Current Setting Resistor
$\overline{RESET}$	45	1	I	Reset to Default; 0 = Reset, 1 = Normal
$\overline{CS}$	76	1	I	Chip Select; 0 = Select, 1 = No Select
SDA	77	1	I	Serial Data Input
SCLK	78	1	I	Serial Data Clock

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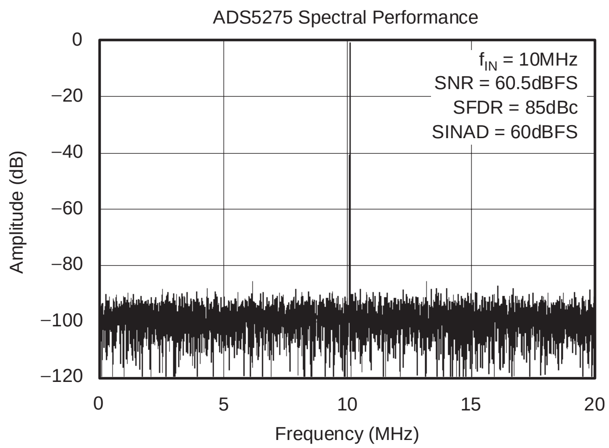
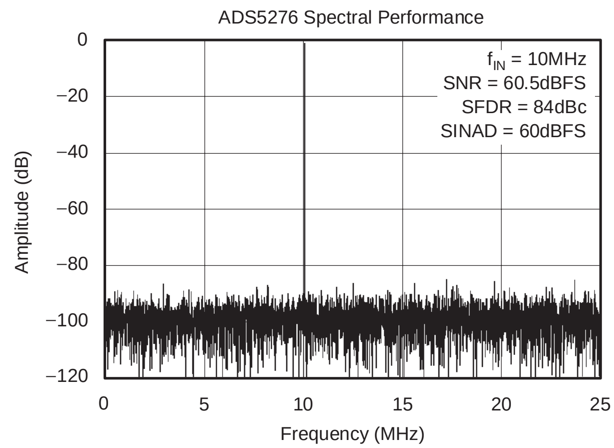
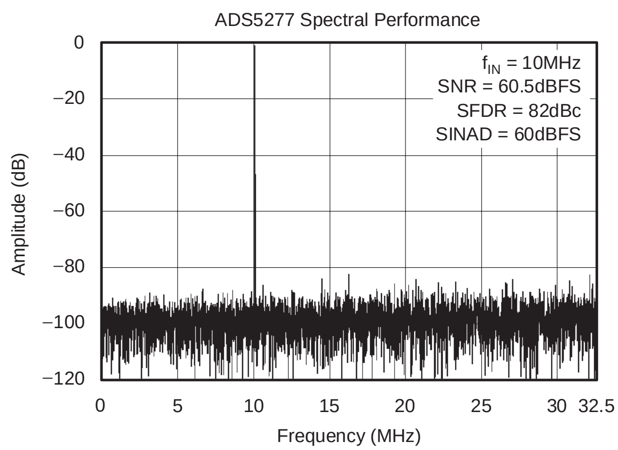
TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, −0.5dBFS, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.







PRODUCT PREVIEW

THEORY OF OPERATION

OVERVIEW

The ADS527x are 8-channel, high-speed, CMOS ADCs. They consist of a high-performance sample-and-hold circuit at the input, followed by a 10-bit ADC. The 10 bits given out by each channel are serialized and sent out on a single pair of pins in LVDS format. All eight channels of the ADS527x run off a single clock referred to as ADCLK. The sampling clocks for each of the eight channels are generated from the input clock using a carefully matched clock buffer tree. The 12X clock required for the serializer is generated internally from ADCLK using a phase lock loop (PLL). A 6X and a 1X clock are also output in LVDS format along with the data to enable easy data capture. The ADS527x operate from internally generated reference voltages that are trimmed to ensure matching across multiple devices on a board. This feature eliminates the need for external routing of reference lines and also improves matching of the gain across devices. The nominal values of REF_P and REF_N are 2V and 1V, respectively. This implies that a differential input of −1V corresponds to the zero code of the ADC, and a differential input of +1V corresponds to the full-scale code (4095 LSB). V_{CM} (common-mode voltage of REF_P and REF_N) is also made available externally through a pin, and is nominally 1.5V.

Both devices employ a pipelined converter architecture consisting of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 10-bit level. The pipeline architecture results in a data latency of 6.5 clock cycles.

The output of the ADC goes to a serializer that operates from a 12X clock generated by the PLL. The 10 data bits from each channel are serialized and output LSB first. In addition to serializing the data, the serializer also generates a 1X clock and a 6X clock. These clocks are generated in the same way the serialized data is generated, so these clocks maintain perfect synchronization with the data. The data and clock outputs of the serializer are buffered externally using LVDS buffers. Using LVDS buffers to transmit data externally has multiple advantages, such as reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital noise coupling to the analog circuit inside the ADS527x.

The ADS527x operate from two sets of supplies and grounds. The analog supply/ground set is denoted as AVDD/AVSS, while the digital set is denoted by LVDD/LVSS.

DRIVING THE ANALOG INPUTS

The analog input biasing is shown in Figure 1. The recommended method to drive the inputs is through AC coupling. AC coupling removes the worry of setting the common-mode of the driving circuit, since the inputs are biased internally using two 600Ω resistors. The sampling capacitor used to sample the inputs is 4pF. The choice of the external AC coupling capacitor is dictated by the attenuation at the lowest desired input frequency of operation. The attenuation resulting from using a 10nF AC coupling capacitor is 0.04%.

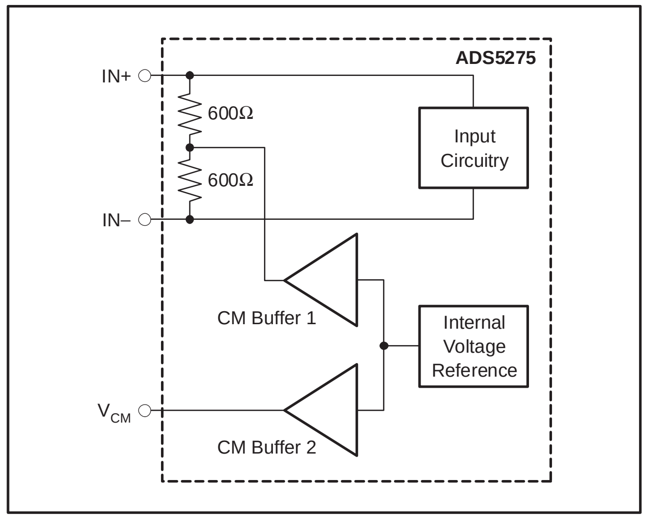


Figure 1. Analog Input Bias Circuitry

If the input is DC coupled, then the output common-mode voltage of the circuit driving the ADS527x should match the V_{CM} (which is provided as an output pin) to within ±50mV. It is recommended that the output common-mode of the driving circuit be derived from V_{CM} provided by the device.

INPUT OVER-VOLTAGE RECOVERY

The differential full-scale input peak-to-peak voltage supported by the ADS527x is 2V. For a nominal value of V_{CM} (1.5V), IN_P and IN_N can swing from 1V to 2V. The ADS527x are specially designed to handle an over-voltage differential peak-to-peak voltage of 4V (2.5V and 0.5V swings on IN_P and IN_N). If the input common-mode is less than 300mV from V_{CM} during overload, recovery from an over-voltage input condition is expected to be within 4 clock cycles. All of the amplifiers in the SHA and ADC are specially designed for excellent recovery from an overload signal.

PRODUCT PREVIEW

REFERENCE CIRCUIT DESIGN

The digital beam-forming algorithm relies heavily on gain matching across all receiver channels. A typical system would have about 10 octal ADCs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the ADCs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures the reference voltages are well matched across different chips.

All bias currents required for the internal operation of the device are set using an external resistor to ground at pin ISET. Using a 56kΩ resistor on ISET generates an internal reference current of 20μA. This current is mirrored internally to generate the bias current for the internal blocks. Using a larger external resistor at ISET reduces the reference bias current and thereby scales down the device operating power. However, it is recommended that the external resistor be within 10% of the specified value of 56k so that the internal bias margins for the various blocks are proper.

Buffering the internal bandgap voltage also generates a voltage called V_{CM}, which is set to the midlevel of REF_T and REF_B, and is accessible on a pin. The internal buffer driving V_{CM} has a drive of ±4mA. It is meant as a reference voltage to derive the input common-mode in case the input is directly coupled.

The device also supports the use of external reference voltages. This involves forcing REF_T and REF_B externally. In this mode, the internal reference buffer is tri-stated. Since the switching current for the eight ADCs comes from the externally forced references, it is possible for the performance to be slightly less than when the internal references are used. It should be noted that in this mode, V_{CM} and ISET continue to be generated from the internal bandgap voltage, as in the internal reference mode. It is therefore important to ensure that the common-mode voltage of the externally forced reference voltages matches to within 50mV of V_{CM}.

CLOCKING

The eight channels on the chip run off a single ADCLK input. To ensure that the aperture delay and jitter are same for all the channels, a clock tree network is used to generate individual sampling clocks to each channel. The clock paths for all the channels are matched from the source point all the way to the sample-and-hold. This ensures that the performance and timing for all the channels are identical. The use of the clock tree for matching introduces an aperture delay, which is defined as the delay between the rising edge of ADCLK and the actual instant of sampling. The aperture delays for all the channels are matched, and vary between 2.5ns to 4.5ns across devices. Another critical spec is the aperture jitter that is defined as the uncertainty of the sampling instant. The gates in the clock path are designed to give an rms jitter of about 1ps.

The input ADCLK should ideally have a 50% duty cycle. However, while routing ADCLK to different components on board, the duty cycle of the ADCLK reaching the ADS527x could deviate from 50%. A smaller (or larger) duty cycle eats into the time available for sample or hold phases of each circuit, and is therefore not optimal. For this reason, the internal PLL is used to generate an internal clock that has a 50% duty cycle.

The use of the PLL automatically dictates the lower frequency of operation to be about 20MHz.

LVDS BUFFERS

The LVDS buffer has two current sources, as shown in Figure 2. OUT_P and OUT_N are loaded externally by a resistive load that is ideally about 100Ω. Depending on the data being 0 or 1, the currents are directed in one or the other direction through the resistor. The LVDS buffer has four current settings. The default current setting is 3.5mA, and gives a differential drop of about ±350mV across the 100Ω resistor.

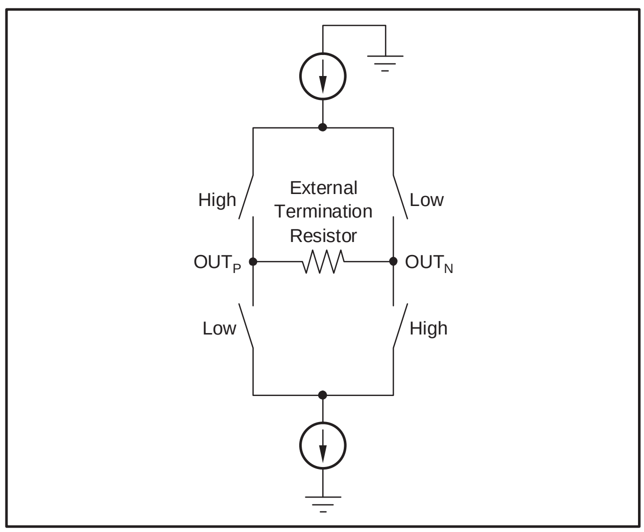


Figure 2. LVDS Buffer

The LVDS buffer gets data from a serializer that takes the output data from each channel and serializes it into a single data stream. For a clock frequency of 40MHz, the data rate output by the serializer is 480 MBPS. The data comes out LSB first, with a register programmability to revert to MSB first. The serializer also gives out a 1X clock and a 6X clock. The 6X clock (denoted as $LCLK_P$/ $LCLK_N$) is meant to synchronize the capture of the LVDS data. The deskew mode can be enabled as well, using a register setting. This mode gives out a data stream of alternate 0s and 1s and can be used determine the relative delay between the 6X clock and the output data for optimum capture. A 1X clock is also generated by the serializer and transmitted by the LVDS buffer. The 1X clock (referred to as $ADCLK_P/ADCLK_N$) is used to determine the start of the 10-bit data frame. The sync mode (enabled through a register setting) gives out a data of six 0s followed by six 1s. Using this mode, the 1X clock can be used to determine the start of the data frame. In addition to the deskew mode pattern and the sync pattern, a custom pattern can be defined by the user and output from the LVDS buffer.

NOISE COUPLING ISSUES

High-speed mixed signals are sensitive to various types of noise coupling. One of the main sources of noise is the switching noise from the serializer and the output buffers. Maximum care is taken to isolate these noise sources from the sensitive analog blocks. As a starting point, the analog and digital domains of the chip are clearly demarcated. AVDD and AVSS are used to denote the supplies for the analog sections, while LVDD and LVSS are used to denote the digital supplies. Care is taken to ensure that there is minimal interaction between the supply sets within the device. The extent of noise coupled and transmitted from the digital to the analog sections depends on the following:

1. The effective inductances of each of the supply/ground sets.
2. The isolation between the digital and analog supply/ground sets.

Smaller effective inductance of the supply/ground pins leads to better suppression of the noise. For this reason, multiple pins are used to drive each supply/ground. It is also critical to ensure that the impedances of the supply and ground lines on board are kept to the minimum possible values. Use of ground planes in the board as well as large decoupling capacitors between the supply and ground lines are necessary to get the best possible SNR from the device.

It is recommended that the isolation be maintained on board by using separate supplies to drive AVDD and LVDD, as well as separate ground planes for AVSS and LVSS.

The use of LVDS buffers reduces the injected noise considerably, compared to CMOS buffers. The current in the LVDS buffer is independent of the direction of switching. Also, the low output swing as well as the differential nature of the LVDS buffer results in low-noise coupling.

POWER-DOWN MODE

The device has a power-down pin, PD. Pulling PD high causes the device to enter the power-down mode. In this mode, the reference and clock circuitry as well as all the channels are powered down. The power consumption of the device drops to less than 100mW in this mode. Individual channels can also be selectively powered down by programming registers.

The ADS527x each have an internal circuit that monitors the state of stopped clocks. If ADCLK is stopped (or if it runs at a speed < 3MHz), this monitoring circuit generates a logic signal that puts the device in a power-down state. As a result, the power consumption of the device goes to less than 100mW when ADCLK is stopped. This circuit can also be disabled using register options.

SUPPLY SEQUENCE

The following supply sequence is recommended for powering up the device:

1. AVDD is powered up.
2. LVDD is powered up.

After the supplies have stabilized, it is required to give the device an active RESET pulse. This results in all internal registers resetting to their default value of 0 (inactive). Without RESET, it is possible that some registers might be in their non-default state on power-up. This condition could cause the device to malfunction.