QLogic Corporation

ISP2200A/33 and ISP2200A/66 Intelligent Fibre Channel Processors

Data Sheet

Features

- Available in two speed grades (collectively referred to as *ISP2200A*):
  - 66-MHz, 64-bit PCI host bus interface (ISP2200A/66)
  - 33-MHz, 64-bit PCI host bus interface (ISP2200A/33)
- Compliance with *PCI Local Bus Specification* revision 2.2
- Supports full-duplex communications in all Fibre Channel topologies
- Compliance with ANSI SCSI standards for class 2 and class 3 service:
  - *Fibre Channel Arbitrated Loop (FC-AL-2)* working draft, rev 6.4, August 28, 1998
  - *Fibre Channel Fabric Loop Attachment (FC-FLA)* working draft, rev 2.7, August 12, 1997
  - *Fibre Channel Private Loop SCSI Direct Attach (FC-PLDA)* working draft, rev 2.1, September 22, 1997
  - *Fibre Channel Tape (FC-TAPE)* profile, T11/98-124vD, rev 1.13, February 3, 1999
- Supports Fibre Channel protocol SCSI (FCP-SCSI) and Fibre Channel IP protocols
- Compliance with *PCI Bus Power Management Interface Specification* Revision 1.0 (PC98)
- Supports up to 200 Mbytes/sec sustained Fibre Channel data transfer rate
- Supports SCSI initiator, initiator/target, and target modes
- Onboard, enhanced RISC processor
- Onboard gigabit serial transceivers
- Supports PCI dual-address cycle and cache commands
- No host intervention required to execute complete SCSI and IP operations
- Supports multi-ID aliasing in target mode
- Supports external frame buffering for performance scalability over long distances

Product Description

The ISP2200A is a single-chip, highly integrated, bus master, Fibre Channel processor that targets storage, clustering, and networking applications. This chip connects the PCI bus to a Fibre Channel loop or to a point-to-point Fibre Channel port.

The ISP2200A/33 is pin compatible with the ISP2100A/33. The ISP2200A/66 is pin compatible with the ISP2100A/66.

The ISP2200A is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention.

The ISP2200A provides power management support in accordance with the *PCI Bus Power Management Interface Specification*. The ISP2200A block diagram is illustrated in figure 1.

ISP Initiator/Target SCSI and IP Firmware

The ISP2200A firmware implements a multitasking host adapter that provides the host system with IP communications and complete SCSI command and data transport capabilities, thus freeing the host system from the simultaneous execution of SCSI and IP traffic. The firmware provides two interfaces to the host system: the command interface and the Fibre Channel transport interface. The single-threaded command interface facilitates debugging, configuration, and recovering errors. The multithreaded transport interface maximizes use of the Fibre Channel and host buses.

The ISP2200A can operate simultaneously in SCSI initiator and target modes, and supports SCSI and IP protocols concurrently.

Software Drivers

The ISP2200A supports a host software interface similar to the QLogic parallel SCSI and FC-AL processor family. Existing ISP2100A software drivers for all major operating systems are easily modified to support the ISP2200A. The ISP2200A also supports FCP-SCSI and IP software drivers for most major operating systems.

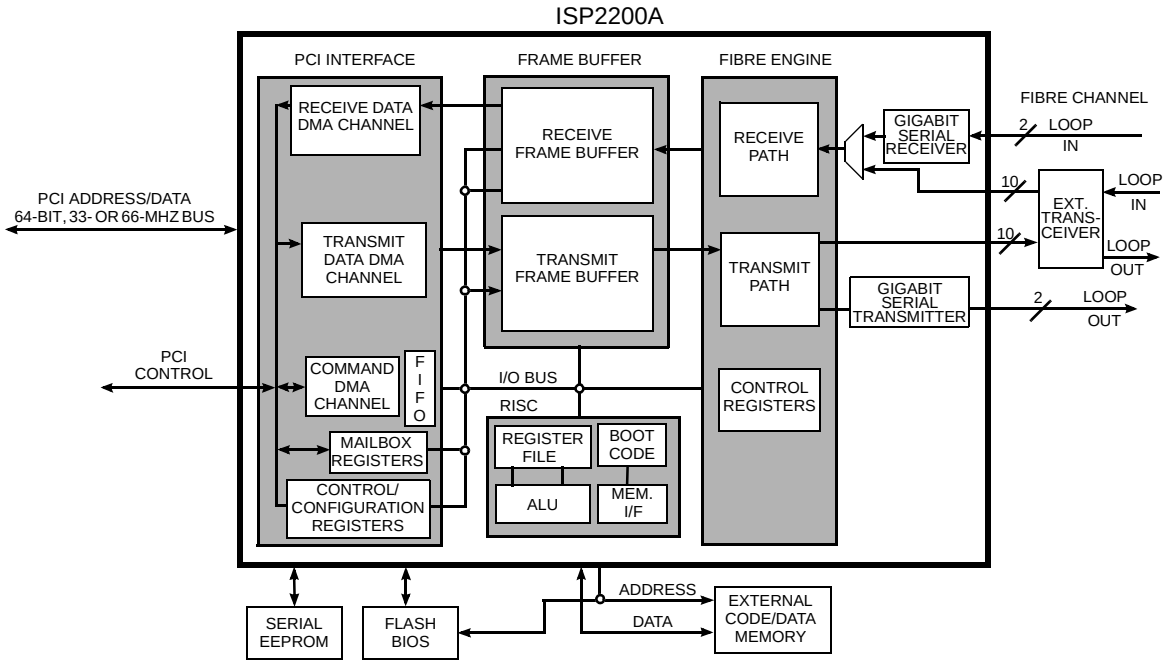

Figure 1. ISP2200A Block Diagram

Subsystem Organization

To maximize I/O throughput and improve host and Fibre Channel utilization, the ISP2200A incorporates a high-speed, proprietary RISC processor; a Fibre Channel protocol manager (FPM); integrated frame buffer memory; and a host bus, three-channel, bus master DMA controller. The FPM and host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance.

The complete I/O subsystem solution using the ISP2200A and directly connected hard drives is shown in figure 2.

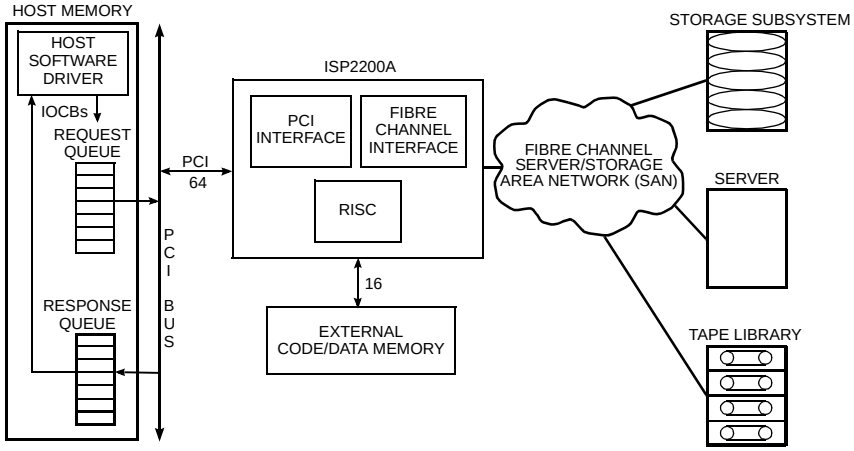

Figure 2. I/O Subsystem Design Using the ISP2200A

Interfaces

The ISP2200A interfaces consist of the FC-AL interface, PCI bus interface, RISC interface, flash BIOS interface, and NVRAM control. Pins that support these interfaces and other chip operations are shown in figure 3.

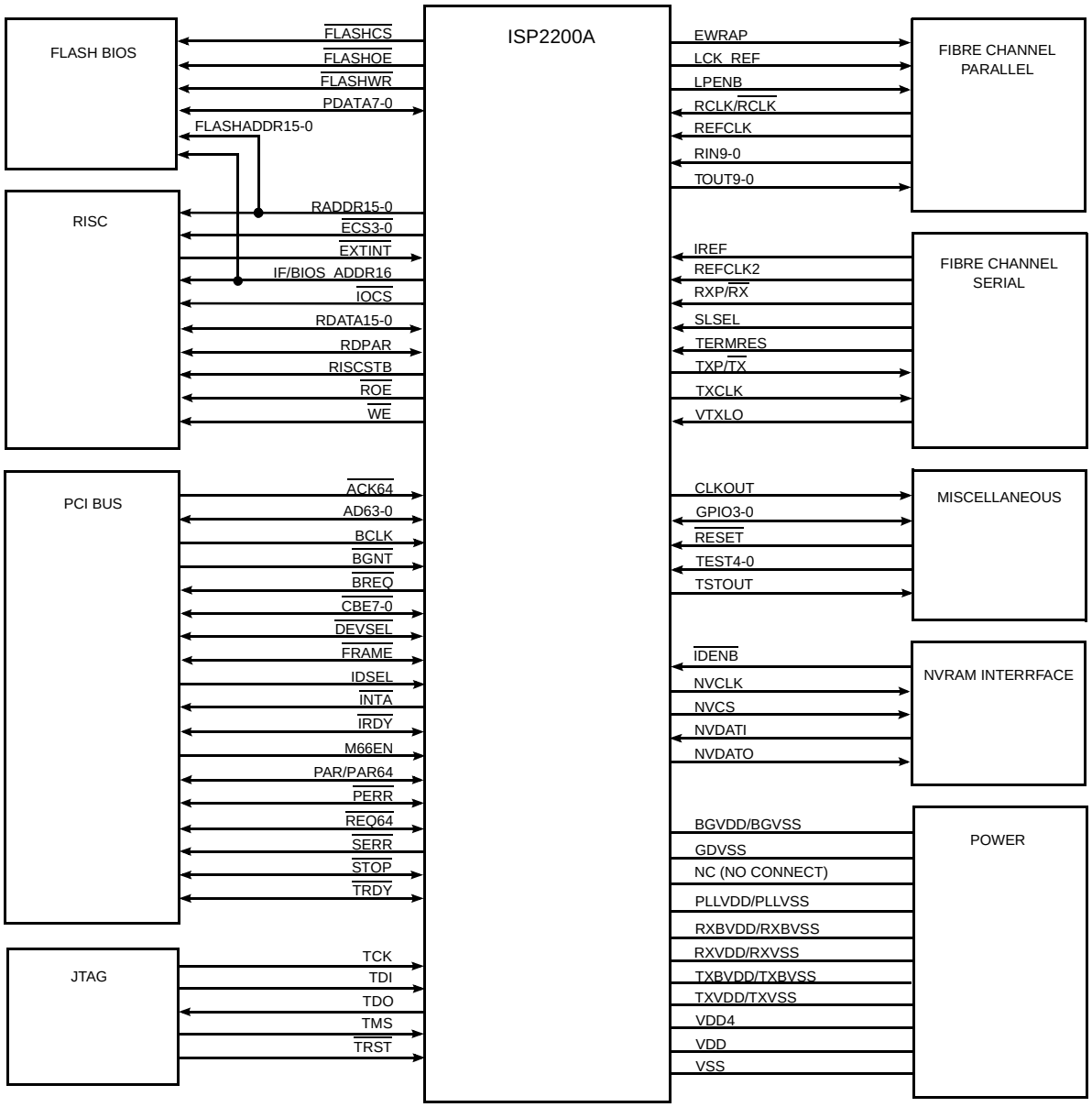

Figure 3. ISP2200A Functional Signal Grouping

Fibre Channel Interface

The ISP2200A provides onboard gigabit transceivers for direct connection to the Fibre Channel ports on copper media. A standard 10-bit interface is also provided to connect to external transceivers, if desired.

Fibre Channel Protocol Manager

The ISP2200A FPM supports the following:

- Support for one Fibre Channel port
- Gigabit serial interface
- Full-duplex data transfer rate up to 200 Mbytes/sec
- 10-bit interface to external transceivers
- Integrated frame buffer that supports up to 2112-byte frame payload
- 8b/10b encoder and decoder with clock skew management
- Support for an external buffer

The FPM transmits and receives at the full Fibre Channel rate of 106.25 Mbytes/sec. The on-chip frame buffer includes separate areas for received data and transmit data, as well as areas for managing special frames such as command and response. The FPM receive path validates and routes frames received from the Fibre Channel to the appropriate area in the frame buffer.

The transmit path transmits frames from the frame buffer to the Fibre Channel. The FPM automatically handles frame delimiters and frame control.

The external buffer supports additional receive buffering for 10-km optical Fibre Channel links to eliminate dead time and allow a remote transmitter to send frames continuously. Enough initial buffer credit can then be issued by the ISP2200A to keep a remote transmitter busy until it sees an R_RDY return.

PCI Interface

The ISP2200A PCI interface supports the following:

- 33-MHz (ISP2200A/33) or 66-MHz (ISP2200A/66), 64-bit, intelligent bus master interface
- 64-bit host memory addressing (dual address cycle)
- Backward compatible to 32-bit PCI
- Three-channel DMA controller
- 16-bit slave mode for communication with host
- Pipelined DMA registers for efficient scatter/gather operations
- 32-bit DMA transfer counter for I/O transfer length of up to four gigabytes
- Support for PCI cache commands
- Support for flash BIOS PROM
- Support for subsystem ID
- 3.3V and 5.0V tolerant PCI I/O buffers

The ISP2200A is designed to interface directly to the PCI bus and operate as a 64-bit DMA bus master. This function is accomplished through a PCI bus interface unit (PBIU) containing an onboard DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the onboard frame buffer. It also allows the host to access the ISP2200A internal registers and communicate with the onboard RISC processor.

The ISP2200A supports the minimum power management capabilities specified in revision 1.0 of the *PCI Bus Power Management Interface Specification*, which defines power states D0-D3, where D0 provides maximum power consumption and D3 provides minimal power consumption. The D3 power state is entered by either software (D3 *hot*) or by physically removing power (D3 *cold*). Hot and cold refer to the presence or absence of VCC, respectively.

The ISP2200A supports power states D0, D3 hot, and D3 cold.

The ISP2200A onboard DMA controller consists of three independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and frame buffer. The command DMA channel is used mainly by the RISC processor for small transfers, such as fetching commands from and writing status information to the host memory over the PCI bus. The two data DMA channels, one for transmit and one for receive, transfer data between the FC-AL and the PCI bus, allowing for fast context switching.

The PBIU internally arbitrates between the two data DMA channels and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

RISC Processor

The ISP2200A RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

One of the major features of the ISP2200A is its ability to handle complete I/O transactions from start to finish with no intervention from the host. This high level of integration is accomplished with the onboard RISC processor. The ISP2200A RISC processor controls the chip interfaces; executes simultaneous, multiple IOCBs; and maintains the required thread information for each transfer.

Packaging

The ISP2200A/33 and the ISP2200A/66 are available in a 256-pin ball grid array (BGA) package. The ISP2200A/33 is pin compatible with the ISP2100A/33. The ISP2200A/66 is pin compatible with the ISP2100A/66.