Preliminary Specification

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUITS

μPD16305GF

40bit ROW Driver for AC-PDP

The μPD16305 is a ROW driver utilized high voltage CMOS for AC plasma display panel. It consists of a 40bit bidirectional shift register, latch circuit, high voltage CMOS driver.

It operates at 5V (CMOS input level) and provides high voltage CMOS, 200V and 400mA max.

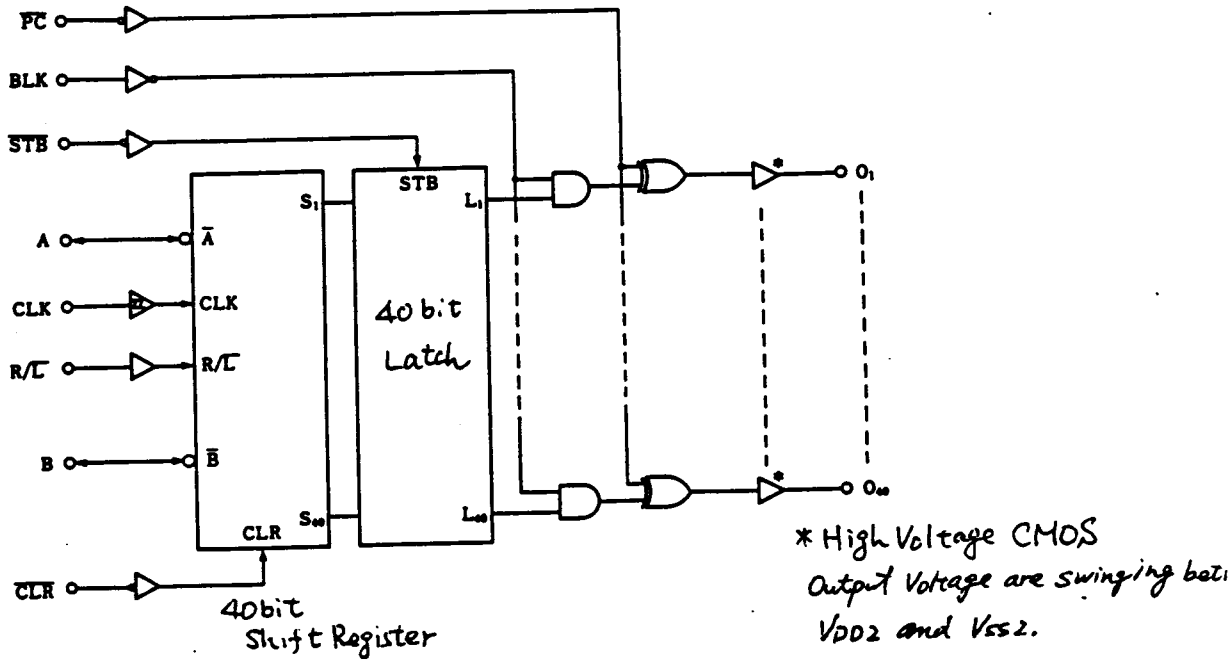
Features :

- High voltage CMOS structure
- High voltage/current Output (200V, 400mA max.)
- Built-in 40bit bidirectional shift register
- Low power dissipation (1mA max., Ta = -40 ～ +85℃)
- Wide operating temperature (-40 ～ +85℃)

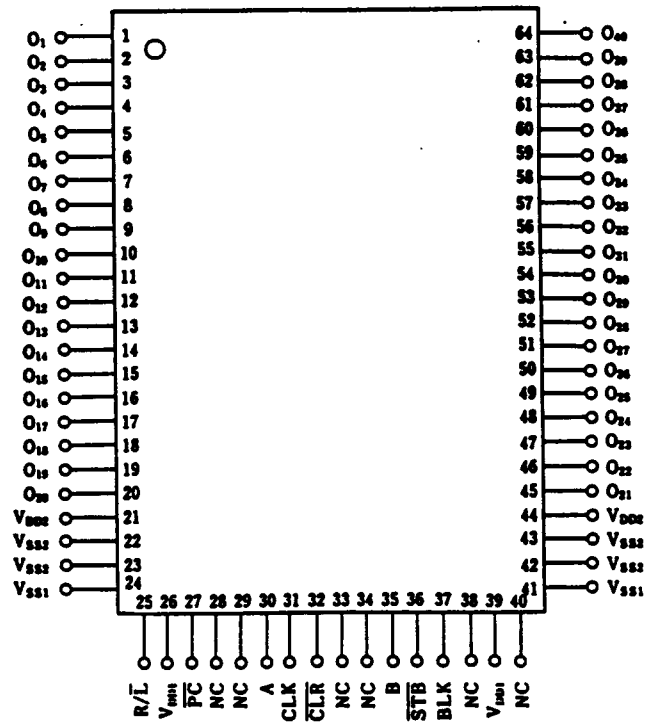
- ORDERING INFORMATION :

  μPD16305GF-3L9 : 80pin Plastic QFP (tri directional lead)

(BLOCK DIAGRAM)



(Top View)



* Please connect between outside the same power supply pins, such as VDD1 , VDD2, and Vss1 and Vss2.

* Please open 33pin because of connecting lead frame.

Pin Configuration

SYMBOL	Pin Name	Pin No.	Function
BLK	Blank Input	37	Refer to below Table 3
A	Right Date I/O	30	R/$\overline{L}$=H : A=IN, B=OUT R/L=L : B=IN, A=OUT
B	Left Data I/O	35	
CLK	Shift Clock Input	31	Positive edge active
$\overline{STB}$	Latch enable Input	36	H : Latch L : Data Through
R/$\overline{L}$	Shift Direction Control Input	25	H : Right shift mode A→O1~O40→B L : Left shift mode B→O40~O1→A
$\overline{CLR}$	Clear Input	32	L : Shift Register, ALL L
$\overline{PC}$	High Voltage Output	27	REFER TO TRUTH TABLE 3
O1 ~O40	High Voltage Output	1~20, 45~64	200V 400mA max.
VDD1	Logic Power Supply	26, 39	5V±10%
VDD2	Driver Power Supply	21, 44	30~240V
VSS1	Ground (Logic)	24, 41	—
VSS2	Ground (Driver)	22, 23, 42, 43	—
NC	No Connection	28, 29, 33, 34 38, 40	No connection Please open 33 pin.

Truth Table 1 (Shift Register)

R/L	CLK	A	B	SHIFT REGISTER
H	↑	Input	Output	Data shift (to Right)
H	H OR L			No change
L	↑	Output	Input	Data shift (to Left)
L	H OR L			No change

Truth Table 2 (Latch)

$\overline{STB}$	OPERATION
H	Data keep just before STB turns H.
L	Shift register data are output.

Truth T-able 3 (Driver)

DATA	BLK	$\overline{PC}$	On	Note
H	L	L	L	Data Reverse Output
L	L	L	H	Data Reverse Output
H	L	H	H	Data Output
L	L	H	L	Data Output
×	H	L	H	All Output : H
×	H	H	L	All Output : L

H = High level, L = Low level, × = H or L

Z = High Impedance

DATA = Contents of Latch L1~L40
(DATA are inverted A/B input.)

Absolute Maximum Ratings
(Ta=25℃, Vss1 = Vss2 = 0V)

ITEMS	SYMBOL	RATINGS	UNIT
Logic Power Supply	VDD1	-0.5~+7.0	V
Driver Power Supply	VDD2	-0.5~+200	V
Logic Output Voltage	V1	-0.5~VDD1+0.5	V
Driver Maximum current	IO	400 *1	mA
Input Current	II	±25	mA
Power Dissipation/Package	PD	1000	mW
Operating Temperature	Topt	-40~+85	℃
Storage Temperature	Tstg	-65~+150	℃

*1 ····· Duty ≦ 1/40

Recommended Operating Conditions
(Ta = -40 ~ +85℃, Vss1 = Vss2 = 0V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT.
Logic Power Supply	VDD1	4.5	5.0	5.5	V
Driver Power Supply	VDD2			180	V
Low Level Input Voltage	V1L	0		0.2·VDD1	V
High Level Input Voltage	V1H	0.7·VDD1		VDD1	V
Driver Output Current	IO			±300	mA

Electrical Characteristics
(Ta = 25℃, VDD1 = 4.5 ~ 5.5V, VDD2 = 180V
Vss = 0V)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Output Voltage	VOH1	Logic IOH1=-1mA	0.9·VDD1			V
Low Level Output Voltage	VOL1	Logic IOL1=1mA			0.1·VDD1	V
High Level Output Voltage	VOH21	O1-40, IOH=-150mA	160			V
	VOH22	O1-40, IOH=-300mA	140			V
Low Level Output Voltage	VOL21	O1-40, IOL=150mA			20	V
	VOL22	O1-40, IOL=300mA			40	V
Input current	II	VI=VDD1 or Vss			±1	μA
High Level Input Voltage	VIH		0.7 VDD1			V
Low Level Input Voltage	VIL				0.2 VDD1	V
Stand by Current	IDD1	Logic:-40~+85℃			1	mA
		Logic:Ta=25℃			10	μA
	IDD2	Driver:-40~+85℃			1	mA
		Driver:Ta=25℃			100	μA

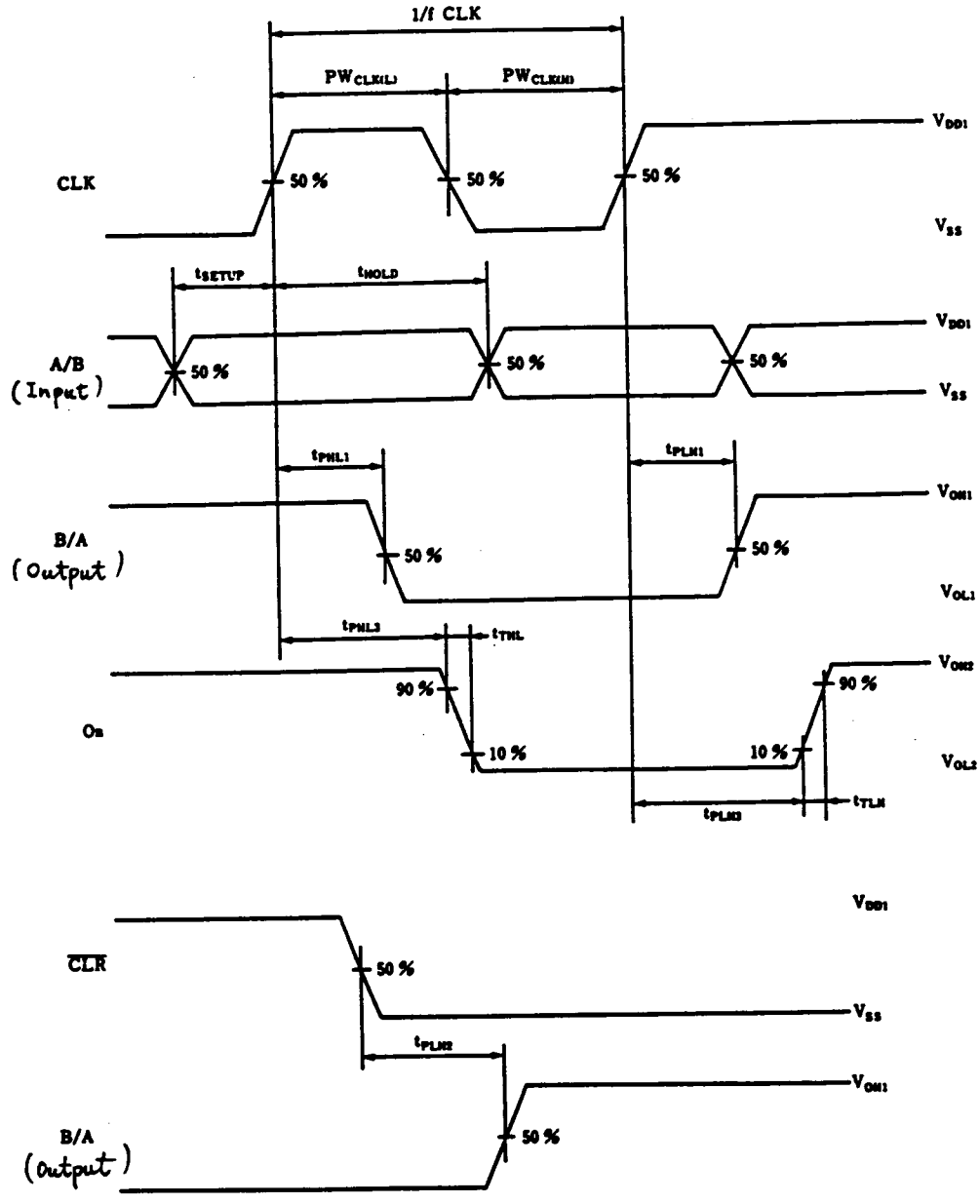
Switching Characteristics
(Ta = 25℃, VDD1 = 4.5 ~ 5.5V, VDD2 = 180V
Logic:CI = 15pF, Driver:CL = 50pF)

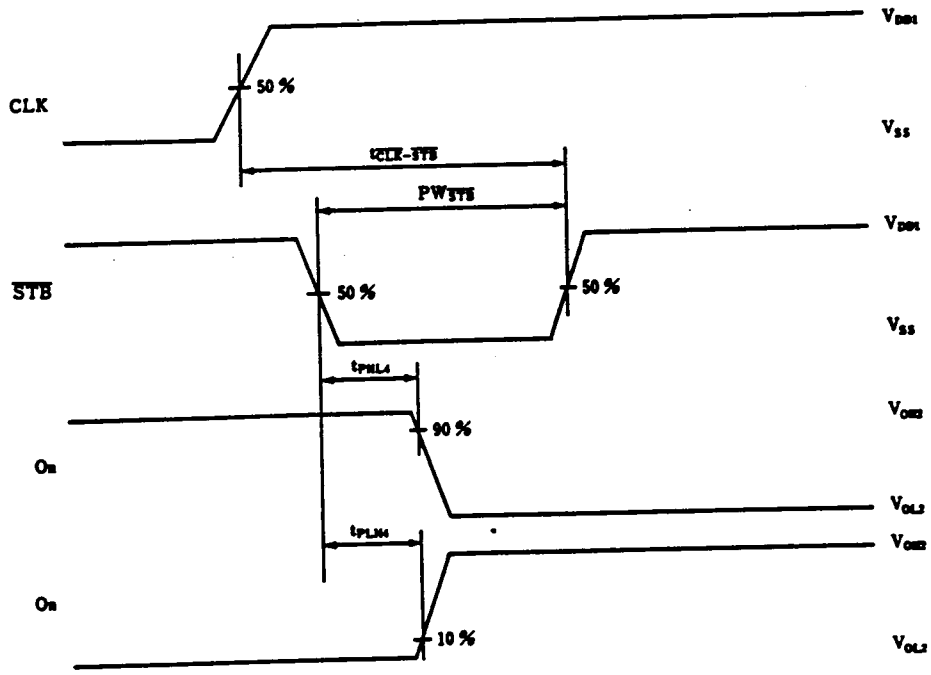
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Delay time	t PHL1	CLK→A/B			60	ns
	t PLH1				60	ns
	t PHL2	$\overline{CLR}$→A/B			60	ns
	t PHL3	CLK→O1~O40			150	ns
	t PLH3				150	ns
	t PHL4	$\overline{STB}$→O1~O40			125	ns
	t PLH4				125	ns
	t PHL5	BLK→O1~O40			100	ns
	t PLH5				100	ns
	t PHL6	$\overline{PC}$→O1~O40			75	ns
	t PLH6				75	ns
Output transient Time	t THL	O1-40			60	ns
	t TLH				60	ns
Maximum Clock Frequency	f MAX	Duty=50%	15			MHz
Input Capasitance	CI				10	pF

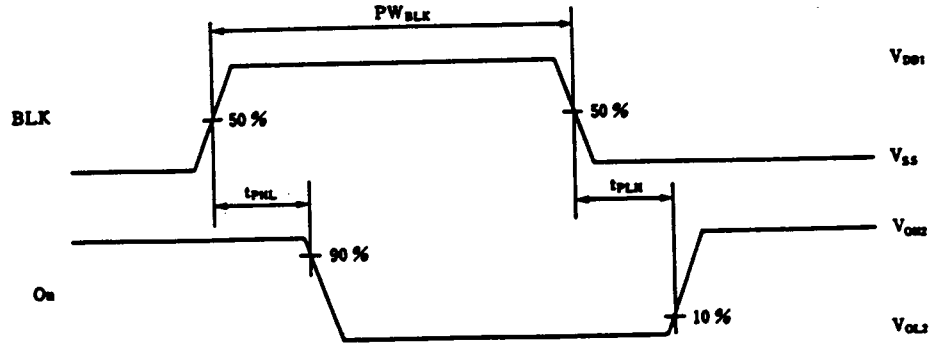
Timing Requirement Conditions
(Ta = -40 ~ +85℃, VDD1 = 4.5 ~ 5.5V)

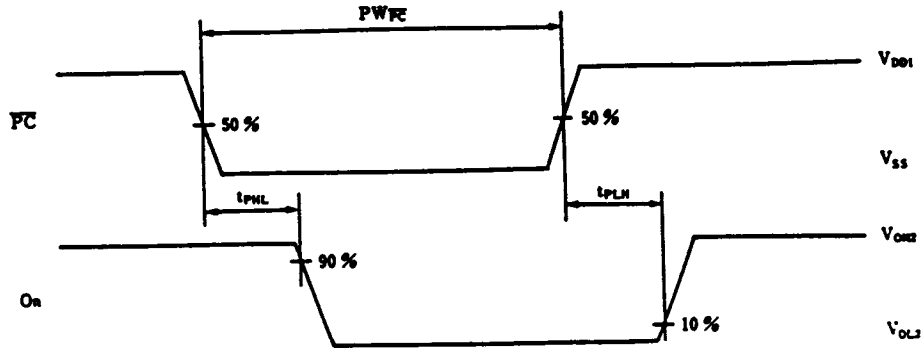
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	PWCLK		30			ns
Strobe Pulse Width	PW$\overline{STB}$		60			ns
Blank Pulse Width	PWBLK		200			ns
Polarity Change Pulse Width	PW$\overline{PC}$		150			ns
Clear Pulse Width	PW$\overline{CLR}$		120			ns
Data Setup Time	t SETUP		20			ns
Data Hold Time	t HOLD		5			ns
Setup Time (CLK → STB)	t CLK-$\overline{STB}$	CLK↑→$\overline{STB}$↑	60			ns

Switching Characteristics Waveform

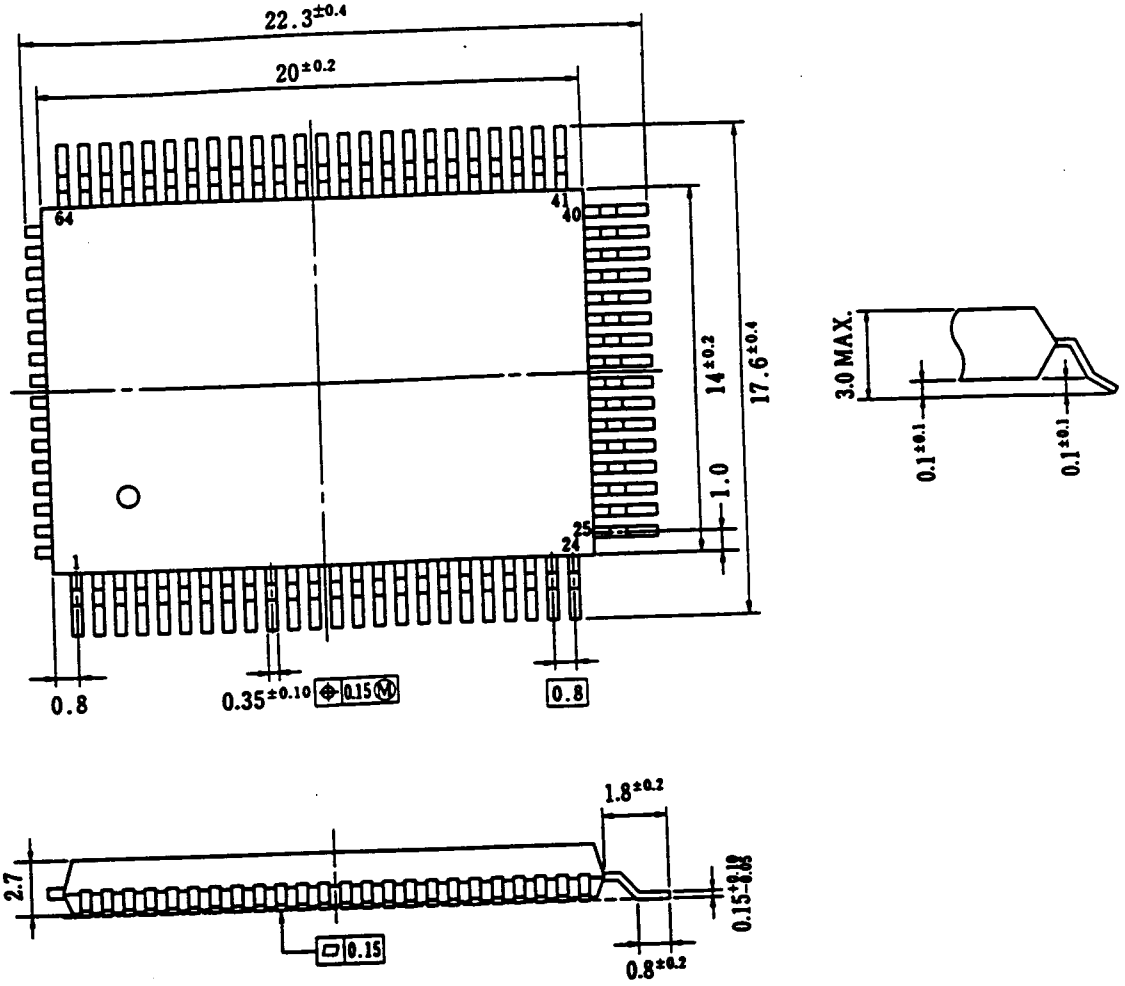



CLK
STB
On
On
50 %
50 %
50 %
90 %
10 %
$t_{CLK-STB}$
PW_{STB}
t_{PHL4}
t_{PLH4}
V_{DD1}
V_{SS}
V_{DD1}
V_{SS}
V_{OH2}
V_{OL2}
V_{OH2}
V_{OL2}


BLK
On
50 %
50 %
90 %
10 %
PW_{BLK}
t_{PHL}
t_{PLH}
V_{DD1}
V_{SS}
V_{OH2}
V_{OL2}


FC
On
50 %
50 %
90 %
10 %
PW_{FC}
t_{PHL}
t_{PLH}
V_{DD1}
V_{SS}
V_{OH2}
V_{OL2}

Pakage Dimensions 80 Pin Plastic QFP (14×20) (3 direction leads)
Unit (mm)



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