NEC Electronics Inc.

μPD7554/54A/64/64A 4-Bit, Single-Chip CMOS Microcomputers With Serial I/O

Description

The μPD7554/54A and μPD7564/64A are low-end versions of μPD7500 series products. These microcomputers incorporate a serial interface and are useful as slave CPUs to high-end μPD7500 series or 8-bit μCOM-87 series products.

The μPD7554/54A/64/64A has output ports that can directly drive triacs and LEDs. Also, various mask-optional I/O circuits can be configured for a wide selection of outputs allowing a reduction of external circuitry in your design.

The μPD7554/54A and μPD7564/64A differ only in their clock circuitry. The μPD7554/54A uses an external resistor with an internal capacitor for an RC oscillator clock, where the μPD7554/54A uses an external ceramic oscillator as a clock. These microcomputers are ideally suited to control devices such as plain paper copiers (PPCs), printers, VCRs, and audio equipment.

Features

- 47 instructions (subset of μPD7500 set B)
- Instruction cycle:
  - — External clock: 2.86 μs/700 kHz, 5 V
  - — RC oscillator (μPD7554/54A): 4 μs/500 kHz, 5 V
  - — Ceramic oscillator (μPD7564/64A): 3 μs/660 kHz, 5 V
- Program memory (ROM) of 1024 x 8-bits
- Data memory (RAM) of 64 x 4-bits
- 8-bit timer/event counter
- 8-bit serial interface
- I/O lines: 16-μPD7554/54A; 15-μPD7564/64A
- Data memory retention at low supply voltage
- CMOS technology
- Low-power consumption
- Single power supply
  - — 2.5 to 6.0 V (μPD7554/54A)
  - — 2.7 to 6.0 V (μPD7564/64A)
  - — 2.0 to 6.0 V (μPD7554A)

Ordering Information

Part Number	Package Type
μPD7554CS	20-pin plastic shrink DIP
μPD7554ACS	
μPD7564CS	
μPD7564ACS	
μPD7554G	20-pin plastic SOP
μPD7554AG	
μPD7564G	
μPD7564AG	

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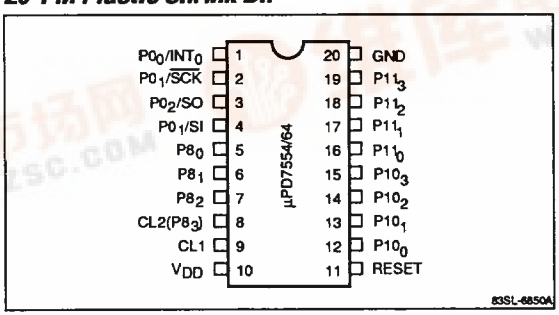
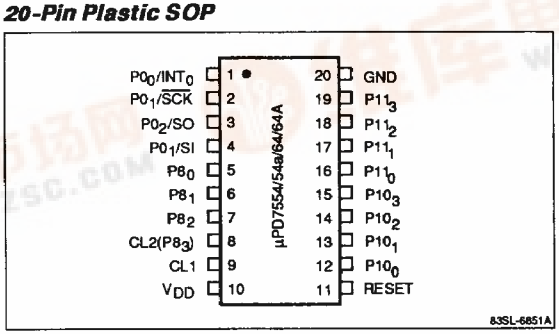
Pin Configurations

20-Pin Plastic Shrink DIP



20-Pin Plastic SOP



Pin Identification

Symbol	Function
$P0_0$/INTO	4-bit input port 0/count clock input/serial interface
$P0_1$/$\overline{SCK}$	
$P0_2$/SO	
$P0_3$/SI	
$P8_0$-$P8_2$	4-bit output port 8
$P8_3$/CL_2	Connection for ceramic resonator or RC
CL1	Connection for ceramic resonator or RC
V_{DD}	+5 V power supply
RESET	Reset input pin
$P10_1$-$P10_3$	4-bit I/O port 10
$P11_0$-$P11_3$	4-bit I/O port 11
V_{SS}	Ground

PIN FUNCTIONS

$P0_0$/INT0, $P0_1$/$\overline{SCK}$ $P0_2$/SO, $P0_3$/SI (Port 0/Count clock input/Serial interface)

4-bit input port 0/count clock input/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface, under control of the serial mode select register. The serial input SI (active high), serial output SO (active low), as the serial clock $\overline{SCK}$ (active low—synchronizes data transfer) comprise the 8-bit serial I/O interface. If $P0_0$/INT0 is unused, connect it to ground. If any of $P0_1$-$P0_3$ are unused, connect them to ground or V_{DD}. The port is in the input state at reset.

$P8_0$-$P8_2$, $P8_3$-CL2 (Port 8/Clock input 2)

4-bit output port 8. This port can sink 15 mA and interface 12 V. On the μPD7554/54A, the port function of $P8_3$/CL2 is specified by mask option. $P8_3$ is a normal output port on the μPD7564/64A. On the μPD7554/54A, CL2 is one of the pins to which a resistor for RC oscillation is connected. On the μPD7564/64A, CL2 is one of the pins to which a ceramic resonator is connected. If any of $P8_0$-$P8_2$ pins are unused, leave them open. The port is in the high impedance state at reset.

CL1 (Clock input 1)

On the μPD7554/54A, CL1 is one of the two pins to which a resistor for RC oscillation is connected. On the μPD7564/64A, CL1 is one of the two pins to which a ceramic resonator is connected.

V_{DD} (Power supply)

Positive power supply.

RESET (Reset)

System reset input pin (active high). This pin can be internally connected to a pull-down resistor if specified by mask option.

$P10_0$-$P10_3$ (Port 10)

4-bit I/O port. This port can sink 10 mA and interface 12 V. If any of these pins are unused, connect them to ground or V_{DD} in the input state, or leave open in the output state. The port is in the high impedance or high-level output state at reset.

$P11_0$-$P11_3$ (Port 11)

4-bit I/O port. This port can sink 10 mA and interface 12 V. If any of these pins are unused, connect them to ground or V_{DD} in the input state, or leave open in the output state. The port is in the high impedance or high-level output state at reset.

V_{SS} (Ground)

Ground.

Pin Mask Options

Table 1 shows the mask options for all the port pins and the RESET pin. You may select these options in bit units.

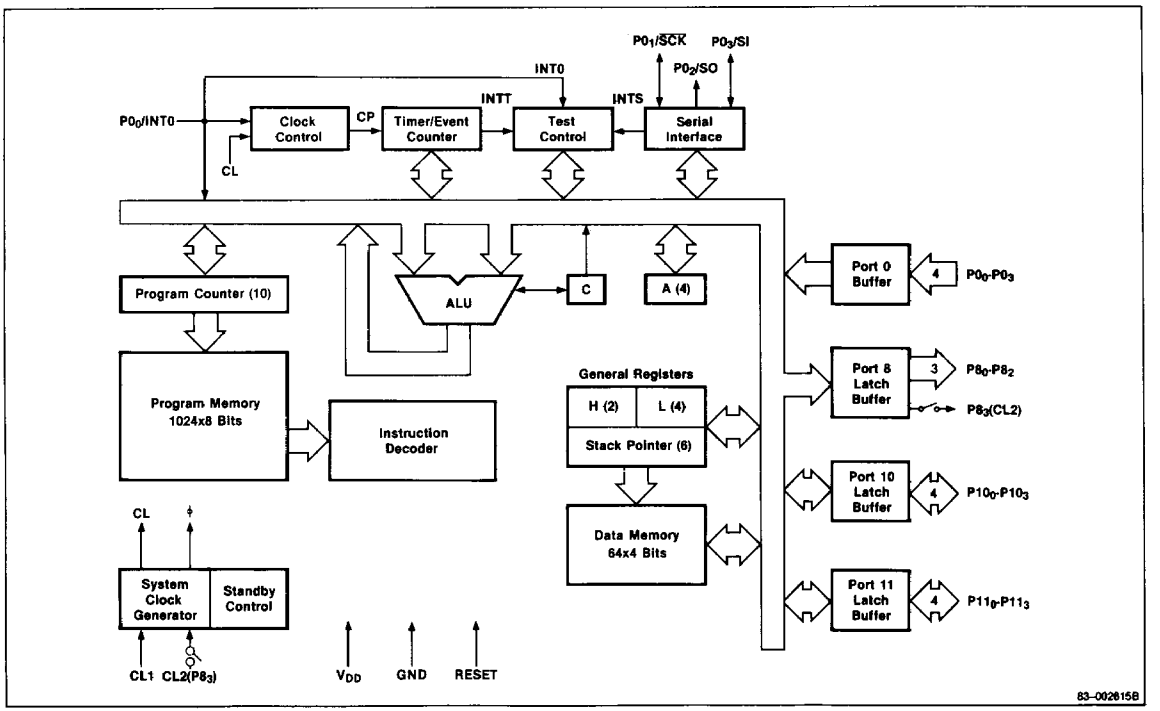
Table 1. Pin Mask Options

Pin	Options
$P0_0$-$P0_3$	1 No connection to internal resistor 2 Connected to internal pull-up resistor 3 Connected to internal pull-down resistor
$P8_0$-$P8_2$	1 CMOS (push-pull) output 2 N-channel, open-drain output
$P8_3$/CL2 (1)	1 Use as $P8_3$ 2 Use as CL2
Used as $P8_3$	1 CMOS (push-pull) output 2 N-channel, open-drain output
$P10_0$-$P10_3$ $P11_0$-$P11_3$	1 N-channel, open drain input/output 2 CMOS (push-pull) input/output 3 N-channel, open-drain input/output with internal pull-up resistor
RESET	1 Connected to internal pull-down resistor 2 Not connected to internal pull-down resistor

Notes:

(1) μPD7554/54A only.

μPD7554/54A Block Diagram



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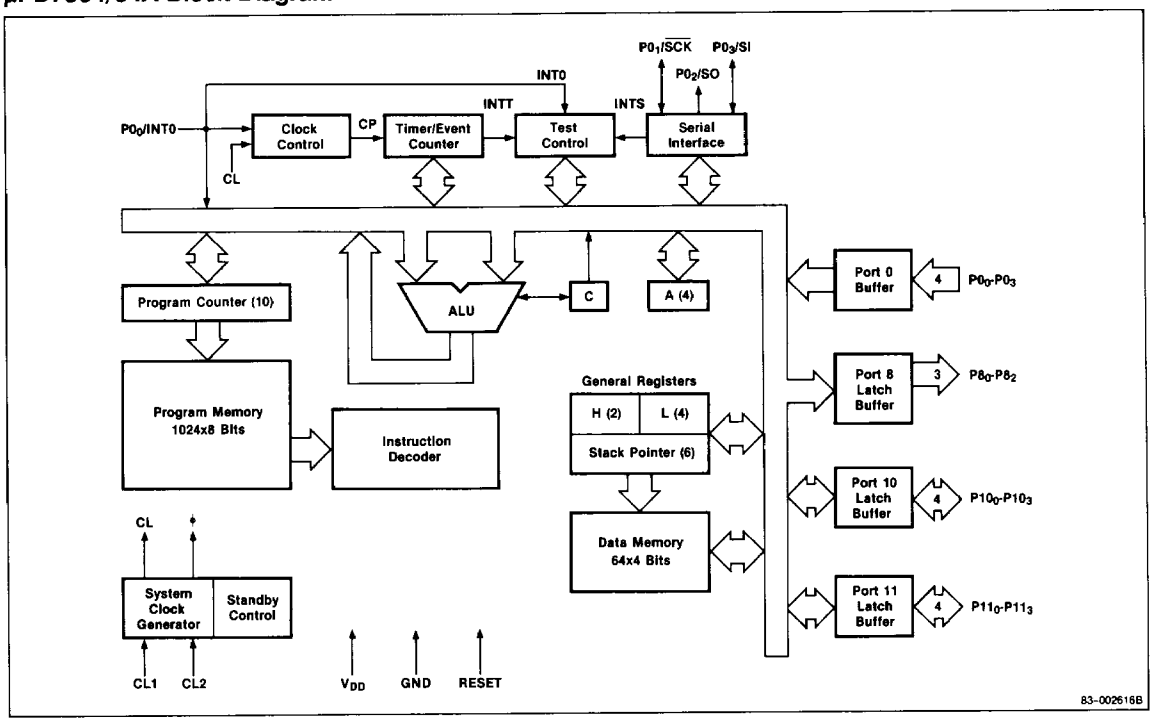
μPD7564/64A Block Diagram



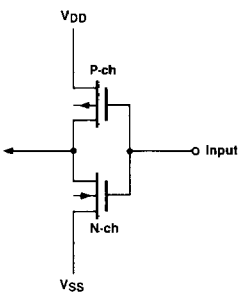
FUNCTIONAL DESCRIPTION

I/O Ports

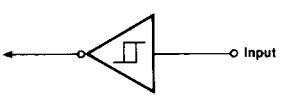
Figure 1 shows the internal circuits at I/O ports P0, P8, P10, and P11.

Figure 1. Interface at I/O Ports

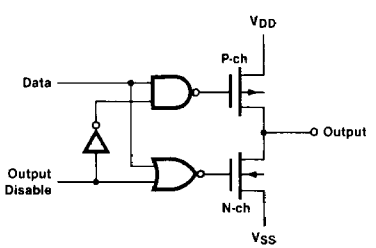
Type A. CMOS Input Cell
(Part of Type E)



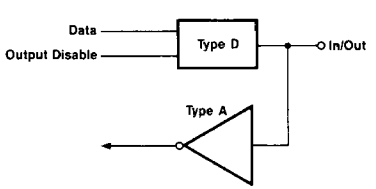
Type B. Schmitt-Triggered Input
P00/INT0, P03/SI



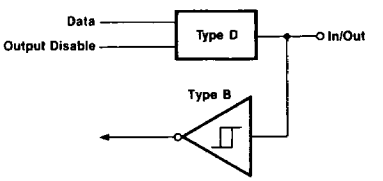
Type D. Push-Pull Output (part of types E and F)
High impedance on RESET (output disabled); both P- and N-channel transistors are turned off.



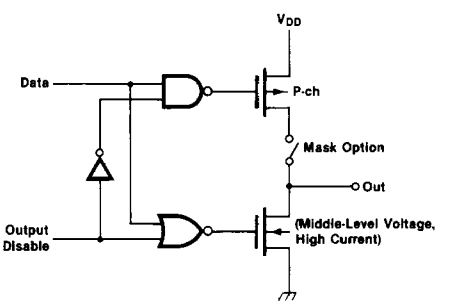
Type E. Type D Output with Type A Input Buffer
P02/SO



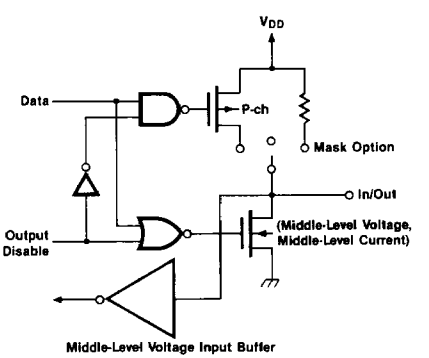
Type F. Type D Output with Type B Schmitt-Triggered input
P01/SCK



Type O. Mid-Level Voltage, High-Current
P80/P82, P83/CL2



Type P. Mid-level Voltage Input Buffer
P100-P103, P110-P113



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Program Memory

The μPD7554/54A/64/64A has a mask-programmable ROM with a capacity of 1024 words by 8 bits for program storage. It is addressed by the program counter. The reset start address is 000H. Figure 2 shows the program memory map.

General-Purpose Registers

Two registers, H(2-bit) and L(4-bit), are provided as general-purpose registers. Each register can be individually manipulated. The two registers also form pair register HL; H being the high register and L being the low one. The HL register is a data pointer to address data memory. Figure 3 shows the configuration of the general purpose registers.

The L register also specifies an I/O port or mode register when an I/O instruction (IPL or OPL) is executed. It also specifies the bits of a port when the SPBL or RPBL instruction is executed.

Data Memory

The data memory is static RAM with a capacity of 64 words by 4 bits. Part of this memory is used as the stack area. The data memory is also used in 8-bit data processing when paired with the accumulator. Figure 4 shows the data memory map.

Data memory can be addressed directly, with the immediate data from an instruction; indirectly, with the contents of HL (including auto-increment and auto-decrement); and indirectly by the contents of the stack pointer.

You may use any area of the data memory as the stack. The boundary of the stack is determined by how the TAMSP instruction initializes the stack pointer. Once the boundary is set, a call or return instruction automatically accesses the stack.

When a call instruction is executed, the contents of the program counter and the program status word (PSW) are stored to the stack in the sequence shown in figure 5.

When a return instruction is executed, the contents of the program counter are automatically restored, but the PSW is not. The contents of data memory can be retained with a low supply voltage during STOP mode.

Accumulator

The accumulator is a 4-bit register used in arithmetic operations. The accumulator can process 8-bit data with paired data addressed by HL. Figure 6 shows the configuration of the accumulator.

Arithmetic Logic Unit

The arithmetic logic unit (ALU) is a 4-bit arithmetic circuit that performs operations such as binary addition, logical operation, increment, decrement, comparison, and bit processing.

Program Status Word

The program status word (PSW) consists of two skip flags (SK0 and SK1), a carry flag (C), and bit 1, which is always zero. Figure 7 shows the configuration of the PSW.

The contents of the PSW are stored to the stack when a call instruction is executed, but are not restored from the stack by the return instruction.

The skip flags retain the following skip conditions: string effect by LAI or LHLI instruction, and skip condition satisfied by an instruction other than a string-effect instruction. The skip flag is set or reset according to the instruction executed.

The carry flag is set to 1 if an addition instruction (ACSC) generates a carry from bit 3 of the ALU. If no carry is generated, the flag is reset to zero. The SC instruction sets the carry flag and the RC instruction resets it.

When a RESET is input, the SK1 and SK0 flags are cleared to zero and the contents of the carry flag are undefined.

Figure 2. Program Memory Map

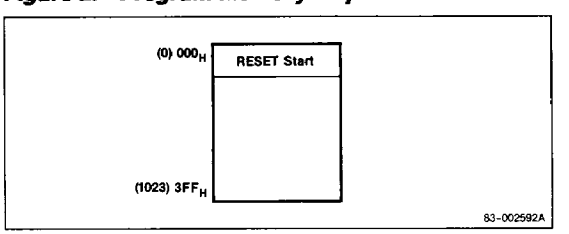


Figure 3. Configuration of General Purpose Registers

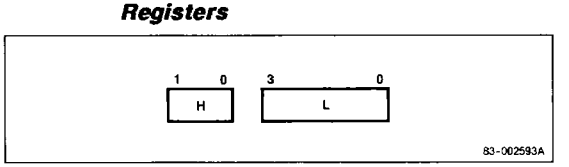


Figure 4. Data Memory Map

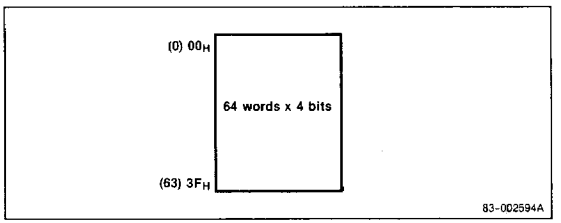


Figure 5. Call Instruction Storage to Stack

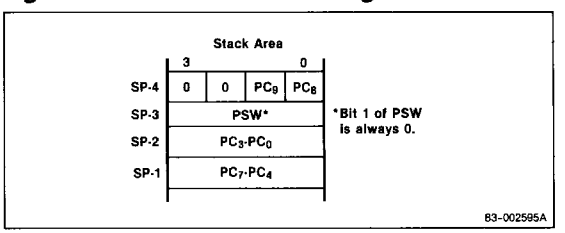


Figure 6. Configuration of the Accumulator

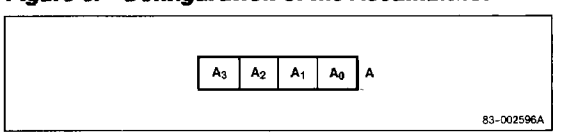
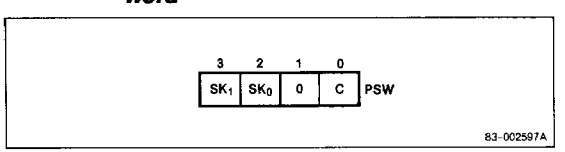


Figure 7. Configuration of the Program Status Word



System Clock Generator

The system clock generator consists of a ceramic oscillator, a 1/2 frequency divider, standby modes (STOP/HALT), and control circuit. Figure 8 is a circuit diagram of the system clock generator.

In the μPD7554/54A, the RC oscillator operates with a single external resistor connected across CL1 and CL2 (the capacitor C is incorporated). When the RC oscillator is not used, external clock pulses can be input by the CL1 pin. In this case, the RC oscillator functions as an inverting buffer. The output from the RC oscillator serves as the system clock (CL) which is then divided by two and used as the CPU clock (ϕ).

The standby mode control circuit is made up of a STOP flip-flop and a HALT flip-flop. The STOP instruction sets the STOP flip-flop and stops the system clock supply. This flip-flop also stops the RC oscillator. The STOP flip-flop is reset by the standby release signal that becomes active when one of the test requests flags is set or at the falling edge of the RESET signal. When the STOP flip-flop is reset, the RC oscillator resumes operation and supplies the system clock.

The HALT and STOP instructions and RESET HIGH set the HALT flip-flop which disables signals from going to the 1/2 frequency divider that generates the CPU clock. Only the CPU clock stops in HALT mode. The HALT flip-flop is reset by the same conditions as the STOP flip-flop.

Figure 9 shows the system clock generator circuit for the μPD7564/64A.

On the μPD7564/64A, the ceramic oscillator operates with a ceramic resonator connected across CL1 and CL2. The output from the ceramic oscillator is used as the system clock (CL); it is divided by two to produce the CPU clock (ϕ).

The standby mode control circuit is made up of a STOP flip-flop and a HALT flip-flop. The STOP instruction sets the STOP flip-flop and stops the ceramic oscillation, thus stopping the supply for all clocks. The STOP flip-flop is reset by the RESET signal (high level) and restarts ceramic oscillation. The supply of each clock resumes when RESET goes low.

The HALT instruction sets the HALT flip-flop which disables signals from going to the 1/2 frequency divider that generates the CPU clock. Only the CPU clock stops in HALT mode. The HALT flip-flop is reset by the HALT RELEASE signal (activated by setting at least one test request flag) or the falling edge of RESET, resuming supply of the CPU clock.

The HALT flip-flop is also set when RESET is active (high level). At power on reset operation, the rising edge of RESET starts ceramic oscillation; however, some time is required to achieve stable oscillation. To prevent the unstable clock from operating the CPU, the HALT flip-flop is set and the CPU clock is stopped while RESET is high. Accordingly, the high-level width of RESET must be more than the required stable time for the ceramic resonator.

Figure 8. System Clock Generator for μPD7554/54A

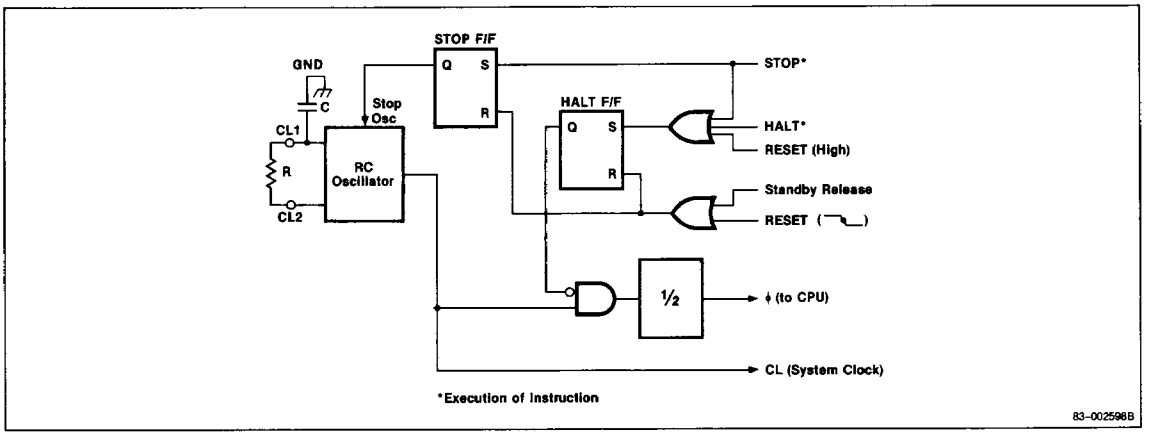
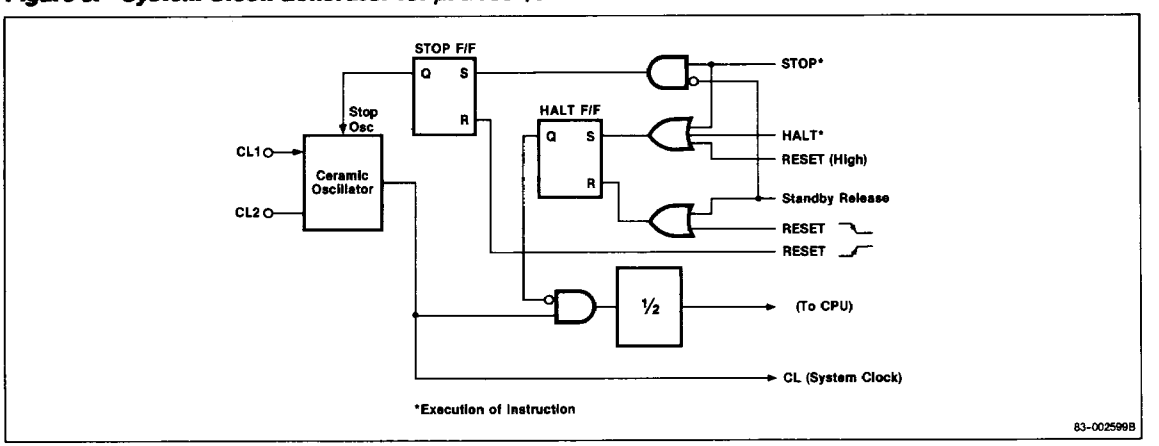


Figure 9. System Clock Generator for μPD7564/64A



Clock Control Circuit

The clock control circuit consists of a 2-bit clock mode register (bits CM1 and CM2), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and event pulses ($P0_0$). It also selects the clock source and prescaler according to the setting in the clock mode register and supplies the timer/event counter with count pulses. Figure 10 shows the clock control circuit.

Table 2 lists the codes set in the clock mode register by the OPL instruction to specify the count pulse frequency.

When you set the clock mode register with the OPL instruction, clear bit 0 of the accumulator (corresponding to bit CM0 of the EVAKIT-7500 or μPD7500H during emulation).

Figure 10. Clock Control Circuit

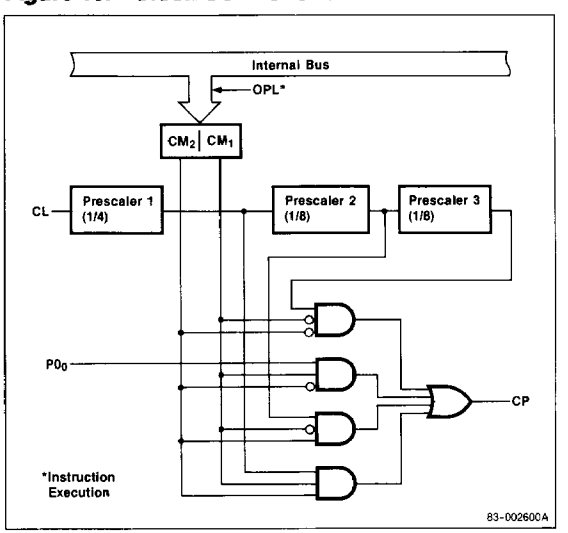


Table 2. Selecting the Count Pulse Frequency

CM2	CM1	Frequency Selected
0	0	CL/256
0	1	$P0_0$
1	0	CL/32
1	1	CL/4

Timer/Event Counter

The timer/event counter is a binary 8-bit up-counter which is incremented each time a count pulse is input. The TIMER instruction or a RESET signal clears it to 00H. When an overflow occurs, the counter is reset from FFH to 00H. Figure 11 shows the inputs and outputs of the counter.

Serial Interface

The serial interface consist of an 8-bit shift register, a 3-bit shift mode register, and a 3-bit counter. This interface inputs and outputs serial data. Figure 12 is a block diagram of the interface.

Test Control Circuit

The μPD7564/64A has three test sources, as shown in table 3.

The test control circuit consists of two test request flags (INTT RQF and INT0/S RQF) set by the three test sources, and a test request flag control circuit that checks the contents of each test request flag by executing an SKI instruction and resetting the flags.

Test sources INT0 and INTS share the request flag INT0/S RQF. Bit 3 of the shift mode register (SM_3) determines which source is selected. A zero in SM_3 selects INTS and a one selects INT0.

Figure 11. Timer/Event Counter

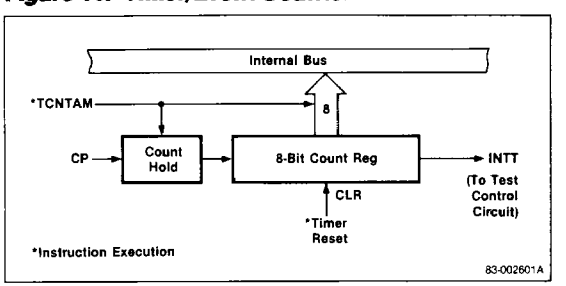


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Table 3. μPD7564/64A Test Sources

Source	Function	Location	Request Flag
INTT	Overflow in timer/ event counter	Internal	INTT RQF
INT0	Test request signal from $P0_0$ pin	External	INT0/S RQF
INTS	Transfer complete signal from serial interface	Internal	INT0/S RQF

The request flag INTT RQF is set when a timer overflow occurs in the timer event counter. The SKI or TIMER instruction resets it.

When SM_3 is zero, request flag INT0/S RQF is set when the INTS signals is generated, indicating the end of an 8-bit serial data transfer. The SKI or SIO instruction resets the flag.

When SM_3 is one, request flag INT0/S RQF is set at the rising edge of the signal input to the $P0_0$/INT0 pin. The SKI instruction resets the flag.

The logical sum of the outputs from the test request flags releases standby mode (STOP[1] or HALT mode). The mode is released when one or both flags are set. Both flags and SM_3 are reset when the RESET signal is input. After reset, source INTS is selected and signal input to the INT0 pin is inhibited as the initial condition.

Figure 13 is a block diagram of the test control circuit.

Note: (1) Only μPD7554/54A.

Figure 12. Serial Interface Block Diagram

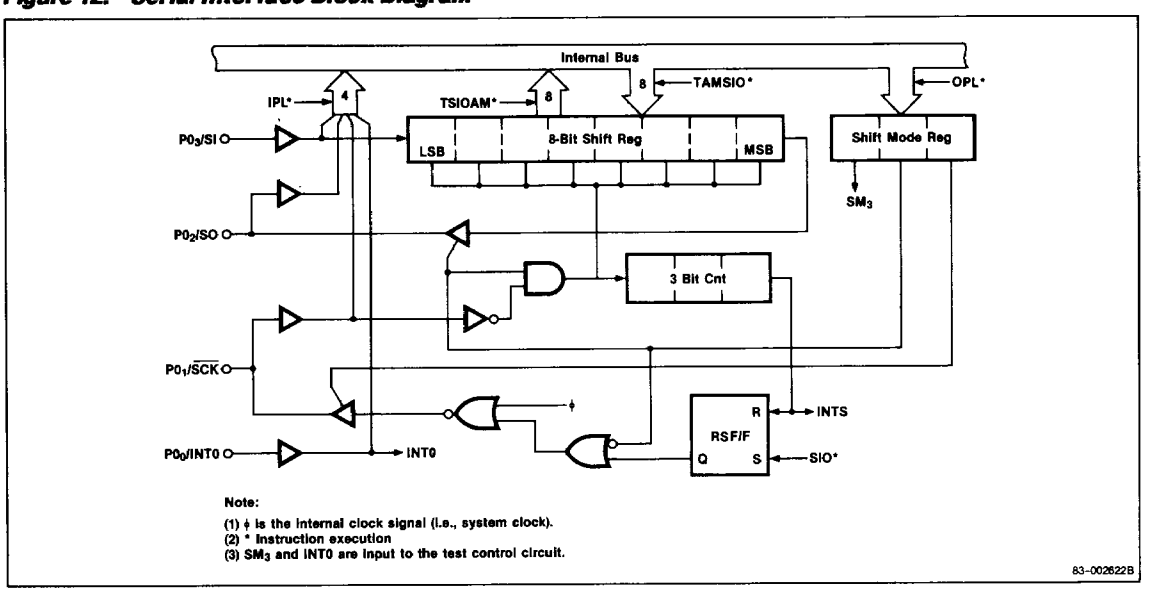
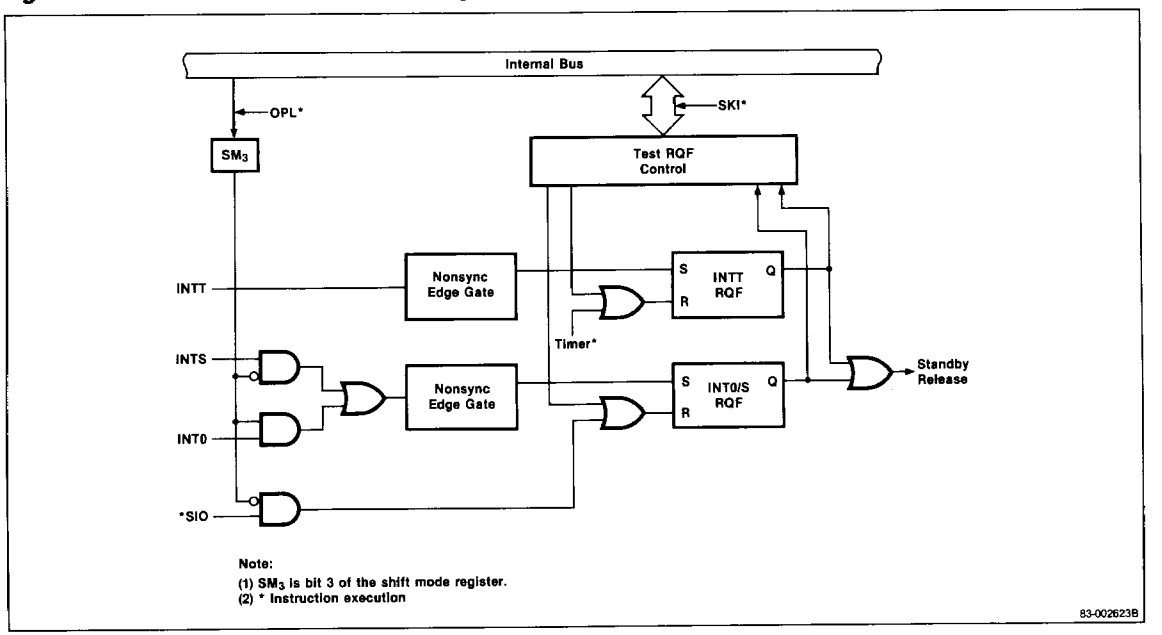


Figure 13. Test Control Circuit Block Diagram



Standby Modes

The μPD7554/54A/64/64A has two standby modes to reduce power consumption while the program is in the wait state. The STOP and HALT instructions set these modes.

When the program enters a standby mode, program execution stops and the contents of all registers and data memory immediately before the program entered standby mode are retained. The timer and serial interface can operate.

The RESET signal and STANDBY Release signal(1) release STOP mode. HALT mode is released when one or both of the test request flags are set, or when the RESET signal is input. The program cannot enter a standby mode when a test request is being set, even if the STOP or HALT command is executed.

If there is some uncertainty about the state of the test request flags, execute the SKI instruction to reset them so the program can enter standby mode.

Table 4 compares STOP and HALT modes. The main difference is that STOP mode stops the system clock and HALT does not. Ceramic oscillation stops during STOP mode. The power consumed by the ceramic oscillator is the difference between the two modes. In STOP mode, data memory can be retained with a lower supply voltage.

Note: (1) Standby release signal for μPD7554/54A only.

Table 4. STOP and HALT Modes

Mode	CL	ϕ	$P0_0$	CPU	Timer	Released by
STOP	x	x	o	x	Δ	RESET input
HALT	o	x	o	x	o	INTT RQF INT0/S RQF RESET input

Notes:

(1) o: operates. x: stops.
Δ: operates depending on clock source. μPD7554/54A; if external clock is used, STOP instruction will not stop CL. In this case STOP mode acts as HALT mode.

Power-on Reset Circuit

Figure 14 shows a circuit example of the power-on reset circuit using a resistor and a capacitor. This is the simplest reset control circuit. Figure 15 shows the circuit with a pull-down resistor internally connected to RESET as a mask option.

μPD7554/54A/64/64A Applications

Figures 16 and 17 show examples of application circuits for the μPD7554/54A/64/64A.

Table 5 compares the features of the low-end products of the 7500 series devices.

Figure 14. Power-on Reset Circuit

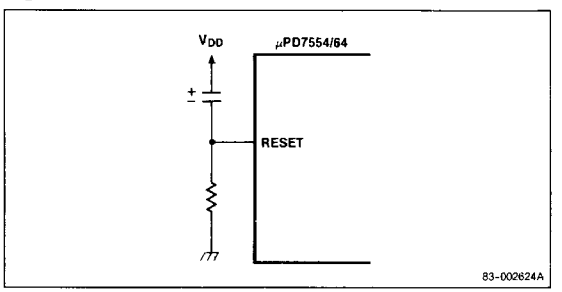


Figure 15. Power-on Reset Circuit with Pull-down Resistor

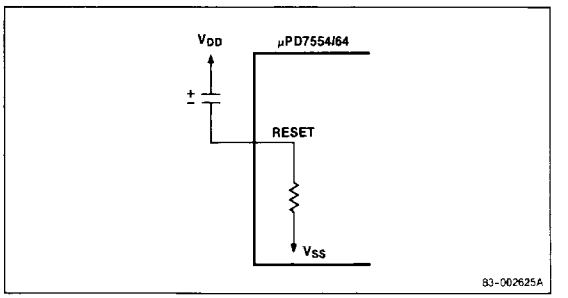
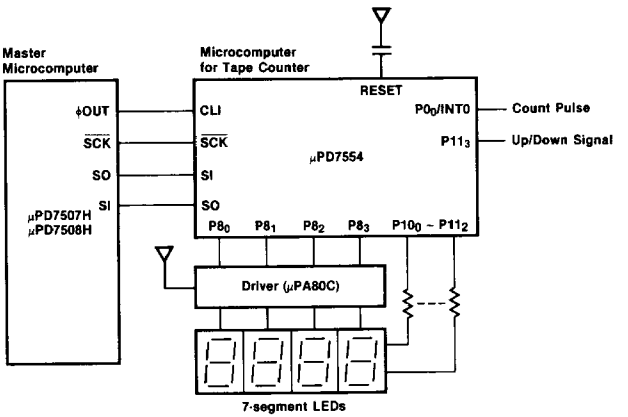


Table 5. Product Comparison

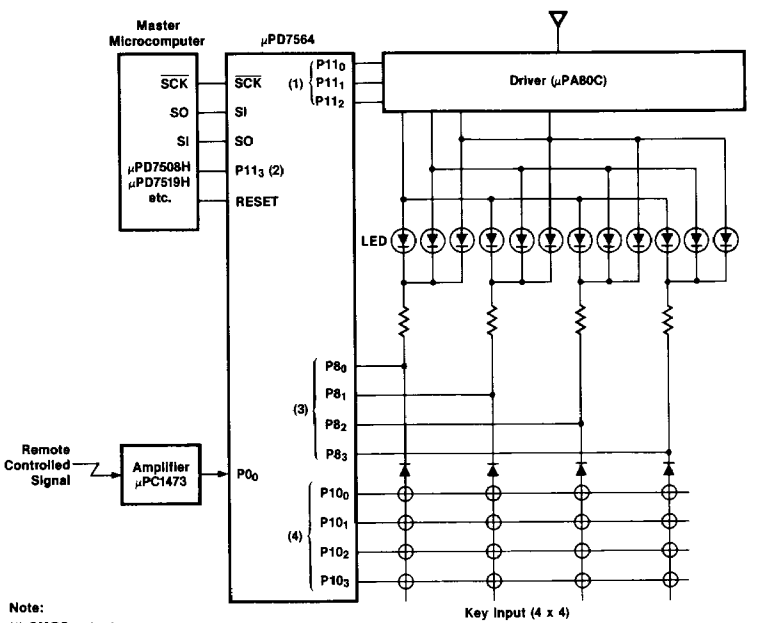
Item		μPD7554/54A	μPD7564/64A	μPD7556/56A	μPD7566/66A
Instruction cycle/system clock (5 V)	RC	4 μs/ 500 kHz		4 μs/ 500 kHz	
	External	2.86 μs/ 700 kHz		2.86 μs/ 700 kHz	
	Ceramic		3 μs/ 660 kHz		3 μs/ 660 kHz
Instruction set		47	47	45	45
ROM		1024 x 8	1024 x 8	1024 x 8	1024 x 8
RAM		64 x 4	64 x 4	64 x 4	64 x 4
I/O port total		16 (max)	15	20 (max)	19
Port 0		$P0_0$-$P0_3$	$P0_0$-$P0_3$	$P0_0$-$P0_1$	$P0_0$-$P0_1$
Port 1				$P1_0$-$P1_3$	$P0_1$-$P0_3$
Port 8		$P8_0$-$P8_2$ $P8_3$/CL2	$P8_0$-$P8_2$	$P8_0$-$P8_2$ $P8_3$/CL2	$P8_0$-$P8_2$
Port 9				$P9_0$-$P9_1$	$P9_0$-$P9_1$
Port 10		$P10_0$-$P10_3$	$P10_0$-$P10_3$	$P10_0$-$P10_3$	$P10_0$-$P10_3$
Port 11		$P11_0$-$P11_3$	$P11_0$-$P11_3$	$P11_0$-$P11_3$	$P11_0$-$P11_3$
Timer/Event counter		8-bit	8-bit	8-bit	8-bit
Serial interface		8-bit	8-bit		
Comparator				4-channel	4-channel
Process		CMOS	CMOS	CMOS	CMOS
Package		20-pin plastic SOP	20-pin plastic SOP	24-pin plastic SOP	24-pin plastic SOP
		20-pin shrink DIP	20-pin shrink DIP	24-pin shrink DIP	24-pin shrink DIP

Figure 16. Tape Counter Circuit



83-002626B

Figure 17. Remote-controlled Data Reception, Key Input and LED Display



Note:
(1) CMOS output
(2) Chip select or transfer request
(3) Open-drain output
(4) Input with internal pull-up resistor

83-002627B

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_I	
Except ports 10, 11	−0.3 to V_{DD} +0.3 V
Ports 10, 11 (Note 1)	−0.3 to V_{DD} +0.3 V
(Note 2)	−0.3 to +13 V
μPD7554A/64A only (Note 2)	−0.3 to +11 V
Output voltage, V_O	
Except ports 8, 10, 11	−0.3 to V_{DD} +0.3 V
Ports 8, 10, 11 (Note 1)	−0.3 to V_{DD} +0.3 V
(Note 2)	−0.3 to +13 V
μPD7554A/64A only (Note 2)	−0.3 V to +11 V
Output current, high I_{OH}	
One port	−5 mA
All output ports, total	−15 mA
Output current, low I_{OL}	
$P0_1$, $P0_2$	5 mA
Ports 9-11	15 mA
Port 8	30 mA
All ports, total	100 mA
Power dissipation, P_D (T_A = +70°C)	
Shrink DIP	480 mW
SOP	250 mW

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) CMOS I/O or N-channel open drain + internal pull up resistor.

(2) N-channel open drain I/O.

Capacitance

T_A = 25°C, V_{DD} = GND = 0 V; f = 1 MHz
Unmeasured pins returned to GND

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_I			15	pF	$P0_0$, $P0_3$
Output capacitance	C_O			35	pF	Port 8
I/O capacitance	$C_{I/O}$			35	pF	Ports 10, 11
				15	pF	$P0_1$, $P0_2$

DC Characteristics 1; V_{DD} = 2.5 to 3.3 V; μPD7554/54A

T_A = −10 to +70°C; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input high voltage except CL1	V_{IH1}	0.8 V_{DD}		V_{DD}	V	
Input high voltage CL1	V_{IH2}	V_{DD} − 0.3		V_{DD}	V	
Input high voltage ports 10, 11	V_{IH3}	0.8 V_{DD}		12 (Note 1); 9 (Note 2)	V	
Input high voltage RESET	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	Data retention mode
Input low voltage except CL1	V_{IL1}	0		0.2 V_{DD}	V	
Input low voltage CL1	V_{IL2}	0		0.3	V	
Input leakage current except CL1	I_{LI1}	−3		3	μA	$0 V \le V_I \le V_{DD}$
Input leakage current CL1	I_{LI2}	−10		10	μA	$0 V \le V_I \le V_{DD}$
Input leakage current ports 10, 11	I_{LI3}			10 (Note 1)	μA	V_I = 12 V
				10 (Note 2)	μA	V_I = 9 V
Output voltage high $P0_1$, $P0_2$, ports 8-11	V_{OH}	V_{DD} − 1.0			V	I_{OH} = −80 μA
Output voltage low $P0_1$, $P0_2$, ports 10, 11	V_{OL}			0.5	V	$P0_1$, $P0_2$: I_{OL} = 350 μA; Ports 10, 11: I_{OL} = 350 μA
Output voltage low port 8	V_{OL}			0.5	V	I_{OL} = 500 μA
Output leakage current	I_{LO1}	−3		3	μA	$0 V \le V_O \le V_{DD}$
Output leakage current ports 8-11	I_{LO2}			10 (Notes 1, 2)	μA	V_O = 12 V μPD7554; V_O = 9 V μPD7554A
Supply voltage, data retention mode	V_{DDDR}	2.0		6.0	V	
Supply current, normal operation; R oscillation (Note 3)	I_{DD1}		55	180	μA	V_{DD} = 3 V ±0.3 V; R = 150 kΩ ±2%
			40	150	μA	V_{DD} = 2.5 V; R = 150 kΩ ±2%
Supply current, HALT mode; R oscillation (Note 3)	I_{DD2}		25	80	μA	V_{DD} = 3 V ±0.3 V; R = 150 kΩ ±2%
			18	60	μA	V_{DD} = 2.5 V; R = 150 kΩ ±2%
Supply current, STOP mode (Note 3)	I_{DD3}		0.1	5	μA	
Supply current, data retention mode (Note 3)	I_{DDDR}		0.1	5	μA	V_{DDDR} = 2.0 V
Pull-up/down resistance, port 0, RESET	RP1	23.5	47	70.5	kΩ	
Pull-up resistance, ports 8-11	RP2	7.5	15	22.5	kΩ	

Notes:

(1) N-channel, open drain I/O ports, μPD7554.

(2) N-channel, open drain I/O ports, μPD7554A.

(3) Current in built-in pull-up/down resistors excluded.

DC Characteristics 2; V_{DD} = 2.7 to 6.0 V; μPD7554/54A/64/64A

T_A = −10 to +70°C; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input high voltage except CL1	V_{IH1}	0.7 V_{DD}		V_{DD}	V	
Input high voltage CL1 (Note 2)	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	
Input high voltage ports 10, 11	V_{IH3}	0.7 V_{DD}		12 (Note 1); 9 (Note 2)	V	
Input high voltage RESET	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	Data retention mode
Input low voltage except CL1 (Note 3)	V_{IL1}	0		0.3 V_{DD}	V	
Input low voltage CL1	V_{IL2}	0		0.5	V	
Input leakage current except CL1 (Note 3)	I_{LI1}	−3		3	μA	0 V ≤ V_I ≤ V_{DD}
Input leakage current CL1	I_{LI2}	−10		10	μA	0 V ≤ V_I ≤ V_{DD}
Input leakage current ports 10, 11 (Note 4)	I_{LI3}			10	μA	V_I = 9 V (7554A); or 12 V
Output voltage high $P0_1$, $P0_2$, ports 8-11	I_{OH}	V_{DD} − 2.0			V	V_{DD} = 4.5 to 6.0 V; I_{OH} = −1 mA
	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 2.7 V; I_{OH} = −100 μA
Output voltage low $P0_1$, $P0_2$	V_{OL}			0.4	V	V_{DD} = 4.5 to 6.0 V; I_{OL} = 1.6 mA
				0.5	V	I_{OL} = 400 μA
Output voltage low ports 10, 11	V_{OL}			0.4	V	V_{DD} = 4.5 to 6.0 V; I_{OL} = 1.6 mA
				2.0	V	V_{DD} = 4.5 to 6.0 V; I_{OL} = 10 mA
				0.5	V	I_{OL} = 400 μA
Output voltage low port 8	V_{OL}			2.0	V	V_{DD} = 4.5 to 6.0 V; I_{OL} = 15 mA
				0.5	V	I_{OL} = 600 μA
Output leakage current	I_{LO1}	−3		3	μA	0 V ≤ V_O ≤ V_{DD}
Output leakage current, port 8-11 (Note 4)	I_{LO2}			10	μA	V_O = 12 V μPD7554/64; V_O = 9 V μPD7554A/64A
Supply voltage, data retention mode	V_{DDDR}	2.0		6.0	V	
Supply current, normal operation; ceramic oscillation (Notes 3, 5)	I_{DD1}		650	2200	μA	V_{DD} = 5 V ±0.5 V; f_{CC} = 700 kHz
			120	360	μA	V_{DD} = 3 V ±10%; f_{CC} = 300 kHz
Supply current, normal operation; R oscillation (Note 3)	I_{DD1}		270	900	μA	V_{DD} = 5 V ±0.5 V; R = 56 kΩ ±2%
			80	240	μA	V_{DD} = 3 V ±10%; R = 100 kΩ ±2%
Supply current, HALT mode; ceramic oscillation (Notes 3, 5)	I_{DD2}		450	1500	μA	V_{DD} = 5 V ±0.5 V; f_{CC} = 700 kHz
			65	200	μA	V_{DD} = 3.0 V ±10%; f_{CC} = 300 kHz
Supply current, HALT mode; R oscillation (Note 3)	I_{DD2}		120	400	μA	V_{DD} = 5 V ±0.5 V; R = 56 kΩ ±2%
			35	110	μA	V_{DD} = 3 V ±10%; R = 100 kΩ ±2%
Supply current, STOP mode (Note 3)	I_{DD3}		0.1	10	μA	V_{DD} = 5 V ±0.5 V
			0.1	5	μA	V_{DD} = 3 V ±10%
Supply current, data retention mode (Note 3)	I_{DDDR}		0.1	5	μA	V_{DDDR} = 2.0 V
Pull-up/down resistance, port 0, RESET	RP1	23.5	47	70.5	kΩ	
Pull-up resistance, ports 8-11	RP2	7.5	15	22.5	kΩ	

Notes:

(1) μPD7554/64.

(2) μPD7554A/64A.

(3) Current in built-in pull-up/down resistors excluded.

(4) N-channel, open-drain I/O ports.

(5) μPD7564/64A.

DC Characteristics 3; V_{DD} = 2.0 to 3.3 V; μPD7554A only

T_A = −10 to +70°C; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input high voltage except CL1	V_{IH1}	0.8 V_{DD}		V_{DD}	V	
Input high voltage CL1	V_{IH2}	V_{DD} − 0.2		V_{DD}	V	
Input high voltage ports 10, 11	V_{IH3}	0.85 V_{DD}		9	V	
Input high voltage RESET	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	Data retention mode
Input low voltage except CL1	V_{IL1}	0		0.15 V_{DD}	V	
Input low voltage CL1	V_{IL2}	0		0.2	V	
Input leakage current except CL1	I_{LI1}	−3		3	μA	$0 V \le V_I \le V_{DD}$
Input leakage current CL1	I_{LI2}	−10		10	μA	$0 V \le V_I \le V_{DD}$
Input leakage current ports 10, 11 (Note 1)	I_{LI3}			10	μA	V_I = 9 V
Output voltage high PO_1, PO_2, ports 8-11	V_{OH}	V_{DD} − 1.0			V	I_{OH} = −70 μA
Output voltage low PO_1, PO_2, ports 10, 11	V_{OL}			0.5	V	PO_1, PO_2: I_{OL} = 270 μA Ports 10, 11: I_{OL} = 300 μA
Output voltage low port 8	V_{OL}			0.5	V	I_{OL} = 400 μA
Output leakage current	I_{LO1}	−3		3	μA	$0 V \le V_O \le V_{DD}$
Output leakage current ports 8-11 (Note 1)	I_{LO2}			10	μA	V_O = 9 V
Supply voltage, data retention mode	V_{DDDR}	2.0		6.0	V	
Supply current, normal operation; R oscillation (Note 2)	I_{DD1}		38	130	μA	V_{DD} = 3.0 V ±10%; R = 240 kΩ ±2%
			20	70	μA	V_{DD} = 2.0 V; R = 240 kΩ ±2%
Supply current, HALT mode; R oscillation (Note 2)	I_{DD2}		17	60	μA	V_{DD} = 3 V ±10%; R = 240 kΩ ±2%
			8	25	μA	V_{DD} = 2 V; R = 240 kΩ ±2%
Supply current, STOP mode (Note 2)	I_{DD3}		0.1	5	μA	
Supply current, data retention mode	I_{DDDR}		0.1	5	μA	V_{DDDR} = 2.0 V
Pull-up/down resistance, port 0, RESET	RP1	23.5	47	70.5	kΩ	
Pull-up resistance, ports 8-11	RP2	7.5	15	22.5	kΩ	

Notes:

(1) N-channel, open-drain I/O ports.

(2) Current in built-in pull-up/down resistors excluded.

3

AC Characteristics 1; V_{DD} = 2.5 to 3.3 V; μPD7554/54A

T_A = −10 to +70°C; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
System clock oscillation frequency	f_{CC}	140	180	220	kHz	R = 150 kΩ ±2%
System clock oscillation frequency, CL1, CL2	f_{CC}	140	175	210	kHz	V_{DD} = 2.5 V; R = 150 kΩ ±2%
External clock frequency, CL1	f_C	10		250	kHz	50% duty
System clock rise time, CL1	t_{CR}			200	ns	
System clock fall time, CL1	t_{CF}			200	ns	
System clock pulse width, high	t_{CH}	2		50	μs	
System clock pulse width, low	t_{CL}	2		50	μs	
External clock frequency ($P0_0$)	f_{P00}	0		250	kHz	50% duty
$P0_0$ rise time	t_{CRP00}			200	ns	
$P0_0$ fall time	t_{CFP0}			200	ns	
$P0_0$ pulse width, high	t_{P00H}	2			μs	
$P0_0$ pulse width, low	t_{P00L}	2			μs	
INT0 high time	t_{I0H}	30			μs	
INT0 low time	t_{I0L}	30			μs	
RESET high time	t_{RSH}	30			μs	
RESET low time	t_{RSL}	30			μs	
RESET setup time	t_{SRS}	0			μs	
RESET hold time	t_{HRS}	0			μs	
$\overline{SCK}$ cycle time	t_{KCY}	8.0			μs	Input
		10.0			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	4.0			μs	Input
$\overline{SCK}$ pulse width, low	t_{KL}	5.0			μs	Output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	0.3			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	0.3			μs	
SO output delay time after $\overline{SCK}$ ↑	t_{KSO}			2.0	μs	C_{OUT} = 100 pF max

AC Characteristics 2; V_{DD} = 2.7 to 6.0 V; μPD7554/54A/64/64A

T_A = −10 to +70°C; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
System clock oscillation frequency (Note 1)	f_{CC}	400	500	600	kHz	V_{DD} = 4.5 to 6.0 V; R = 56 kΩ ±2%
		200	250	300	kHz	V_{DD} = 3 V ±10%; R = 100 kΩ ±2%
External clock frequency, CL1	f_C	10		710	kHz	V_{DD} = 4.5 to 6.0 V; 50% duty
		10		350	kHz	V_{DD} = 2.7 V; 50% duty
System clock oscillation frequency (Note 2)	f_{CC}	290	700	710	kHz	V_{DD} = 4.5 to 6.0V
		290	500	510	kHz	V_{DD} = 4.0 to 6.0 V
		290	400	410	kHz	V_{DD} = 3.5 to 6.0 V
		290	300	310	kHz	V_{DD} = 2.7 to 6.0 V
Oscillation stabilization time	t_{OS}	20			ms	V_{DD} = 2.7 to 6.0 V
System clock rise time, CL1	t_{CR}			200	ns	
System clock fall time, CL1	t_{CF}			200	ns	
System clock pulse width	t_{CH}	0.7		50	μs	V_{DD} 4.5 to 6.0 V
System clock pulse width, CL1	t_{CL}	1.45		50	μs	V_{DD} = 2.7 V
External clock frequency ($P0_0$)	f_{P00}	0		710	kHz	V_{DD} = 4.5 to 6.0 V; 50% duty
		0		350	kHz	V_{DD} = 2.7 V; 50% duty
$P0_0$ rise time	t_{CRP00}			200	ns	
$P0_0$ fall time	t_{CFP0}			200	ns	
$P0_0$ pulse width, high	t_{P00H}	0.7			μs	V_{DD} = 4.5 to 6.0 V
$P0_0$ pulse width, low	t_{P00L}	1.45			μs	V_{DD} = 2.7 V
INT0 high time	t_{IOH}	10			μs	
INT0 low time	t_{IOL}	10			μs	
RESET high time	t_{RSH}	10			μs	
RESET low time	t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			μs	
RESET hold time	t_{HRS}	0			μs	
$\overline{SCK}$ cycle time	t_{KCY}	2.0			μs	Input; V_{DD} = 4.5 to 6.0 V
		2.5			μs	Output; ; V_{DD} = 4.5 to 6.0 V
		5.0			μs	Input; V_{DD} = 2.7 V
		5.7			μs	Output; ; V_{DD} = 2.7 V
$\overline{SCK}$ pulse width	t_{KH}	1.0			μs	Input; V_{DD} = 4.5 to 6.0 V
		1.25			μs	Output; V_{DD} = 4.5 to 6.0 V
$\overline{SCK}$ pulse width	t_{KL}	2.5			μs	Input; V_{DD} = 2.7 V
		2.85			μs	Output; V_{DD} = 2.7 V
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	0.1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	0.1			μs	
SO output delay time after $\overline{SCK}$ ↑	t_{KSO}			0.85	μs	V_{DD} = 4.5 to 6.0 V; C_{OUT} = 100 pF max
				1.2	μs	V_{DD} = 2.7 V; C_{OUT} = 100 pF max

Notes:

(1) μPD7554/54A.

(2) μPD7564/64A.

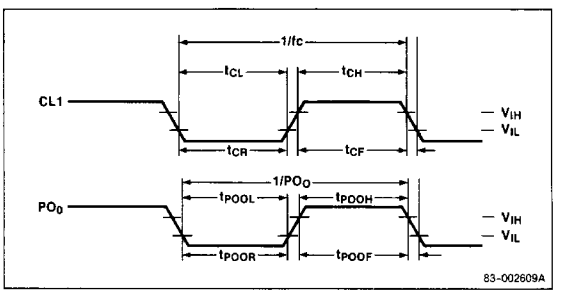
AC Characteristics 3; V_{DD} = 2.0 to 3.3 V; μPD7554A

T_A = −10 to +70°C; GND = 0 V

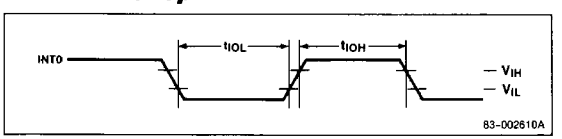
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
System clock oscillation frequency	f_{CC}	65	120	145	kHz	R = 240 kΩ ±2%
System clock oscillation frequency, CL1, CL2	f_{CC}	65	100	130	kHz	V_{DD} = 2.0 V; R = 240 kΩ ±2%
External clock frequency, CL1	f_C	10		150	kHz	
System clock rise time, CL1	t_{CR}			200	ns	
System clock fall time, CL1	t_{CF}			200	ns	
System clock pulse width, high	t_{CH}	3.3		50	μs	
System clock pulse width, low	t_{CL}	3.3		50	μs	
External clock frequency ($P0_0$)	f_{P00}	0		150	kHz	50% duty
$P0_0$ rise time	t_{CRP00}			200	ns	
$P0_0$ fall time	t_{CFP0}			200	ns	
$P0_0$ pulse width, high	t_{P00H}	3.3			μs	
$P0_0$ pulse width, low	t_{P00L}	3.3			μs	
INT0 high time	t_{IOH}	50			μs	
INT0 low time	t_{IOL}	50			μs	
RESET high time	t_{RSH}	50			μs	
RESET low time	t_{RSL}	50			μs	
RESET setup time	t_{SRS}	0			μs	
RESET hold time	t_{HRS}	0			μs	
$\overline{SCK}$ cycle time	t_{KCY}	13.4			μs	Input
		16.6			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	6.7			μs	Input
$\overline{SCK}$ pulse width, low	t_{KL}	8.3			μs	Output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	0.5			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	0.5			μs	
SO output delay time after $\overline{SCK}$ ↑	t_{KSO}			3.5	μs	C_{OUT} = 100 pF max

TIMING WAVEFORMS

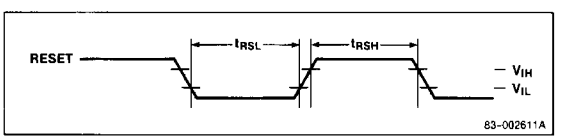
Clocks



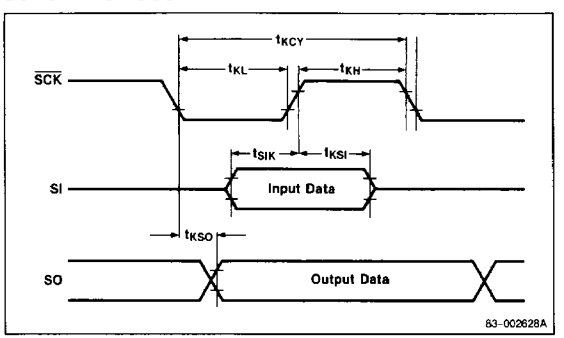
External Interrupt



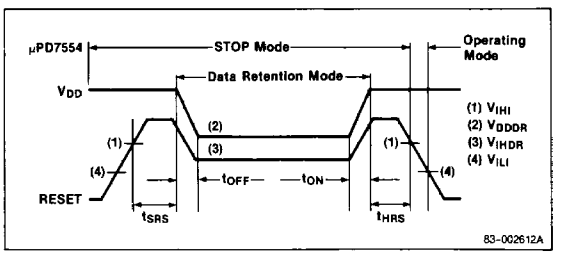
Reset



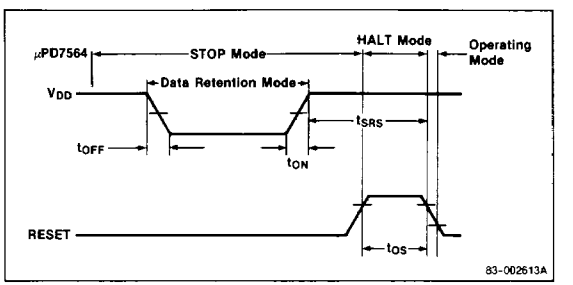
Serial Interface



Data Retention Mode, μPD7554/54A



Data Retention Mode, μPD7564/64A



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