

System Reset (with built-in watchdog timer) Monolithic IC MM1136

Outline

These ICs were developed to drive low voltage batteries, and have a watchdog timer with built-in microcomputer reset voltage detection circuit and low battery detection circuit.

A single reference voltage is used for low battery voltage detection and microcomputer reset voltage detection, so detection voltage difference is uniform ($\approx 0.2V$). Further, there is a built-in watchdog timer for operation diagnosis, which prevents the system from running wild by generating an intermittent reset pulse during system mis-operation.

Features

1. Accurate voltage drop detection voltage
 1. Low battery detection $3.4V \pm 3\%$
 2. Power supply voltage detection $3.2V \pm 3\%$
 3. Detection voltage error $0.2V \pm 20mV$ 1-2
 4. Hysteresis Both $50mV$ typ.
2. Watchdog function stop pin (can be made to function only as reset IC during V_{CC} rise)
3. Low current consumption $150\mu A$ typ.

Package

SOP-8C (MM1136XF)

Applications

1. 3V cordless telephones
2. Various types of small, handy equipment

Series Table

Model	V_{SLB}	V_{SLR}	T_{PR}	T_{WD}	T_{WR}
MM1136	3.4V	3.2V	100ms	100ms	2ms

* $C_T = 0.02\mu F$

T_{PR} : Reset hold time during V_{CC} rise

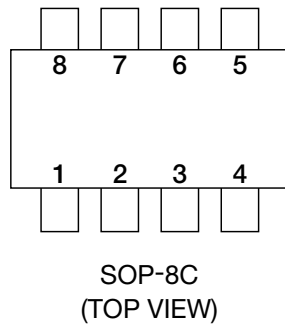
T_{WD} : Timer monitoring time

T_{WR} : Reset time

V_{SLB} : Battery check detection voltage

V_{SLR} : Reset detection voltage

Pin Assignment

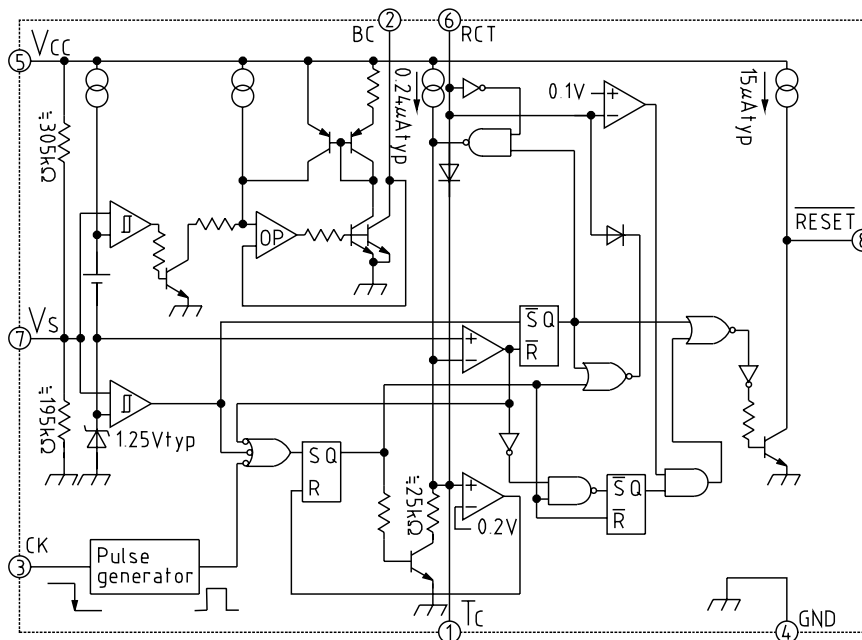


1	TC
2	BC (RESET)
3	CK
4	GND
5	V _{CC}
6	RCT
7	V _S
8	RESET

Pin Description

Pin No.	Pin name	Function
1	TC	T _{WD} , T _{WR} , T _{PR} time setting pins.
2	BC (RESET)	Battery check output pin (RESET low level output) for 3.4V
3	CK	Clock input pin
4	GND	GND pin
5	V _{CC}	Power supply voltage input pin
6	RCT	Watchdog timer stop pin Operation → OPEN, Stop → connect to GND
7	V _S	Detection voltage fine adjustment pin
8	RESET	Reset output pin (low output)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	$V_{CC \text{ max.}}$	-0.3~+7	V
Voltage applied to input pin	V_{IN}	-0.3~ $V_{CC}+0.3$ ($\leq +7$)	V
Voltage applied to output pin	V_{OUT}	-0.3~ $V_{CC}+0.3$ ($\leq +7$)	V
Allowable loss	P_d	450	mW
Storage temperature	T_{STG}	-40~+125	°C

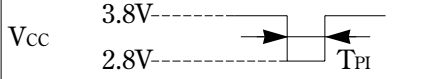
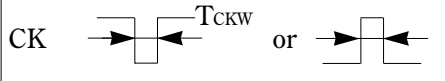
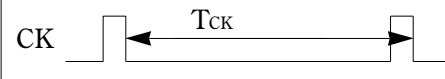
Recommended Operating Conditions

Item	Symbol	Rating	Units
Power supply voltage	V_{CC}	+2.5~+6.5	V
RESET sync current	I_{OLR}	0~1.5	mA
BC sync current	I_{OLC}	0~1.5	mA
Clock input high level voltage	V_{CKH}	1.4<	V
Clock input low level voltage	V_{CKL}	<0.4	V
Clock monitoring time setting	T_{WD}	1~1000	ms
Clock rise and fall times	t_{RCK}, t_{FCK}	<100	μs
Power supply voltage rise times	t_{RVCC}	100<	μs
Power supply voltage fall times	t_{FVCC}	50<	μs
TC pin capacitance	C_T	0.002~2	μF
Operating temperature	T_{OP}	-25~+75	°C

Electrical Characteristics

(Except where noted otherwise, Ta=25°C, Vcc=3.8V)
(Except where noted otherwise, resistance unit is Ω)

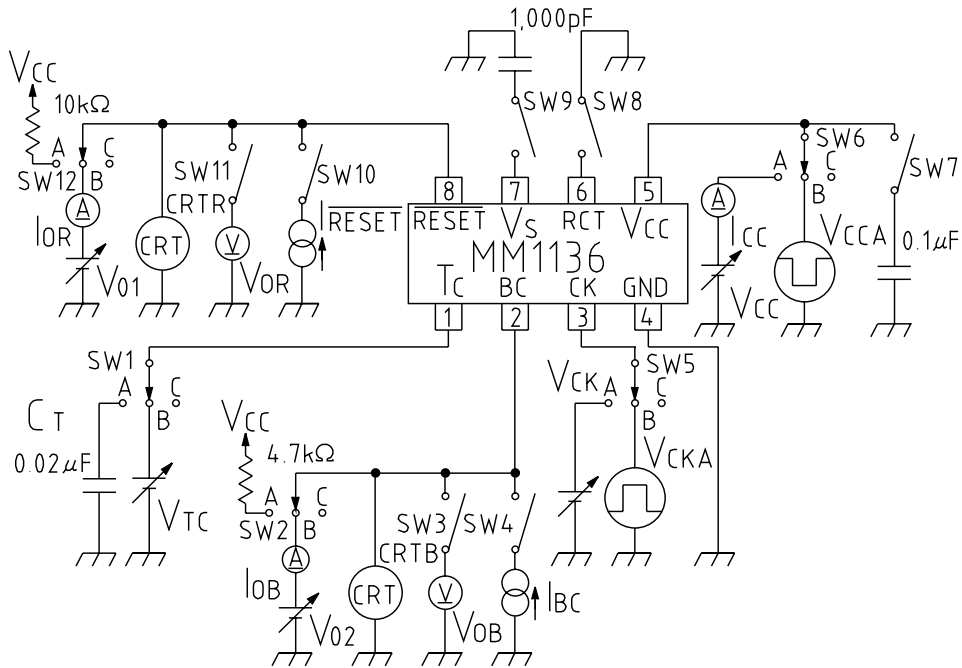
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current	I _{CC}	No load		200	280	μA
RESET detection voltage	V _{SLR}	V _{CC} : High→Low RCT : GND, V _{TC} =OPEN	3.10	3.20	3.30	V
Detection voltage temperature coefficient R	$\frac{\Delta V_{SR}}{\Delta T}$			±0.01	±0.05	%/°C
Hysteresis voltage R	V _{HYSR}	V _{CC} : Low→High RCT : GND, V _{TC} =OPEN	25	50	100	mV
BC detection voltage	V _{SLB}	V _{CC} : High→Low, R _{LB} =10k	3.30	3.40	3.50	V
Detection voltage temperature coefficient B	$\frac{\Delta V_{SB}}{\Delta T}$			±0.01	±0.05	%/°C
Hysteresis voltage B	V _{HYSB}	V _{CC} : Low→High, R _{LB} =10k	25	50	100	mV
Detection voltage difference	ΔV_{SL}	$\Delta V_{SL}=V_{SLB}-V_{SLR}$	0.18	0.20	0.22	V
CK input threshold	V _{TH}		0.8	1.2	2	V
CK input current	I _{IH}	V _{CK} =3.8V		0	1	μA
	I _{IL}	V _{CK} =0.0V	-15	-6	-2	
Output voltage RH	V _{OHR}	I _{RESET} =-5μA	3.0	3.4		V
Output voltage BH	V _{OHB}	R _{LB} =10k	3.2	3.6		V
Output voltage RL	V _{OLR}	I _{RESET} =1mA, V _{CC} =3.0V		0.3	0.5	V
Output voltage BL	V _{OLB}	I _{BC} =5mA, V _{CC} =3.0V		0.3	0.5	V
Output sync current R	I _{OLR}	V _{RESET} =0.5V, V _{CC} =3.0V	1	2		mA
Output sync current B	I _{OLB}	V _{BC} =0.5V, V _{CC} =3.0V	5	10		mA
Output source current R	I _{OHR}	V _{RESET} =3.4V	8	15		μA
C _T charge current	I _{CT1}	V _{TC} =1.0V during watchdog timer operation	-0.48	-0.24	-0.16	μA
	I _{CT2}	V _{TC} =1.0V during power ON reset operation	-0.48	-0.24	-0.16	μA
Minimum operating power supply voltage to ensure RESET	V _{CC}	V _{RESET} =0.4V I _{RESET} =0.1mA		0.8	1.0	V

V _{CC} input pulse width	T _{PI}		8			μs
CK input pulse width	T _{CKW}		3			μs
CK input cycle	T _{CK}		20			μs
Watchdog timer monitoring time *1	T _{WD}	C _T =0.02μF	50	100	150	ms
Watchdog timer reset time *2	T _{WR}	C _T =0.02μF	1	2	3	ms
Reset hold time for power supply rise *3	T _{PR}	C _T =0.02μF	50	100	150	ms
RESET delay time	t _{PDR}	V _{CC} : High → Low, R _{LR} =10k, C _{LR} =15pF		10		μs
BC delay time	t _{PDB}	V _{CC} : High → Low, R _{LB} =4.7k, C _{LB} =15pF		10		μs
RESET rise time	t _{RR}	R _{LR} =10k, C _{LR} =15pF		10		μs
RESET fall time	t _{FR}	R _{LR} =10k, C _{LR} =15pF		2		μs
BC rise time	t _{RB}	R _{LB} =4.7k, C _{LB} =15pF		10		μs
BC fall time	t _{FB}	R _{LB} =4.7k, C _{LB} =15pF		2		μs

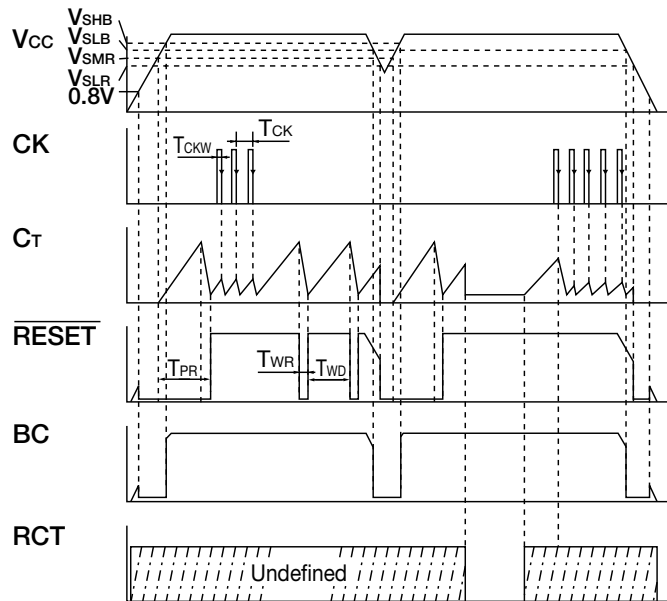
Notes:

- *1 Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse until reset pulse output.
In other words, reset output is output if a clock pulse is not input during this time.
- *2 Reset time means reset pulse width. However, this does not apply to power ON reset.
- *3 Reset hold time is the time from when V_{CC} exceeds detection voltage (V_{SHR}) during power ON reset until reset release (RESET output high).
- *4 Watchdog timer monitoring time (T_{WD}), watchdog timer reset time (T_{WR}) and reset hold time (T_{PR}) during power supply rise can be changed by varying C_T capacitance. The times are expressed by the following formulae.
 $T_{PR} (ms) \approx 5000 \times C_T (\mu F)$
 $T_{WD} (ms) \approx 5000 \times C_T (\mu F)$
 $T_{WR} (ms) \approx 100 \times C_T (\mu F)$
 Example : When C_T=0.02μF
 $T_{PR} \approx 100ms$
 $T_{WD} \approx 100ms$
 $T_{WR} \approx 2ms$
- *5 T_{WD} can be varied by placing a resistor (1MEGΩ or more) between the RCT pin and V_{CC}.
- *6 The voltage range when measuring output rise and fall time is 10~90%.
- *7 V_{CC} rise time should be 100μs or more, and fall time should be 50μs or more.

Measuring Circuit



Timing Chart



Basic Circuit Diagram

