

Lithium Ion Battery Protection (for 1-cell in series) Monolithic IC MM1446

Outline

This IC is a lithium ion battery protection IC that adds control using a fuse to the method of overcurrent detection control used in the familiar MM1301 series. An OSI pin (charge control pin) also has been provided.

1-Cell Protection ICs

Temperature conditions A : Ta=25 ~ 75°C, B : Ta=-20 ~ 70°C, C : Ta=0 ~ 50°C,
D : Ta=0 ~ 40°C, E : Ta=-20 ~ 25°C

Model	Package	Overcharge detection voltage (V)	Overcharge detection voltage temperature conditions	Overcharge detection hysteresis voltage (V)	Overdischarge detection voltage (V)	Overdischarge resumption voltage (V)	Overcurrent detection voltage (mV)
	VSOP-8B						
MM1446	BW	4.270±0.030	C	100±30	2.55±0.05	3.70	39.0±4.5
	CW	4.270±0.030	C	100±30	2.55±0.05	3.70	52.0±4.5
	DW	4.180±0.030	C	110±30	2.50±0.05	3.10±0.078	39.0±4.5
	EW	4.280±0.030	C	110±30	2.50±0.05	3.10±0.078	39.0±4.5

* The series will continue to be expanded.

* Overcharge and overdischarge voltages and overcurrent detection voltage can be changed at the customer's request.

Features

- Overcharge detection voltage Ta = 0 ~ +50°C V_{CEL} ±30mV
- Overcharge detection dead time C_{TD} = 0.1µF 1.0 sec
- Consumption current (normal mode V_{CEL} = 3.5V) 14µA typ.
- Consumption current (overdischarge mode V_{CEL} = 1.9V) 0.2µA typ.
- Overcurrent protection release Load open: between both ends of battery pack load of 500MΩ or higher

Package

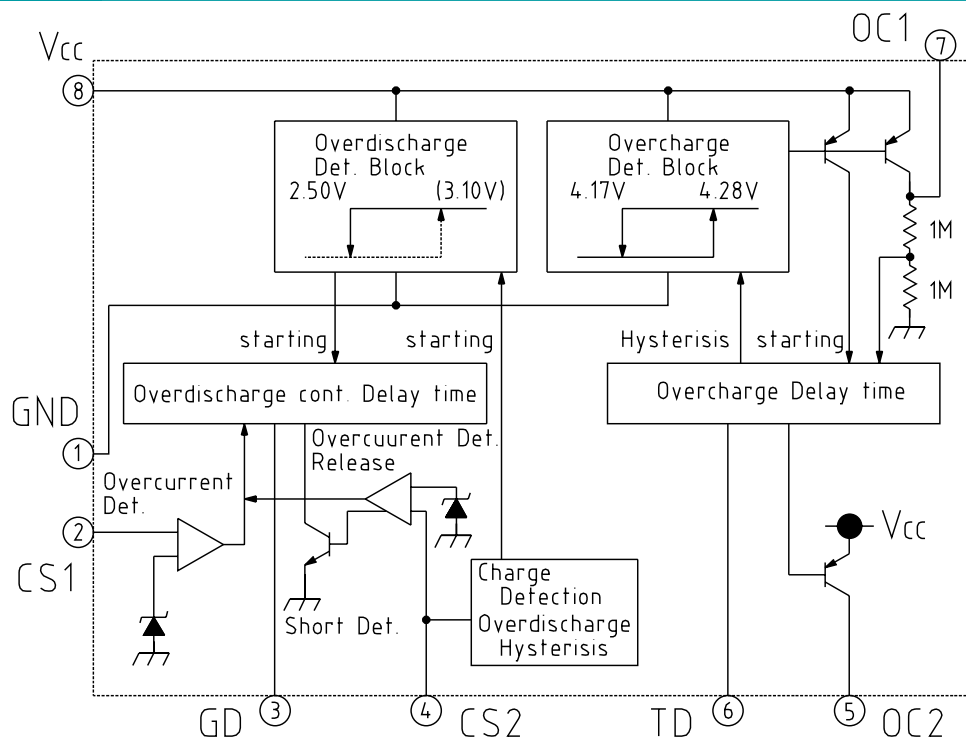
VSOP-8B

Applications

Lithium ion battery packs (for battery protection)



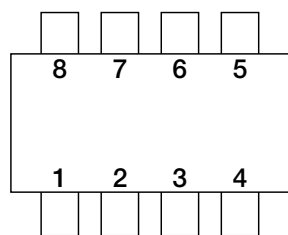
Block Diagram



*1: Over-discharge detection voltage

*2: Over-charge detection voltage

Pin Assignment



SOP-8B

1	GND
2	CS1
3	GD
4	CS2
5	OC2
6	TD
7	OC1
8	Vcc

Pin Description

PIN No.	PIN Name	Function
1	GND	Negative power supply for this IC. Also act as detection voltage pin for the battery connected between Vcc-GND.
2	CS1	Detection pin for voltage between CS1-GND. When CS1 is connected with the Source of discharge FET, Detects overcurrent using an external resistor and discharge current. When CS1 is connected with CS2(4PIN), and connects with the Dorein of charge and discharge FET, Detects overcurrent using an On state resistor of discharge control FET and discharge current. Discharge Current=CS1-GND Voltage / External Resistor CS1-GND Voltage / On state resistance of discharge control FET
3	GD	N-ch FET gate connection pin for discharge control. Switchesgate OFF when overdischarge is detected, and for current protection. Swiches gate ON when overcharge is detected, and in normal state.
4	CS2	Detection pin for overcurrent mode release and start-up voltage. Detected load release resets from overcurrent mode. When the battery is being charged and the Voltage between CS2-GND during overdischarge mode falls bellow start-up voltage, the bias current is drained to the interior circuit and operating status result.
5	OC2	Control pin for N-ch FET for charge control. Switches FET OFF by activating an external transistor when overcharge is detected. This operation continues until the voltage falls bellow overcharge release voltage.
6	TD	Overcharge detection dead time setting pin. $T_{ARAM} \approx 10.0 \times C_{TD}$ (sec) C_{TD} : TD pin external capacitance value (μF)
7	OC1	Overcharge detection output (input) pin. For overcharge detection, output goes high without dead time set by TD pin. (Hysteresis does not go on until OC2 output goes high.) Charging control FET is turned off by the OC2 pin when OC1 pin input is high.
8	Vcc	Positive power supply for this IC. Also act as detection voltage pin for the battery connected between Vcc-GND.

Overcharge Mode : Battery Voltage > Overcharge Det. Voltage

Nomal Mode : Overdischarge Det. Voltage < Battery Voltage < Overcharge Det. Voltage

Discharge Current < Overcurrent Det. Voltage / External Det. resistor

Overdischarge Mode : Overdischarge Det. Voltage > Battery Voltage

Overcurrent Mode : Discharge Current > Overcurrent Det. Voltage / External Det. Resistor

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+70	°C
Supply voltage	V _{CC} max.	-0.3~+12	V
OC1 Terminal Voltage CS1 Terminal Voltage	V _{OC1} max. V _{CS1} max.	-0.3~V _{CC}	V
OC2 Terminal Voltage CS2 Terminal Voltage	V _{OC2} max. V _{CS2} max.	-0.6~V _{CC}	V
Allowable loss	P _D	170 (Alone)	mW

Recommended Operating Conditions

Item	Symbol	Ratings	Unit
Operating Temperature	T _{OPR}	-20~+70	°C
Supply Voltage	V _{OP}	+0.9~+12	V

Electrical Characteristics (Unless otherwise specified Ta=25°C, model name MM1446E)

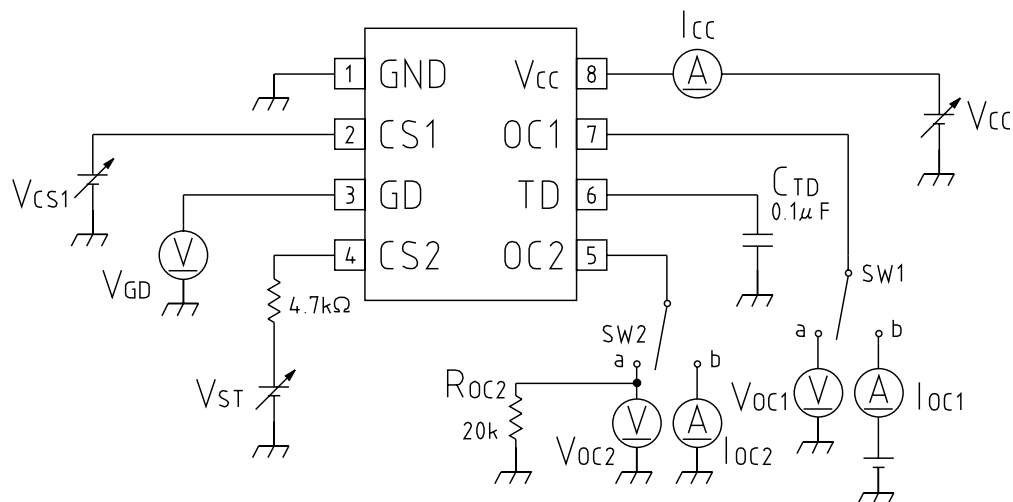
Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Current Consumption 1 (Overcharge Mode)	I _{CC1}	V _{CC} =4.5V R _{OC1} , R _{OC2} =∞		150	250	μA
Current Consumption 2 (Nomal Mode)	I _{CC2}	V _{CC} =3.5V		14	20	μA
Current Consumption 3 (Overdischarge Mode)	I _{CC3}	V _{CC} =1.9V		0.2	0.5	μA
Current Consumption 4 (Overdischarge Mode)	I _{CC4}	V _{CC} =1.9V (Ta=70°C)		0.5	0.8	μA
Current Cosumption 5 (OC1 Output)	I _{CC5}	V _{CC} =4.5V, V _{TD} =0V R _{OC1} =∞		45		μA
Overcharge Detection Voltage	V _{ALM}	Ta=0°C ~ 50°C V _{CC} =4.0V→4.5V, V _{OC1, 2} : L→H	4.250	4.280	4.310	V
Overcharge Release Voltage	V _{ALML}	V _{CC} =4.5V→4.0V, V _{OC1, 2} : H→L	4.120	4.170	4.220	V
Overcharge Hysteresis Voltage	ΔV _{ALM}	V _{ALM} -V _{ALML}	80	110	140	mV
Overdischarge Detection Voltage	V _{OD}	V _{CC} =3.0V→2.0V V _{GD} : H→L	2.45	2.50	2.55	V
Overdischarge Resumption Voltage	V _{ODF}	V _{CC} =2.0V→4.0V V _{GD} : L→H	3.022	3.10	3.178	V
		(*1) (V _{CC} >Overdischarge Release Voltage) or (Charge and V _{CC} >Overdischarge detection voltage.)				
Start-up Voltage	V _{ST}	V _{CC} =2.7V V _{CS2} : 0V→-0.5V, V _{GD} : L→H	-0.4	-0.1		V
Overcurrent Detection Voltage	V _{CS1}	V _{CS1} : 0V→-0.2V, V _{GD} : H→L	34.5	39.5	43.5	mV
Overcurrent Protection Release		Load release (500MEGΩ min.)				

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Overdischarge Detection Delay Time	t_{OD}	$V_{CC}=3.0V \rightarrow 2.0V$ (*1), $V_{GD} : H \rightarrow L$ CIRCUIT2, SW1 : a, SW2 : b, SW3 : b	5.0	10.0	15.0	ms
Overcurrent Detection Delay Time 1	t_{CS1}	$V_{CS1}=0V \rightarrow 0.2V$ (*1), $V_{GD} : H \rightarrow L$ CIRCUIT2, SW1 : a, SW2 : b, SW3 : b	5.0	10.0	15.0	ms
Overcurrent Detection Delay Time 2	t_{CS2}	$V_{CS2}=0V \rightarrow 1.0V$ (*1) , $V_{GD} : H \rightarrow L$ CIRCUIT2, SW1 : b, SW2 : a, SW3 : b			100	μs
Overcharge Detection Delay Time 1	t_{ALM1}	$V_{CC}=4.0V \rightarrow 4.5V$ (*1) , $C_{TD}=0.1\mu F$, $V_{OC2} : L \rightarrow H$ CIRCUIT2, SW1 : a, SW2 : b, SW3 : b	0.5	1.0	1.5	s
Overcharge Detection Delay Time 2	$\triangle t_{ALM2}$	$V_{CC}=4.0V \rightarrow 4.5V$ (*1) , $V_{OC1} : H \rightarrow L$ CIRCUIT2, SW1 : a, SW2 : b, SW3 : b			100	μs
Operating Limit Voltage (*2)	V_{OP}	V_{CC} when $V_{GDL2} > 0.4V$			1.2	V
GD Terminal Output Voltage H	V_{GDH}		$V_{CC}-0.3$	$V_{CC}-0.1$		V
GD Terminal Output Voltage L1	V_{GDL1}	$V_{CS2} > 1.0V$		0.1	0.3	V
GD Terminal Output Voltage L2	V_{GDL2}	$V_{CC}=1.5V$		0.2	0.4	V
OC1 Terminal Output Current	I_{OC1}	$V_{CC}=4.5V$, $V_{OC1}=1.6V$ CIRCUIT1, SW1 : b, SW2 : a			-30	μA
OC2 Terminal Output Current	I_{OC2}	$V_{CC}=4.5V$, $V_{OC1}=0V$ CIRCUIT1, SW1 : a, SW2 : b			-500	μA

(*1) Refer to input waveforms.

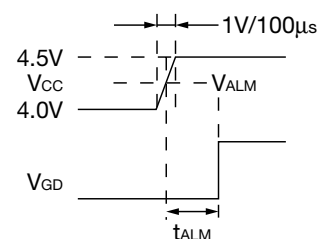
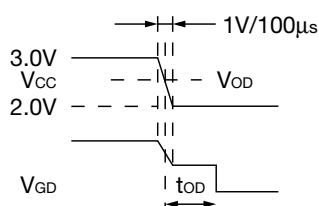
(*2) Operation is unstable below the operating limit voltage.

■ Measuring Circuit 1

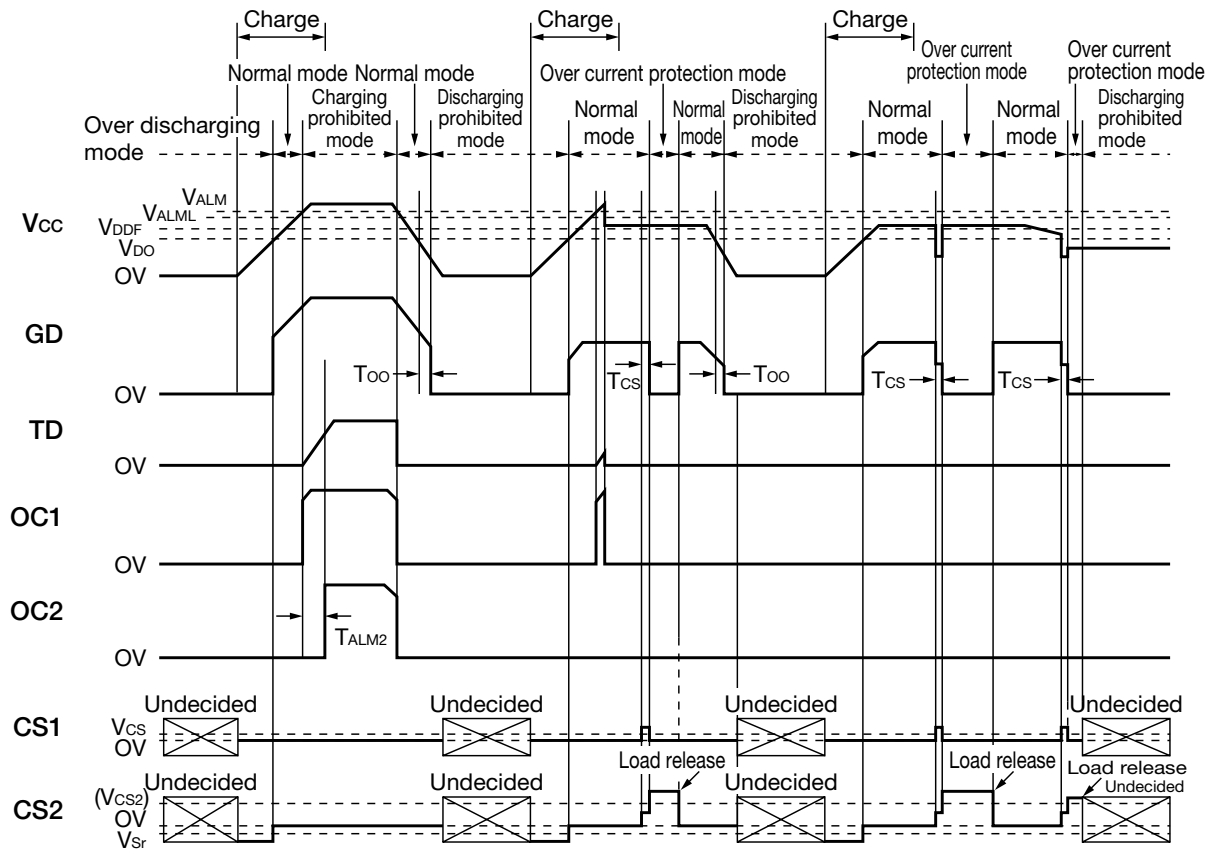


The diagram shows a 40106 hex inverter chip with the following connections:

- Pin 1 (GND):** Connected to ground.
- Pin 2 (CS1):** Connected to a square wave source labeled V_{CS1} through a switch $SW1$.
- Pin 3 (GD):** Connected to a square wave source labeled V_{CS2} through a switch $SW2$.
- Pin 4 (CS2):** Connected to ground through a $4.7k\Omega$ resistor.
- Pin 5 (OC2):** Connected to ground through a $20k$ resistor. A square wave source V_{CC} is connected to this node through a switch $SW3$.
- Pin 6 (TD):** Connected to ground through a $0.1\mu F$ capacitor.
- Pin 7 (OC1):** Connected to a square wave source labeled V_{CC} through a switch $SW3$.
- Pin 8 (V_{CC}):** Connected to a square wave source labeled V_{CC} through a switch $SW3$.

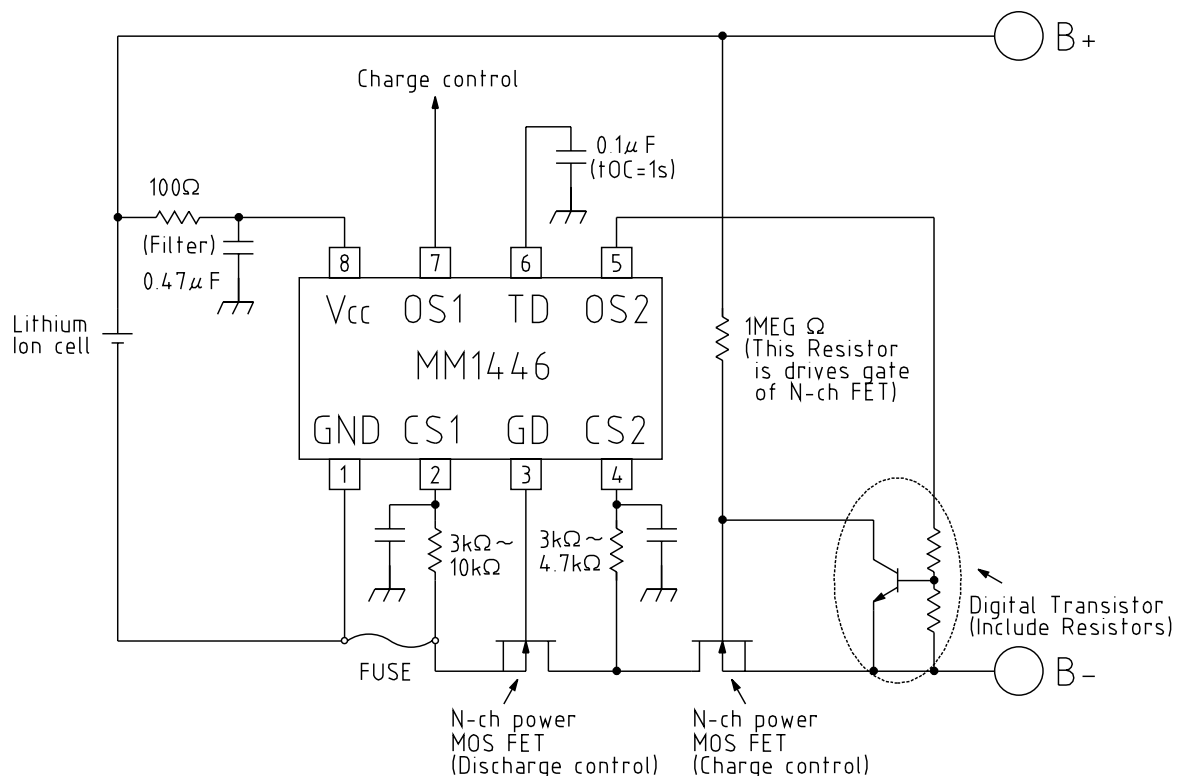


Timing Chart

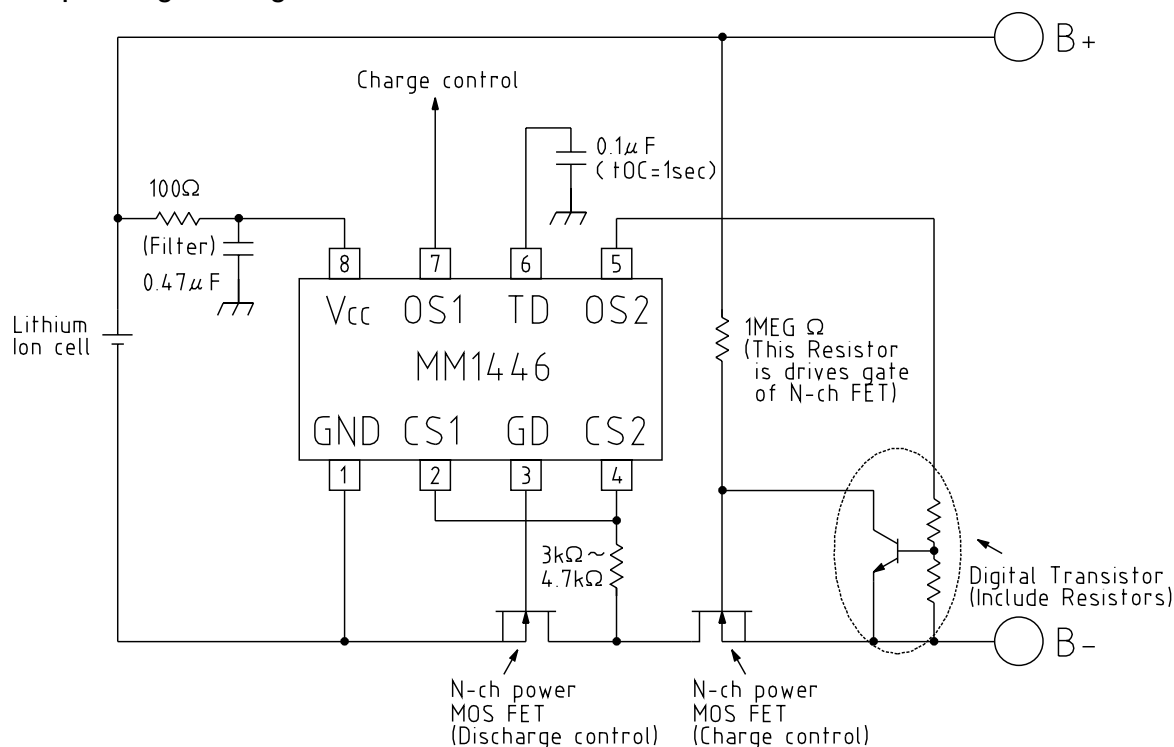


Application Circuits

(1) Example using shunt resistance to detect overcurrent.

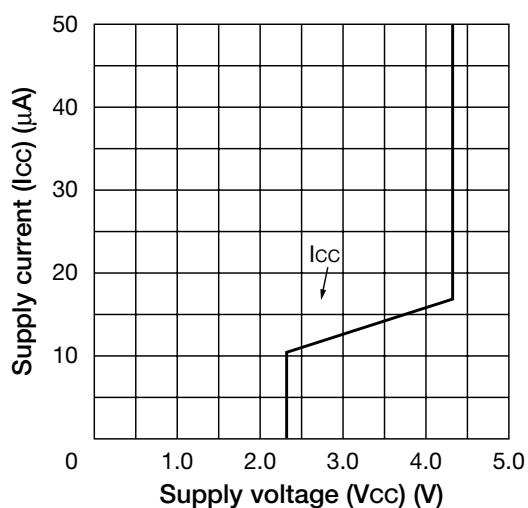


(2) Example using discharge FET on resistance to detect overcurrent.

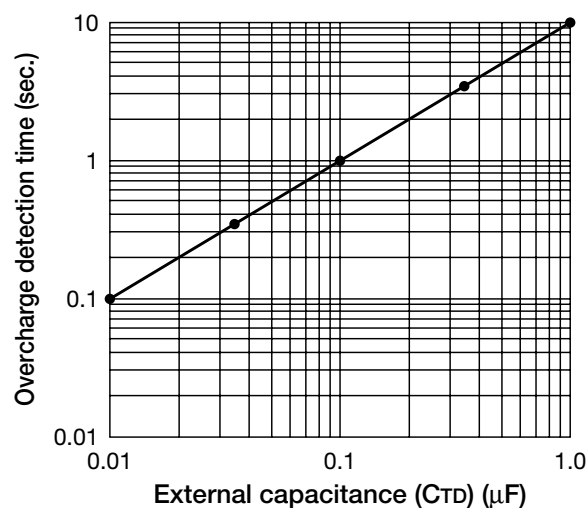


Note: Applicable circuits shown are typical examples provided for reference purposes. Mitsumi cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

■ Supply current vs supply voltage



■ Overcharge detection time (deat time)



Note: The above specifications are representative, and are not guaranteed values.