

CUS/MUS INTEGRATED CIRCUITS

7929225 S G S SEMICONDUCTOR CORP



DUAL UP-COUNTERS: HCC/HCF 4518B DUAL BCD UP-COUNTER HCC/HCF 4520B DUAL BINARY UP-COUNTER

- MEDIUM-SPEED OPERATION - 6 MHz TYP. CLOCK FREQUENCY AT 10V
- POSITIVE - OR NEGATIVE - EDGE TRIGGERING
- SYNCHRONOUS INTERNAL CARRY PROPAGATION
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The HCC 4518B/4520B (extended temperature range) and HCF 4518B/4520B (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The HCC/HCF 4518B Dual BCD Up Counter and HCC/HCF 4520B Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the Enable input is maintained "high" and the counter advances on each positive-going transition of the Clock. The counters are cleared by high levels on their Reset lines. The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the clock input of the latter is held low.

ABSOLUTE MAXIMUM RATINGS

V_{DD}^*	Supply voltage: HCC types HCF types	-0.5 to 20 -0.5 to 18 -0.5 to $V_{DD} + 0.5$	V V V
V_I	Input voltage	± 10	mA
I_I	DC input current (any one input)	200	mW
P_{tot}	Total power dissipation (per package) Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: HCC types HCF types	-55 to 125 -40 to 85	°C °C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

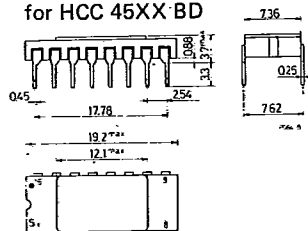
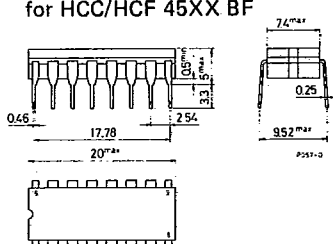
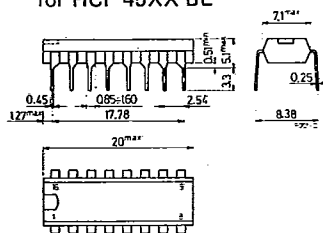
HCC 45XX BD for dual in-line ceramic package
HCC 45XX BF for dual in-line ceramic package, frit seal
HCC 45XX BK for ceramic flat package
HCF 45XX BE for dual in-line plastic package
HCF 45XX BF for dual in-line ceramic package, frit seal

T-45-23-05

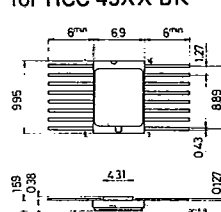
HCC/HCF 4518 B
HCC/HCF 4520 B

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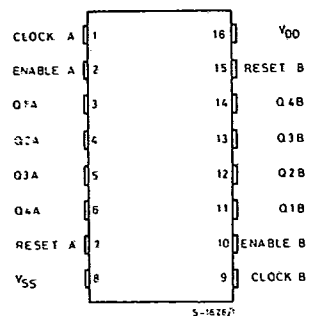
MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package
for HCC 45XX-BD 736Dual in-line ceramic package
for HCC/HCF 45XX BFDual in-line plastic package
for HCF 45XX BE

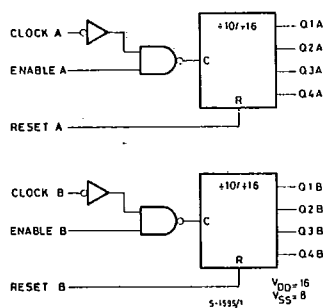
**Ceramic flat package
for HCC 45XX BK**



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: HCC types	3 to 18	V
	HCF types	3 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: HCC types	-55 to 125	°C
	HCF types	-40 to 85	°C

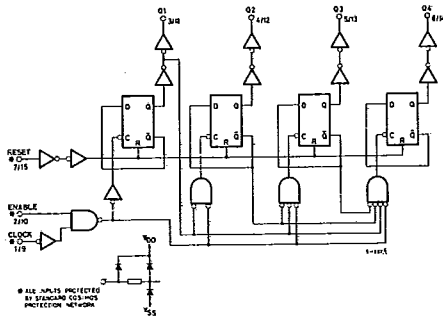
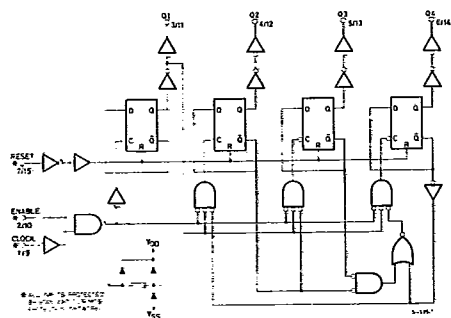
HCC/HCF 4518B
 HCC/HCF 4520B

T-45-23-05

LOGIC DIAGRAMS (for one of two identical counter)

Decade counter for 4518B

Binary counter for 4520B

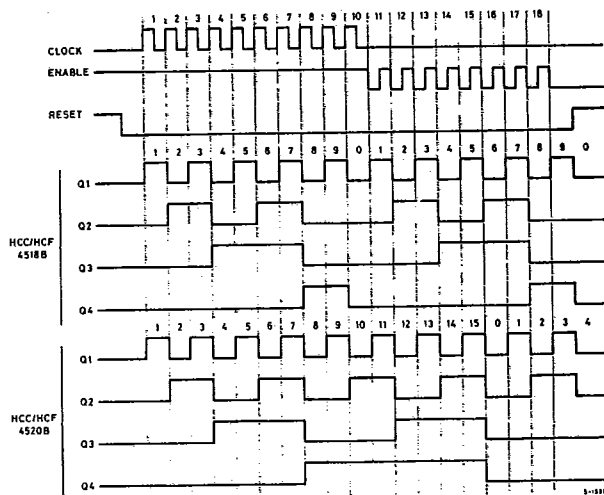


TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q1 thru Q4 = 0

X= Don't Care 1= High State 0= Low State

TIMING DIAGRAM



HCC/HCF 4518B
HCC/HCF 4520B

T-45-23-05

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values						Unit	
			V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{Low} *		25°C			T _{High} *		
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I _L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
	HCF types	0/ 5			5		20		0.04	20		150		
		0/10			10		40		0.04	40		300		
		0/15			15		80		0.04	80		600		
V _{OH}	Output high voltage	0/ 5		< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL}	Output low voltage	5/0		< 1	5		0.05			0.05		0.05	V	
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V _{IH}	Input high voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V _{IL}	Input low voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I _{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
	HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1			
		0/ 5	4.6		5	-0.52		-0.44	-1		-0.36			
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9			
I _{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
	HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36			
		0/10	0.5		10	1.3		1.1	2.6		0.9			
		0/15	1.5		15	3.6		3.0	6.8		2.4			
I _{IH} , I _{IL}	Input leakage current	HCC types	0/18	Any input	18		±0.1		±10 ⁻⁵	±0.1		± 1	μA	
		HCF types	0/15		15		±0.3		±10 ⁻⁵	±0.3		± 1		
C _I	Input capacitance			Any input					5	7.5			pF	

* T_{Low} = - 55°C for HCC device; -40°C for HCF device.* T_{High} = +125°C for HCC device; +85°C for HCF device.The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

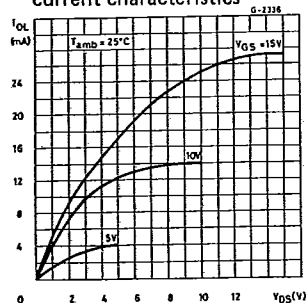


T-45-23-05

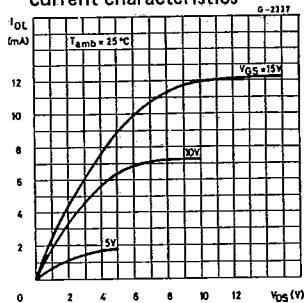
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$, typical temperature coefficient for all $V_{DD} = 0.3\%/^{\circ}\text{C}$ values, all input rise and fall time = 20 ns)

Parameter	Test conditions	Values				Unit
		$V_{DD} \text{ (V)}$	Min.	Typ.	Max.	
t_{PLH} , t_{PHL} Propagation delay time (Reset to output)		5		280	560	ns
		10		115	230	
		15		80	160	
t_{PLH} , t_{PHL} Propagation delay time (Clock or Enable to output)		5		330	650	ns
		10		130	225	
		15		90	170	
t_{TLH} , t_{THL} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	
t_W Clock pulse width		5	200	100		ns
		10	100	50		
		15	70	35		
t_W Reset pulse width		5	250	125		ns
		10	110	55		
		15	80	40		
t_W Enable pulse width		5	400	200		ns
		10	200	100		
		15	140	70		
t_r , t_f Clock or enable rise and fall time		5			15	μs
		10			15	
		15			5	
f_{max} Maximum clock frequency		5	1, 5	3		MHz
		10	3	6		
		15	4	8		
t_r , t_f Clock input rise or fall time		5			15	μs
		10			5	
		15			5	

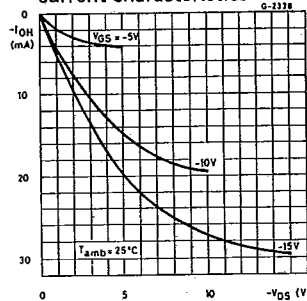
Typical output low (sink) current characteristics



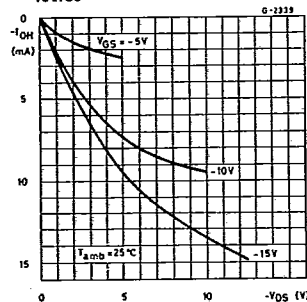
Minimum output low (sink) current characteristics



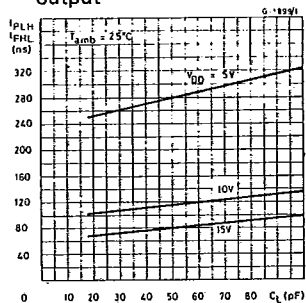
Typical output high (source) current characteristics



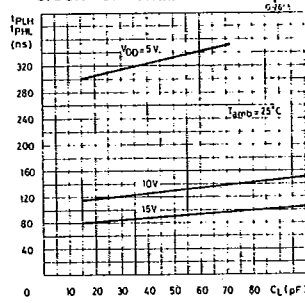
Minimum output high (source) current characteristics



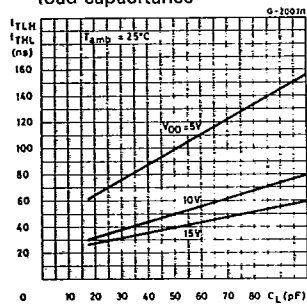
Typical propagation delay vs. load capacitance, reset to output



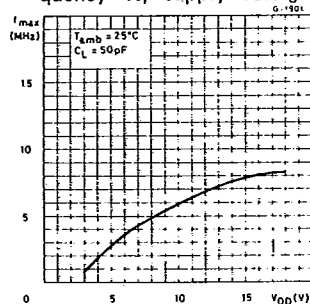
Typical propagation delay time vs. load capacitance, clock or enable to output



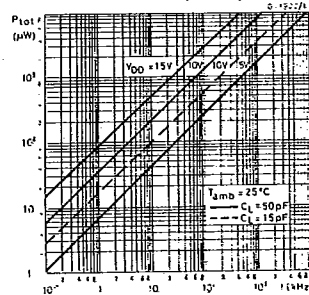
Typical transition time vs. load capacitance



Typical maximum-clock frequency vs. supply voltage



Typical power dissipation/counter vs. frequency

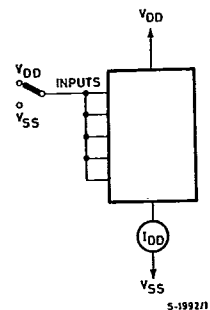




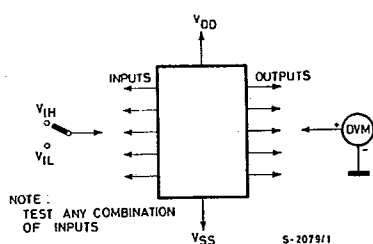
T-45-23-05

TEST CIRCUITS

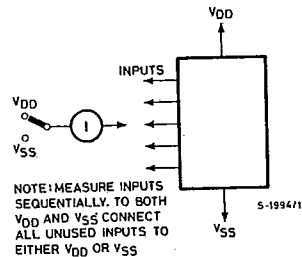
Quiescent device current



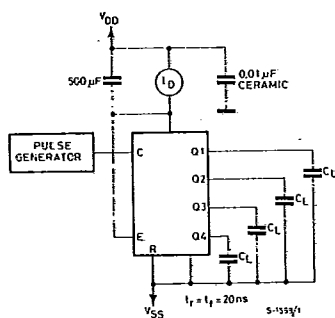
Noise immunity



Input leakage current

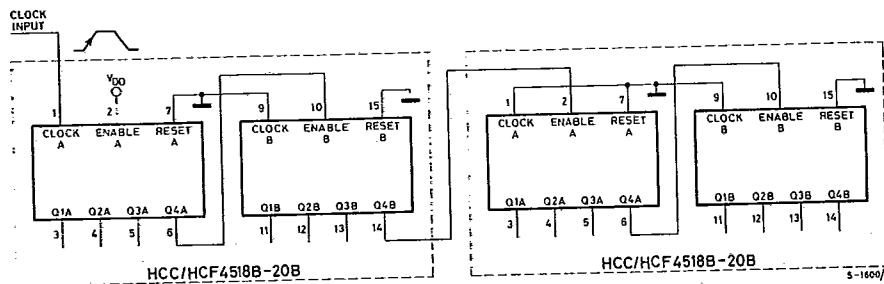


Dynamic power dissipation



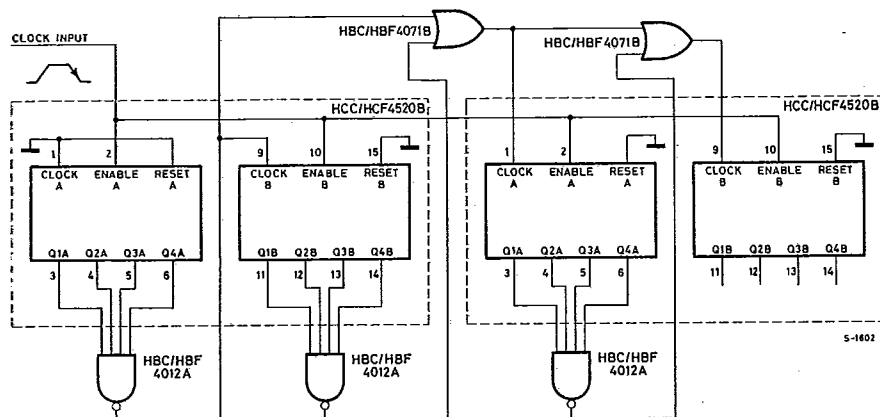
TYPICAL APPLICATIONS

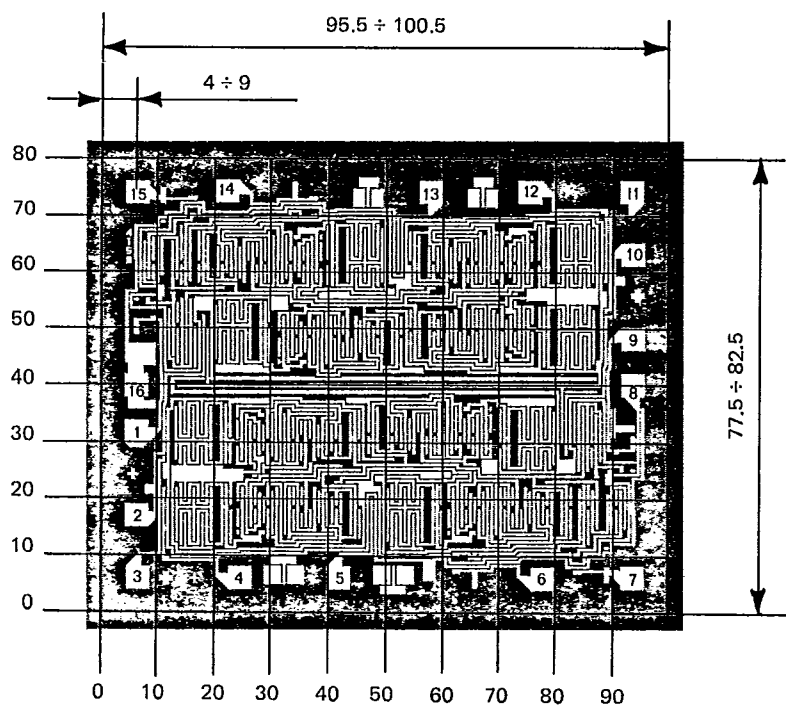
Ripple cascading of four counters with positive-edge triggering



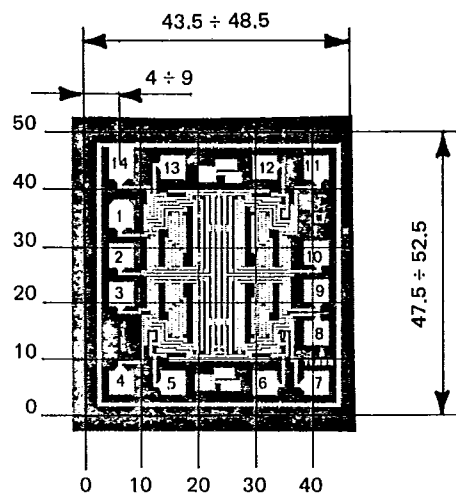
TYPICAL APPLICATIONS (continued)

Synchronous cascading of four binary counters with negative-edge triggering





4015B



4016B