TMS320LF2401A DSP CONTROLLER

SPRS161 – MARCH 2001

PRODUCT PREVIEW

- High-Performance Static CMOS Technology
  - 25-ns Instruction Cycle Time (40 MHz)
  - 40-MIPS Performance
  - Low-Power 3.3-V Design
- Based on TMS320C2xx DSP CPU Core
  - Code-Compatible With 240x and F243/F241/C242
  - Instruction Set Compatible With F240/C240
- On-Chip Memory
  - Up to 8K Words x 16 Bits of Flash EEPROM (2 Sectors)
  - Programmable “Code-Security” Feature for the On-Chip Flash
  - Up to 1K Words x 16 Bits of Data/Program RAM
    - 544 Words of Dual-Access RAM
    - Up to 512 Words of Single-Access RAM
- Boot ROM
  - SCI Bootloader
- Event-Manager (EV) Module (EVA), Which Includes:
  - Two 16-Bit General-Purpose Timers
  - Seven 16-Bit Pulse-Width Modulation (PWM) Channels Which Enable:
    - Three-Phase Inverter Control
    - Center- or Edge-Alignment of PWM Channels
    - Emergency PWM Channel Shutdown With External $\overline{\text{PDPINTA}}$ Pin
  - Programmable Deadband (Deadtime) Prevents Shoot-Through Faults
  - One Capture Unit For Time-Stamping of External Events
  - Input Qualifier for Select Pins
  - Synchronized A-to-D Conversion
  - Designed for AC Induction, BLDC, Switched Reluctance, and Stepper Motor Control
- Small Foot-Print (7 mm × 7 mm) Ideally Suited for Space-Constrained Applications
- Watchdog (WD) Timer Module
- 10-Bit Analog-to-Digital Converter (ADC)
  - 5 Multiplexed Input Channels
  - 500 ns Minimum Conversion Time
  - Selectable Twin 8-State Sequencers Triggered by Event Manager
- Serial Communications Interface (SCI)
- Phase-Locked-Loop (PLL)-Based Clock Generation
- Up to 13 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins
- User-Selectable Dual External Interrupts (XINT1 and XINT2)
- Power Management:
  - Three Power-Down Modes
  - Ability to Power Down Each Peripheral Independently
- Real-Time JTAG-Compliant Scan-Based Emulation, IEEE Standard 1149.1† (JTAG)
- Development Tools Include:
  - Texas Instruments (TI) ANSI C Compiler, Assembler/Linker, and Code Composer Studio™ Debugger
  - Evaluation Modules
  - Scan-Based Self-Emulation (XDS510™)
  - Broad Third-Party Digital Motor Control Support
- 32-Pin VF Low-Profile Quad Flatpack (LQFP)
- Extended Temperature Options (A and S)
  - A: – 40°C to 85°C
  - S: – 40°C to 125°C

Code Composer Studio and XDS510 are trademarks of Texas Instruments.

† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port

TEXAS INSTRUMENTS

TMS320LF2401A
DSP CONTROLLER

SPRS161 – MARCH 2001

Table of Contents

Description 2
TMS320x240xA Device Summary 3
Functional Block Diagram of the 2401A DSP Controller 4
Terminal Functions 6
Memory Map 8
Peripheral Memory Map 9
Device Reset and Interrupts 10
DSP CPU Core 13
TMS320LF2401A Instruction Set 13
Functional Block Diagram of the 2401A DSP CPU . . 15
Peripherals 24
Event Manager Module (EVA) 24
Enhanced Analog-to-Digital Converter (ADC) Module 28
Serial Communications Interface (SCI) Module 30
PLL-Based Clock Module 32
Digital I/O and Shared Pin Functions 35
Watchdog (WD) Timer Module 37
Development Support 39
Documentation Support 42
Absolute Maximum Ratings 43
Recommended Operating Conditions 43
Migrating From Other 240xA Devices to LF2401A . . . 63
Peripheral Register Description 65
Mechanical Data 73

PRODUCT PREVIEW

description

The TMS320LF2401A device, a new member of the TMS320C24x™ generation of digital signal processor (DSP) controllers, is part of the TMS320C2000™ platform of fixed-point DSPs. The LF2401A device offers the enhanced TMS320™ DSP architectural design of the C2xx core CPU for low-cost, low-power, and high-performance processing capabilities. Several advanced peripherals, optimized for digital motor and motion control applications, have been integrated to provide a true single-chip DSP controller. While code-compatible with the existing 240x and C24x™ DSP controller devices, the LF2401A offers increased processing performance (40 MIPS) and a higher level of peripheral integration. See the *Device Summary* section for device-specific features.

The LF2401A device offers a peripheral suite tailored to meet the specific price/performance points required by various applications. The LF2401A also offers a cost-effective reprogrammable solution for volume production. A password-based “code security” feature on the device is useful in preventing unauthorized duplication of proprietary code stored in on-chip Flash. Note that the LF2401A contains a 256-word boot ROM to facilitate in-circuit programming.

The LF2401A offers an event manager module which has been optimized for digital motor control and power conversion applications. Capabilities of this module include center- and/or edge-aligned PWM generation, programmable deadband to prevent shoot-through faults, and synchronized analog-to-digital conversion. Select EV pins have been provided with an “input-qualifier” circuitry, which minimizes inadvertent pin-triggering by glitches.

The high-performance, 10-bit analog-to-digital converter (ADC) has a minimum conversion time of 500 ns and offers up to 5 channels of analog input. The autosequencing capability of the ADC allows a maximum of 16 conversions to take place in a single conversion session without any CPU overhead.

A serial communications interface (SCI) is integrated on all devices to provide asynchronous communication to other devices in the system. To maximize device flexibility, functional pins are also configurable as general-purpose inputs/outputs (GPIOs).

To streamline development time, JTAG-compliant scan-based emulation has been integrated into all devices. This provides non-intrusive real-time capabilities required to debug digital control systems. A complete suite of code-generation tools from C compilers to the industry-standard Code Composer Studio™ debugger supports this family. Numerous third-party developers not only offer device-level development tools, but also system-level design and development support.

TMS320x240xA device summary

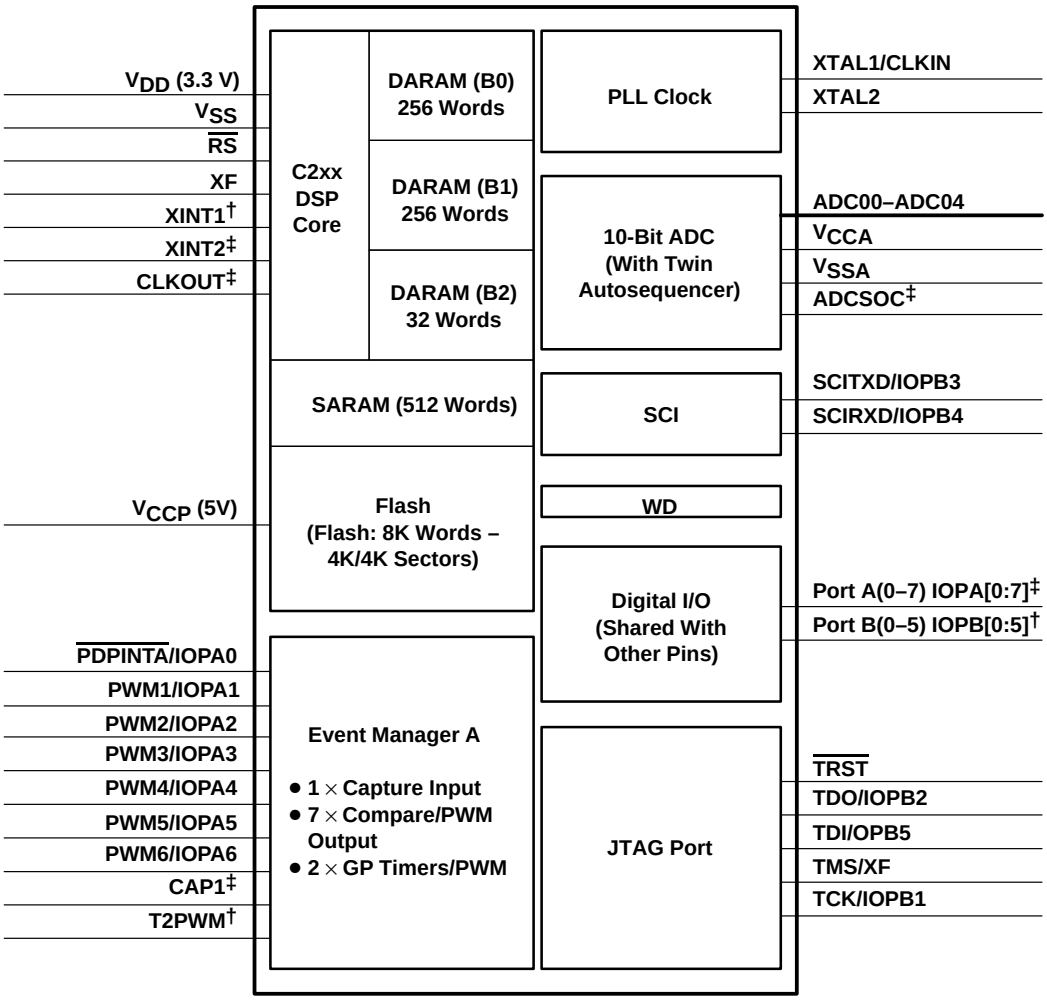
Table 1. Device Feature Comparison Between LF2401A and Lx2402A

FEATURE		LF2401A	LF2402A	LC2402A
C2xx DSP Core		Yes	Yes	Yes
Instruction Cycle		25 ns	25 ns	25 ns
MIPS (40 MHz)		40 MIPS	40 MIPS	40 MIPS
RAM (16-bit word)	Dual-Access RAM (DARAM)	544	544	544
	Single-Access RAM (SARAM)	512	512	—
3.3-V Flash (Program Space, 16-bit word)		8K	8K	—
Flash Sectors		4/4	4/4	—
On-chip ROM (Program Space, 16-bit word)		—	—	6K
Code Security for On-Chip Flash/ROM		Yes	Yes	Yes
Boot ROM		Yes	Yes	—
External Memory Interface		—	—	—
Event Manager A (EVA)		EVA	EVA	EVA
• General-Purpose (GP) Timers		2	2	2
• Compare (CMP)/PWM		7	8	8
• Capture (CAP)/QEP		1	3/2	3/2
• Input qualifier circuitry on $\overline{\text{PDPINTx}}$, CAPn, XINT1/2, and ADCSOC pins		Yes†	Yes	Yes
Watchdog Timer		Yes	Yes	Yes
10-Bit ADC		Yes	Yes	Yes
• Channels		5	8	8
• Conversion Time (minimum)		500 ns	500 ns	500 ns
SPI		—	—	—
SCI		Yes	Yes	Yes
CAN		—	—	—
Digital I/O Pins (Shared)		13	21	21
External Interrupts		2	3	3
Supply Voltage	Core	3.3 V	3.3 V	3.3 V
	I/O	3.3 V	3.3 V	3.3 V
Packaging		32-pin VF	64-pin PG	64-pin PG 64-pin PAG

† Some pins may not be applicable to LF2401A.

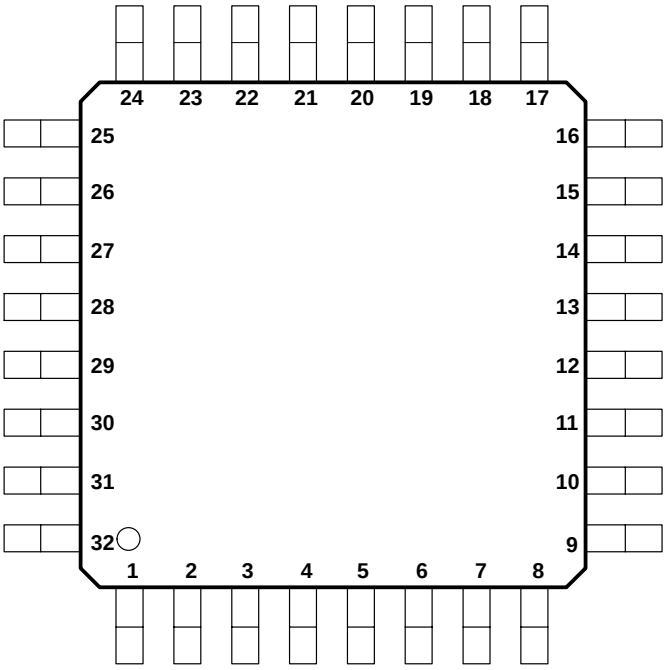
PRODUCT PREVIEW

functional block diagram of the 2401A DSP controller



† T2PWM, XINT1, and IOPB0 functionalities are multiplexed into a single pin, T2PWM/XINT1/IOPB0.
‡ XINT2, ADCSOC, CAP1, IOPA7, and CLKOUT functionalities are multiplexed into a single pin, XINT2/ADCSOC/CAP1/IOPA7/CLKOUT.

32-PIN VF PACKAGE
(TOP VIEW)



TBD – Pin assignments for the 32-pin VF package to be supplied later.

PRODUCT PREVIEW

terminal functions

Terminal Functions†

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
$\overline{RS}$		Device reset. $\overline{RS}$ causes the device to terminate execution and to set PC = 0. When $\overline{RS}$ is brought to a high level, execution begins at location zero of program memory. (↑)
$\overline{PDPINTA}$/IOPA0		Power drive protection input. When this pin is pulled low by an external event, an interrupt is generated and all PWM outputs go to high-impedance state. $\overline{PDPINTA}$ will keep PWM outputs in high-impedance state even when the DSP is not executing. The device comes up with $\overline{PDPINTA}$ activated; however, the user can disable the $\overline{PDPINTA}$ function if needed, by writing to bit 0 of the EVAIMRA register. (↑) This pin *must* be held high when on-chip boot ROM is invoked.
PWM1/**IOPA1**		Compare/PWM output 1 or GPIO (↑)
PWM2/**IOPA2**		Compare/PWM output 2 or GPIO (↑)
PWM3/**IOPA3**		Compare/PWM output 3 or GPIO (↑)
PWM4/**IOPA4**		Compare/PWM output 4 or GPIO (↑)
PWM5/**IOPA5**		Compare/PWM output 5 or GPIO (↑)
PWM6/**IOPA6**		Compare/PWM output 6 or GPIO (↑)
T2PWM/**XINT1**/**IOPB0**		Upon reset, this pin comes up as XINT1/IOPB0 pin. To enable the XINT1 function, the appropriate bit in the XINT1CR register must be set. No special configuration sequence is needed to use this pin as a GPIO. However, a write to the PADATDIR register is necessary to configure this pin as a general-purpose output. Configuration of this pin as T2PWM is achieved by writing a one to bit 8 of the MCRA register. Note that the value of bit 8 in the MCRA register does not affect the XINT1 functionality of this pin. The XINT1 function is enabled/disabled by the value written into the XINT1CR register and is independent of the value written in bit 8 in the MCRA register. (↑)
XINT2/**ADCSOC**/**CAP1**/ **IOPA7**/CLKOUT		Upon reset, this pin can be configured as **any one** of the following: XINT2, ADCSOC, CAP1, or IOPA7. To configure this pin for XINT2 function, the appropriate bit in the XINT2CR register must be set. To configure this pin for ADCSOC function, the appropriate bit in the ADCTRL2 register must be set. To configure this pin for CAP1 function, the appropriate bits in the CAPCONA register must be configured. To summarize, the XINT2, ADCSOC, and CAP1 functions are enabled at the respective peripheral level. No special configuration sequence is needed to use this pin as a GPIO. However, a write to the PADATDIR register is necessary to configure this pin as a general-purpose output. This pin can also function as the CPU clock output. This is achieved by writing a one to bit 7 of the MCRA register. When CLKOUT is chosen, the internal logic for the XINT2, ADCSOC, and CAP1 sees the pin as a “1”. (↑)
ADC00		Analog input channel 0
ADC01		Analog input channel 1
ADC02		Analog input channel 2
ADC03		Analog input channel 3
ADC04		Analog input channel 4
V_{CCA}		Analog supply voltage for ADC (3.3 V).‡ Internally connected to V_{REFHI}
V_{SSA}		Analog ground reference for ADC. Internally connected to V_{REFLO}.

† Bolding indicates function of the device pin after reset.
‡ It is highly recommended that V_{CCA} be isolated from the digital supply voltage (and V_{SSA} from digital ground) to maintain the specified accuracy and improve the noise immunity of the ADC.
§ TDI is muxed with digital output, not digital I/O.
LEGEND: ↑ – Internal pullup ↓ – Internal pulldown (Typical active pullup/pulldown value is ±20 µA.)
NOTE: On the target hardware, pins 13 and 14 of the JTAG header must be pulled high.

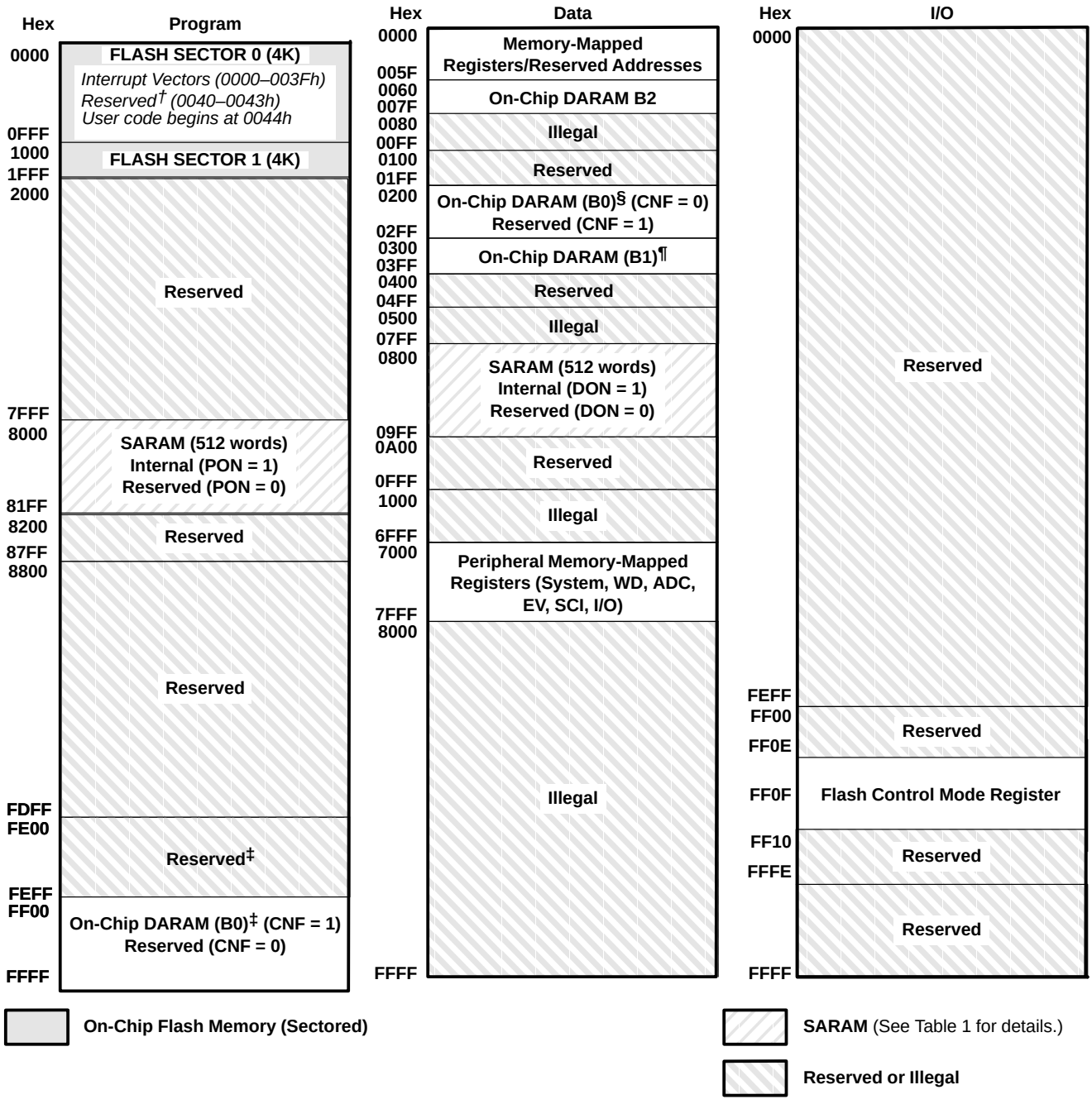
terminal functions (continued)

Terminal Functions† (Continued)

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
SCITXD/**IOPB3**		SCI asynchronous serial port transmit data or GPIO (↑)
SCIRXD/**IOPB4**		SCI asynchronous serial port receive data or GPIO (↑)
TCK/**IOPB1**		JTAG test clock or GPIO (↑)
TDI/**OPB5**§		JTAG test data input or GPO. When $\overline{\text{TRST}}$ is low (i.e., when the JTAG connector is not connected to the DSP), the TDI/**OPB5** pin acts as an output. When $\overline{\text{RS}}$ is low, the **OPB5** pin is asynchronously forced into a high-impedance state and when $\overline{\text{RS}}$ subsequently rises, it will remain in high-impedance state until software configures this pin as an output. The B5DIR bit (bit 13 of the PBDATDIR register) controls the enable to this output buffer. Bit 13 of the MCRA register will have no effect on this pin. (↑) This pin *must* be held low during a reset to invoke the on-chip boot ROM.
TDO/**IOPB2**		JTAG scan out, test data output or GPIO (↓)
TMS/**XF**		JTAG test mode select or GPO. External flag output (latched software-programmable signal). XF is a general-purpose output pin. It is set/reset by the `SETC XF/CLRC XF` instruction. This pin is configured as an external flag output by all device resets. (↑)
$\overline{\text{TRST}}$		JTAG test reset. After power-up or reset, the function of the TCK, TDI, TDO, and TMS pins will depend on the state of the $\overline{\text{TRST}}$ pin. If $\overline{\text{TRST}}$ = 1 (Test or Debugging mode), the function of these pins will be JTAG function (the GPIO and SCI functions of these pins are not available). If $\overline{\text{TRST}}$ = 0 (Functional mode), these pins function as GPIO or SCI pins, as appropriate. (↓)
XTAL1/CLKIN		Crystal/Clock input to PLL
XTAL2		Crystal output
V_{CCP}		Flash programming supply voltage
V_{DD}		Core supply (3.3 V)
V_{DD}		Core supply (3.3 V)
V_{SS}		Core ground
V_{SS}		Core ground
V_{SS}		Core ground

† Bolding indicates function of the device pin after reset.
‡ It is highly recommended that V_{CCA} be isolated from the digital supply voltage (and V_{SSA} from digital ground) to maintain the specified accuracy and improve the noise immunity of the ADC.
§ TDI is muxed with digital output, not digital I/O.
LEGEND: ↑ – Internal pullup ↓ – Internal pulldown (Typical active pullup/pulldown value is ±20 µA.)
NOTE: On the target hardware, pins 13 and 14 of the JTAG header must be pulled high.

memory map



NOTE A: Boot ROM: If the boot ROM is enabled, then addresses 0000–00FF in the program space will be occupied by boot ROM.

† Addresses 0040h–0043h in program memory are reserved for code security passwords.

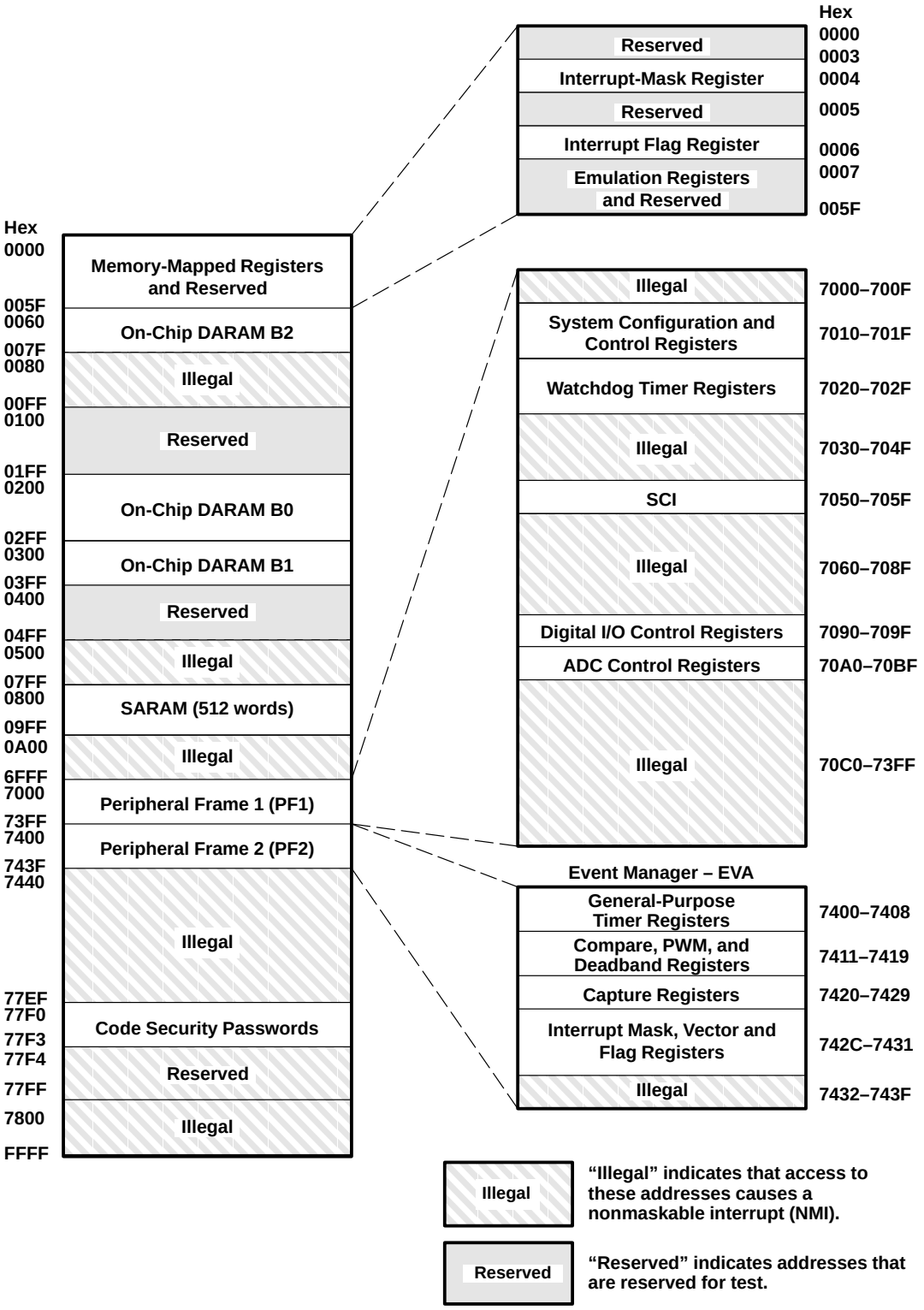
‡ When CNF = 1, addresses FE00h–FEFFh and FF00h–FFFFh are mapped to the same physical block (B0) in program-memory space. For example, a write to FE00h has the same effect as a write to FF00h. For simplicity, addresses FE00h–FEFFh are referred to as reserved.

§ When CNF = 0, addresses 0100h–01FFh and 0200h–02FFh are mapped to the same physical block (B0) in data-memory space. For example, a write to 0100h has the same effect as a write to 0200h. For simplicity, addresses 0100h–01FFh are referred to as reserved.

¶ Addresses 0300h–03FFh and 0400h–04FFh are mapped to the same physical block (B1) in data-memory space. For example, a write to 0400h has the same effect as a write to 0300h. For simplicity, addresses 0400h–04FFh are referred to as reserved.

Figure 1. TMS320LF2401A Memory Map

peripheral memory map



PRODUCT PREVIEW

device reset and interrupts

The TMS320LF2401A software-programmable interrupt structure supports flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The LF2401A recognizes three types of interrupt sources.

- **Reset** (hardware- or software-initiated) is unarbitrated by the CPU and takes immediate priority over any other executing functions. All maskable interrupts are disabled until the reset service routine enables them.

  The LF2401A devices have two sources of reset: an external reset pin and a watchdog timer time-out (reset).

- **Hardware-generated interrupts** are requested by external pins or by on-chip peripherals. There are two types:

  – *External interrupts* are generated by one of three external pins corresponding to the interrupts XINT1, XINT2, and $\overline{\text{PDPINTA}}$. These three can be masked both by dedicated enable bits and by the CPU's interrupt mask register (IMR), which can mask each maskable interrupt line at the DSP core.

  – *Peripheral interrupts* are initiated internally by these on-chip peripheral modules: event manager A, SCI, and ADC. They can be masked both by enable bits for each event in each peripheral and by the CPU's IMR, which can mask each maskable interrupt line at the DSP core.

- **Software-generated interrupts** for the LF2401A devices include:

  – *The INTR instruction.* This instruction allows initialization of any LF2401A interrupt with software. Its operand indicates the interrupt vector location to which the CPU branches. This instruction globally disables maskable interrupts (sets the INTM bit to 1).

  – *The NMI instruction.* This instruction forces a branch to interrupt vector location 24h. This instruction globally disables maskable interrupts. LF2401A devices do not have the NMI hardware signal, only software activation is provided.

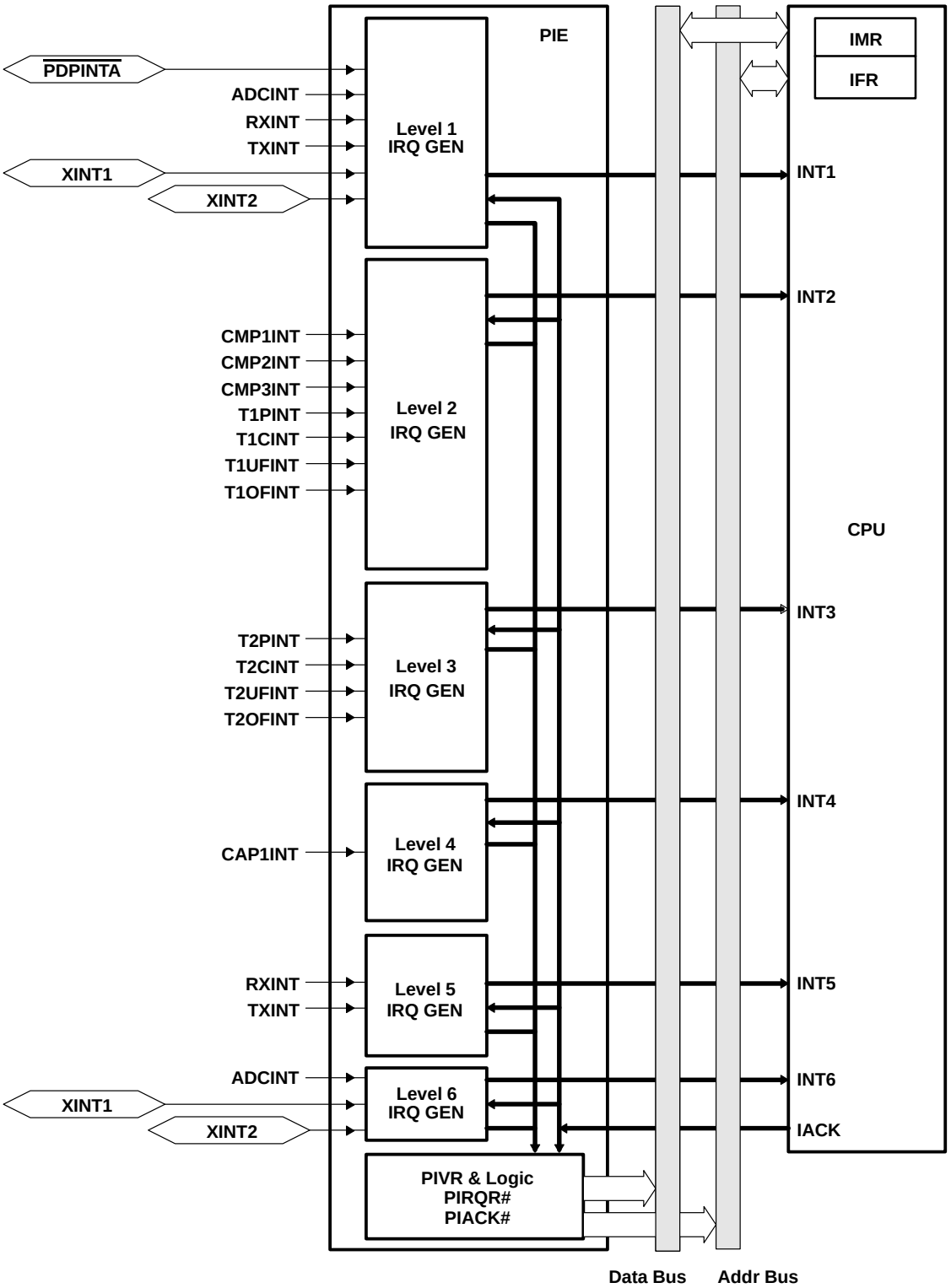
  – *The TRAP instruction.* This instruction forces the CPU to branch to interrupt vector location 22h. The TRAP instruction does *not* disable maskable interrupts (INTM is not set to 1); therefore, when the CPU branches to the interrupt service routine, that routine can be interrupted by the maskable hardware interrupts.

  – *An emulator trap.* This interrupt can be generated with either an INTR instruction or a TRAP instruction.

Six core interrupts (INT1–INT6) are expanded using a peripheral interrupt expansion (PIE) module identical to the F24x devices. The PIE manages all the peripheral interrupts from the LF2401A peripherals and are grouped to share the six core level interrupts. Figure 2 shows the PIE block diagram for hardware-generated interrupts.

The PIE block diagram (Figure 2) and the interrupt table (Table 2) explain the grouping and interrupt vector maps. LF2401A devices have interrupts identical to those of the F24x devices. See Table 2 for details.

device reset and interrupts (continued)



Interrupt from external interrupt pin. The remaining interrupts are internal to the peripherals.

Figure 2. Peripheral Interrupt Expansion (PIE) Module Block Diagram for Hardware-Generated Interrupts

interrupt request structure

Table 2. TMS320LF2401A Interrupt Source Priority and Vectors

INTERRUPT NAME	OVERALL PRIORITY	CPU INTERRUPT AND VECTOR ADDRESS	BIT POSITION IN PIRQRx AND PIACKRx	PERIPHERAL INTERRUPT VECTOR (PIV)	MASK-ABLE?	SOURCE PERIPHERAL MODULE	DESCRIPTION
Reset	1	RSN 0000h		N/A	N	$\overline{RS}$ pin, Watchdog	Reset from pin, watchdog timeout
Reserved	2	– 0026h		N/A	N	CPU	Emulator trap
NMI	3	NMI 0024h		N/A	N	Nonmaskable Interrupt	Nonmaskable interrupt, software interrupt only
PDPINTA	4	INT1 0002h	0.0	0020h	Y	EVA	Power device protection interrupt pin
ADCINT	6		0.1	0004h	Y	ADC	ADC interrupt in high-priority mode
XINT1	7		0.2	0001h	Y	External Interrupt Logic	External interrupt pins in high priority
XINT2	8		0.3	0011h	Y	External Interrupt Logic	
RXINT	10		0.5	0006h	Y	SCI	SCI receiver interrupt in high-priority mode
TXINT	11		0.6	0007h	Y	SCI	SCI transmitter interrupt in high-priority mode
CMP1INT	14	INT2 0004h	0.9	0021h	Y	EVA	Compare 1 interrupt
CMP2INT	15		0.10	0022h	Y	EVA	Compare 2 interrupt
CMP3INT	16		0.11	0023h	Y	EVA	Compare 3 interrupt
T1PINT	17		0.12	0027h	Y	EVA	Timer 1 period interrupt
T1CINT	18		0.13	0028h	Y	EVA	Timer 1 compare interrupt
T1UFINT	19		0.14	0029h	Y	EVA	Timer 1 underflow interrupt
T1OFINT	20		0.15	002Ah	Y	EVA	Timer 1 overflow interrupt
T2PINT	28	INT3 0006h	1.0	002Bh	Y	EVA	Timer 2 period interrupt
T2CINT	29		1.1	002Ch	Y	EVA	Timer 2 compare interrupt
T2UFINT	30		1.2	002Dh	Y	EVA	Timer 2 underflow interrupt
T2OFINT	31		1.3	002Eh	Y	EVA	Timer 2 overflow interrupt
CAP1INT	36	INT4 0008h	1.4	0033h	Y	EVA	Capture 1 interrupt
RXINT	43	INT5 000Ah	1.8	0006h	Y	SCI	SCI receiver interrupt (low-priority mode)
TXINT	44		1.9	0007h	Y	SCI	SCI transmitter interrupt (low-priority mode)

† Refer to the *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357A) for more information.

NOTE: Some interrupts may not be available in a particular device due to the absence of a peripheral. See Table 1 for more details.

interrupt request structure (continued)

Table 2. TMS320LF2401A Interrupt Source Priority and Vectors (Continued)

INTERRUPT NAME	OVERALL PRIORITY	CPU INTERRUPT AND VECTOR ADDRESS	BIT POSITION IN PIRQRx AND PIACKRx	PERIPHERAL INTERRUPT VECTOR (PIV)	MASK-ABLE?	SOURCE PERIPHERAL MODULE	DESCRIPTION
ADCINT	47	INT6 000Ch	1.12	0004h	Y	ADC	ADC interrupt (low priority)
XINT1	48		1.13	0001h	Y	External Interrupt Logic	External interrupt pins (low-priority mode)
XINT2	49		1.14	0011h	Y	External Interrupt Logic	
Reserved		000Eh		N/A	Y	CPU	Analysis interrupt
TRAP	N/A	0022h		N/A	N/A	CPU	TRAP instruction
Phantom Interrupt Vector	N/A	N/A		0000h	N/A	CPU	Phantom interrupt vector
INT8–INT16	N/A	0010h–0020h		N/A	N/A	CPU	Software interrupt vectors†
INT20–INT31	N/A	00028h–0603Fh		N/A	N/A	CPU	

† Refer to the *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357A) for more information.

NOTE: Some interrupts may not be available in a particular device due to the absence of a peripheral. See Table 1 for more details.

DSP CPU core

The TMS320LF2401A device uses an advanced Harvard-type architecture that maximizes processing power by maintaining two separate memory bus structures — program and data — for full-speed execution. This multiple bus structure allows data and instructions to be read simultaneously. Instructions support data transfers between program memory and data memory. This architecture permits coefficients that are stored in program memory to be read in RAM. This, coupled with a four-deep pipeline, allows the LF2401A device to execute most instructions in a single cycle. See the functional block diagram of the 2401A DSP CPU for more information.

TMS320LF2401A instruction set

The 2401A DSP implements a comprehensive instruction set that supports both numeric-intensive signal-processing operations and general-purpose applications, such as multiprocessing and high-speed control.

For maximum throughput, the next instruction is prefetched while the current one is being executed.

addressing modes

The TMS320LF2401A instruction set provides four basic memory-addressing modes: direct, indirect, immediate, and register.

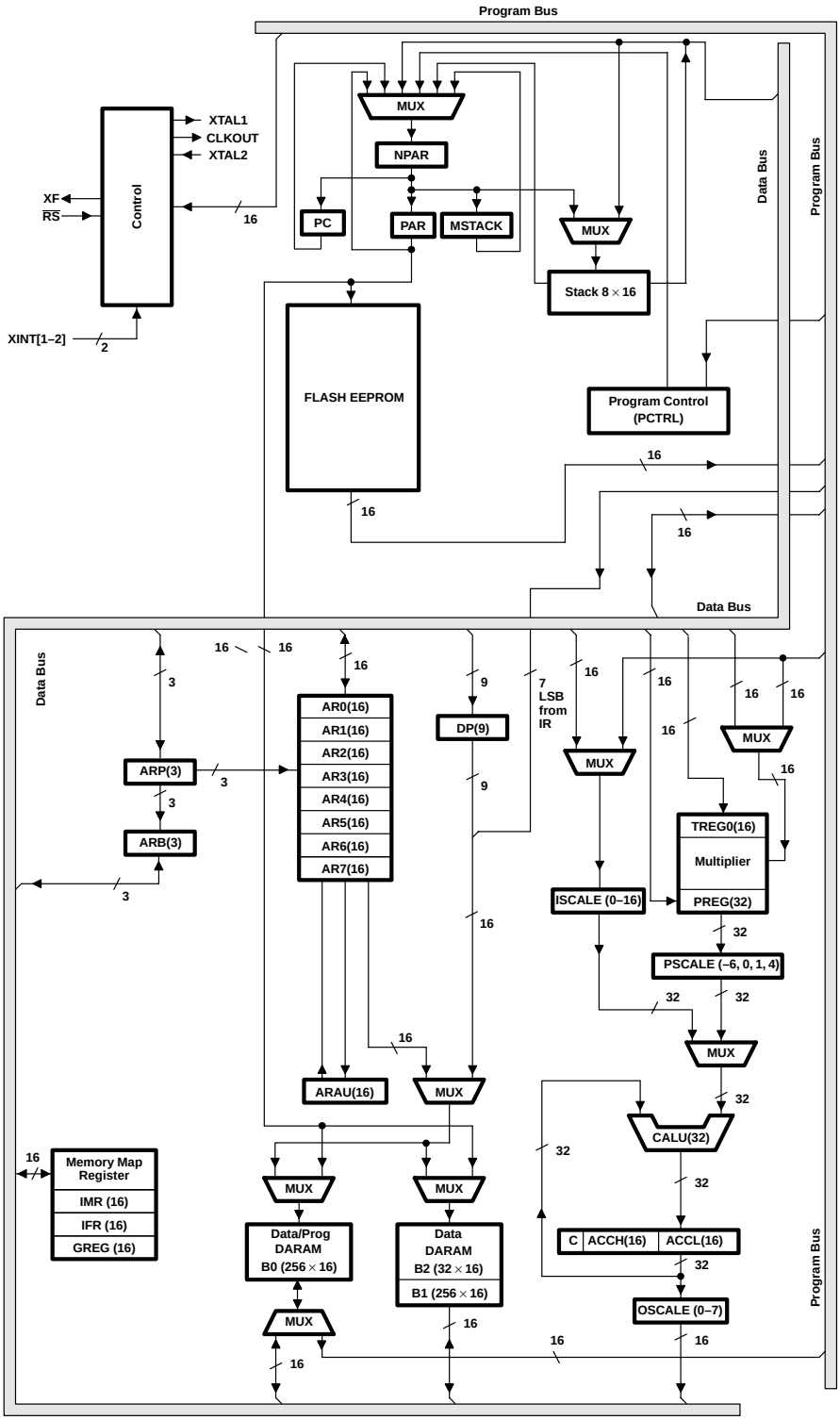
In direct addressing, the instruction word contains the lower seven bits of the data memory address. This field is concatenated with the nine bits of the data memory page pointer (DP) to form the 16-bit data memory address. Therefore, in the direct-addressing mode, data memory is paged effectively with a total of 512 pages, with each page containing 128 words.

Indirect addressing accesses data memory through the auxiliary registers. In this addressing mode, the address of the instruction operand is contained in the currently selected auxiliary register. Eight auxiliary registers (AR0–AR7) provide flexible and powerful indirect addressing. To select a specific auxiliary register, the auxiliary register pointer (ARP) is loaded with a value from 0 to 7 for AR0 through AR7, respectively.

scan-based emulation

TMS320x2xx devices incorporate scan-based emulation logic for code-development and hardware-development support. Scan-based emulation allows the emulator to control the processor in the system without the use of intrusive cables to the full pinout of the device. The scan-based emulator communicates with the x2xx by way of the IEEE 1149.1-compatible (JTAG) interface. The LF2401A DSP does not include boundary scan. The scan chain of the device is useful for emulation function only.

functional block diagram of the 2401A DSP CPU



NOTES: A. See Table 3 for symbol descriptions.
B. For clarity, the data and program buses are shown as single buses although they include address and data bits.
C. Refer to the *TMS320F/C24x DSP Controllers Reference Guide: CPU and Instruction Set* (literature number SPRU160) for CPU instruction set information.

2401A legend for the internal hardware

Table 3. Legend for the 2401A DSP CPU Internal Hardware

SYMBOL	NAME	DESCRIPTION
ACC	Accumulator	32-bit register that stores the results and provides input for subsequent CALU operations. Also includes shift and rotate capabilities
ARAU	Auxiliary Register Arithmetic Unit	An unsigned, 16-bit arithmetic unit used to calculate indirect addresses using the auxiliary registers as inputs and outputs
AUX REGS	Auxiliary Registers 0–7	These 16-bit registers are used as pointers to anywhere within the data space address range. They are operated upon by the ARAU and are selected by the auxiliary register pointer (ARP). AR0 can also be used as an index value for AR updates of more than one and as a compare value to AR.
C	Carry	Register carry output from CALU. C is fed back into the CALU for extended arithmetic operation. The C bit resides in status register 1 (ST1), and can be tested in conditional instructions. C is also used in accumulator shifts and rotates.
CALU	Central Arithmetic Logic Unit	32-bit-wide main arithmetic logic unit for the TMS320C2xx core. The CALU executes 32-bit operations in a single machine cycle. CALU operates on data coming from ISCALE or PSCALE with data from ACC, and provides status results to PCTRL.
DARAM	Dual-Access RAM	If the on-chip RAM configuration control bit (CNF) is set to 0, the reconfigurable data dual-access RAM (DARAM) block B0 is mapped to data space; otherwise, B0 is mapped to program space. Blocks B1 and B2 are mapped to data memory space only, at addresses 0300–03FF and 0060–007F, respectively. Blocks 0 and 1 contain 256 words, while block 2 contains 32 words.
DP	Data Memory Page Pointer	The 9-bit DP register is concatenated with the seven least significant bits (LSBs) of an instruction word to form a direct memory address of 16 bits. DP can be modified by the LST and LDP instructions.
GREG	Global Memory Allocation Register	GREG specifies the size of the global data memory space. Since the global memory space is not used in the 240x devices, this register is reserved.
IMR	Interrupt Mask Register	IMR individually masks or enables the seven interrupts.
IFR	Interrupt Flag Register	The 7-bit IFR indicates that the TMS320C2xx has latched an interrupt from one of the seven maskable interrupts.
INT#	Interrupt Traps	A total of 32 interrupts by way of hardware and/or software are available.
ISCALE	Input Data-Scaling Shifter	16- to 32-bit barrel left-shifter. ISCALE shifts incoming 16-bit data 0 to16 positions left, relative to the 32-bit output within the fetch cycle; therefore, no cycle overhead is required for input scaling operations.
MPY	Multiplier	16 × 16-bit multiplier to a 32-bit product. MPY executes multiplication in a single cycle. MPY operates either signed or unsigned 2s-complement arithmetic multiply.
MSTACK	Micro Stack	MSTACK provides temporary storage for the address of the next instruction to be fetched when program address-generation logic is used to generate sequential addresses in data space.
MUX	Multiplexer	Multiplexes buses to a common input
NPAR	Next Program Address Register	NPAR holds the program address to be driven out on the PAB in the next cycle.
OSCALE	Output Data-Scaling Shifter	16- to 32-bit barrel left-shifter. OSCALE shifts the 32-bit accumulator output 0 to 7 bits left for quantization management and outputs either the 16-bit high- or low-half of the shifted 32-bit data to the data-write data bus (DWEB).
PAR	Program Address Register	PAR holds the address currently being driven on PAB for as many cycles as it takes to complete all memory operations scheduled for the current bus cycle.
PC	Program Counter	PC increments the value from NPAR to provide sequential addresses for instruction-fetching and sequential data-transfer operations.
PCTRL	Program Controller	PCTRL decodes instruction, manages the pipeline, stores status, and decodes conditional operations.

2401A legend for the internal hardware (continued)

Table 3. Legend for the 2401A DSP CPU Internal Hardware (Continued)

SYMBOL	NAME	DESCRIPTION
PREG	Product Register	32-bit register holds results of 16 × 16 multiply
PSCALE	Product-Scaling Shifter	0-, 1-, or 4-bit left shift, or 6-bit right shift of multiplier product. The left-shift options are used to manage the additional sign bits resulting from the 2s-complement multiply. The right-shift option is used to scale down the number to manage overflow of product accumulation in the CALU. PSCALE resides in the path from the 32-bit product shifter and from either the CALU or the data-write data bus (DWEB), and requires no cycle overhead.
STACK	Stack	STACK is a block of memory used for storing return addresses for subroutines and interrupt-service routines, or for storing data. The C2xx stack is 16 bits wide and 8 levels deep.
TREG	Temporary Register	16-bit register holds one of the operands for the multiply operations. TREG holds the dynamic shift count for the LACT, ADDT, and SUBT instructions. TREG holds the dynamic bit position for the BITT instruction.

status and control registers

Two status registers, ST0 and ST1, contain the status of various conditions and modes. These registers can be stored into data memory and loaded from data memory, thus allowing the status of the machine to be saved and restored for subroutines.

The load status register (LST) instruction is used to write to ST0 and ST1. The store status register (SST) instruction is used to read from ST0 and ST1 — except for the INTM bit, which is not affected by the LST instruction. The individual bits of these registers can be set or cleared when using the SETC and CLRC instructions. Figure 3 shows the organization of status registers ST0 and ST1, indicating all status bits contained in each. Several bits in the status registers are reserved and are read as logic 1s. Table 4 lists status register field definitions.

	15	13	12	11	10	9	8	0
ST0	ARP		OV	OVM	1	INTM	DP	

	15	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST1	ARB		CNF	TC	SXM	C	1	1	1	1	XF	1	1	PM	

Figure 3. Organization of Status Registers ST0 and ST1

Table 4. Status Register Field Definitions

FIELD	FUNCTION
ARB	Auxiliary register pointer buffer. When the ARP is loaded into ST0, the old ARP value is copied to the ARB except during an LST instruction. When the ARB is loaded by way of an LST #1 instruction, the same value is also copied to the ARP.
ARP	Auxiliary register (AR) pointer. ARP selects the AR to be used in indirect addressing. When the ARP is loaded, the old ARP value is copied to the ARB register. ARP can be modified by memory-reference instructions when using indirect addressing, and by the LARP, MAR, and LST instructions. The ARP is also loaded with the same value as ARB when an LST #1 instruction is executed.
C	Carry bit. C is set to 1 if the result of an addition generates a carry, or reset to 0 if the result of a subtraction generates a borrow. Otherwise, C is reset after an addition or set after a subtraction, except if the instruction is ADD or SUB with a 16-bit shift. In these cases, ADD can only set and SUB can only reset the carry bit, but cannot affect it otherwise. The single-bit shift and rotate instructions also affect C, as well as the SETC, CLRC, and LST #1 instructions. Branch instructions have been provided to branch on the status of C. C is set to 1 on a reset.
CNF	On-chip RAM configuration control bit. If CNF is set to 0, the reconfigurable data dual-access RAM blocks are mapped to data space; otherwise, they are mapped to program space. The CNF can be modified by the SETC CNF, CLRC CNF, and LST #1 instructions. $\overline{RS}$ sets the CNF to 0.

status and control registers (continued)

Table 4. Status Register Field Definitions (Continued)

FIELD	FUNCTION
DP	Data memory page pointer. The 9-bit DP register is concatenated with the 7 LSBs of an instruction word to form a direct memory address of 16 bits. DP can be modified by the LST and LDP instructions.
INTM	Interrupt mode bit. When INTM is set to 0, all unmasked interrupts are enabled. When set to 1, all maskable interrupts are disabled. INTM is set and reset by the SETC INTM and CLRC INTM instructions. $\overline{RS}$ also sets INTM. INTM has no effect on the unmaskable $\overline{RS}$ and NMI interrupts. Note that INTM is unaffected by the LST instruction. This bit is set to 1 by reset. It is also set to 1 when a maskable interrupt trap is taken.
OV	Overflow flag bit. As a latched overflow signal, OV is set to 1 when overflow occurs in the arithmetic logic unit (ALU). Once an overflow occurs, the OV remains set until a reset, BCND/D on OV/NOV, or LST instruction clears OV.
OVM	Overflow mode bit. When OVM is set to 0, overflowed results overflow normally in the accumulator. When set to 1, the accumulator is set to either its most positive or negative value upon encountering an overflow. The SETC and CLRC instructions set and reset this bit, respectively. LST can also be used to modify the OVM.
PM	Product shift mode. If these two bits are 00, the multiplier's 32-bit product is loaded into the ALU with no shift. If PM = 01, the PREG output is left-shifted one place and loaded into the ALU, with the LSB zero-filled. If PM = 10, the PREG output is left-shifted by 4 bits and loaded into the ALU, with the LSBs zero-filled. PM = 11 produces a right shift of 6 bits, sign-extended. Note that the PREG contents remain unchanged. The shift takes place when transferring the contents of the PREG to the ALU. PM is loaded by the SPM and LST #1 instructions. PM is cleared by $\overline{RS}$.
SXM	Sign-extension mode bit. SXM = 1 produces sign extension on data as it is passed into the accumulator through the scaling shifter. SXM = 0 suppresses sign extension. SXM does not affect the definitions of certain instructions; for example, the ADDS instruction suppresses sign extension regardless of SXM. SXM is set by the SETC SXM instruction and reset by the CLRC SXM instruction and can be loaded by the LST #1 instruction. SXM is set to 1 by reset.
TC	Test/control flag bit. TC is affected by the BIT, BITT, CMPR, LST #1, and NORM instructions. TC is set to a 1 if a bit tested by BIT or BITT is a 1, if a compare condition tested by CMPR exists between AR (ARP) and AR0, if the exclusive-OR function of the 2 most significant bits (MSBs) of the accumulator is true when tested by a NORM instruction. The conditional branch, call, and return instructions can execute based on the condition of TC.
XF	XF pin status bit. XF indicates the state of the XF pin, a general-purpose output pin. XF is set by the SETC XF instruction and reset by the CLRC XF instruction. XF is set to 1 by reset.

central processing unit

The TMS320LF2401A central processing unit (CPU) contains a 16-bit scaling shifter, a 16 x 16-bit parallel multiplier, a 32-bit central arithmetic logic unit (CALU), a 32-bit accumulator, and additional shifters at the outputs of both the accumulator and the multiplier. This section describes the CPU components and their functions. The functional block diagram shows the components of the CPU.

input scaling shifter

The TMS320LF2401A provides a scaling shifter with a 16-bit input connected to the data bus and a 32-bit output connected to the CALU. This shifter operates as part of the path of data coming from program or data space to the CALU and requires no cycle overhead. It is used to align the 16-bit data coming from memory to the 32-bit CALU. This is necessary for scaling arithmetic as well as aligning masks for logical operations.

The scaling shifter produces a left shift of 0 to 16 on the input data. The LSBs of the output are filled with zeros; the MSBs can either be filled with zeros or sign-extended, depending upon the value of the SXM bit (sign-extension mode) of status register ST1. The shift count is specified by a constant embedded in the instruction word or by a value in TREG. The shift count in the instruction allows for specific scaling or alignment operations specific to that point in the code. The TREG base shift allows the scaling factor to be adaptable to the system's performance.

multiplier

The TMS320LF2401A device uses a 16 x 16-bit hardware multiplier that is capable of computing a signed or an unsigned 32-bit product in a single machine cycle. All multiply instructions, except the MPYU (multiply unsigned) instruction, perform a signed multiply operation. That is, two numbers being multiplied are treated as 2s-complement numbers, and the result is a 32-bit 2s-complement number. There are two registers associated with the multiplier, as follow:

- 16-bit temporary register (TREG) that holds one of the operands for the multiplier
- 32-bit product register (PREG) that holds the product

Four product-shift modes (PM) are available at the PREG output (PSCALE). These shift modes are useful for performing multiply/accumulate operations, performing fractional arithmetic, or justifying fractional products. The PM field of status register ST1 specifies the PM shift mode, as shown in Table 5.

Table 5. PSCALE Product-Shift Modes

PM	SHIFT	DESCRIPTION
00	No shift	Product feed to CALU or data bus with no shift
01	Left 1	Removes the extra sign bit generated in a 2s-complement multiply to produce a Q31 product
10	Left 4	Removes the extra 4 sign bits generated in a 16x13 2s-complement multiply to a produce a Q31 product when using the multiply-by-a-13-bit constant
11	Right 6	Scales the product to allow up to 128 product accumulation without the possibility of accumulator overflow

The product can be shifted one bit to compensate for the extra sign bit gained in multiplying two 16-bit 2s-complement numbers (MPY instruction). A four-bit shift is used in conjunction with the MPY instruction with a short immediate value (13 bits or less) to eliminate the four extra sign bits gained in multiplying a 16-bit number by a 13-bit number. Finally, the output of PREG can be right-shifted 6 bits to enable the execution of up to 128 consecutive multiply/accumulates without the possibility of overflow.

The LT (load TREG) instruction normally loads TREG to provide one operand (from the data bus), and the MPY (multiply) instruction provides the second operand (also from the data bus). A multiplication also can be performed with a 13-bit immediate operand when using the MPY instruction. Then, a product is obtained every two cycles. When the code is executing multiple multiplies and product sums, the CPU supports the pipelining of the TREG load operations with CALU operations using the previous product. The pipeline operations that run in parallel with loading the TREG include: load ACC with PREG (LTP); add PREG to ACC (LTA); add PREG to ACC and shift TREG input data (DMOV) to next address in data memory (LTD); and subtract PREG from ACC (LTS).

Two multiply/accumulate instructions (MAC and MACD) fully utilize the computational bandwidth of the multiplier, allowing both operands to be processed simultaneously. The data for these operations can be transferred to the multiplier each cycle by way of the program and data buses. This facilitates single-cycle multiply/accumulates when used with the repeat (RPT) instruction. In these instructions, the coefficient addresses are generated by program address generation (PAGEN) logic, while the data addresses are generated by data address generation (DAGEN) logic. This allows the repeated instruction to access the values from the coefficient table sequentially and step through the data in any of the indirect addressing modes.

The MACD instruction, when repeated, supports filter constructs (weighted running averages) so that as the sum-of-products is executed, the sample data is shifted in memory to make room for the next sample and to throw away the oldest sample.

multiplier (continued)

The MPYU instruction performs an unsigned multiplication, which greatly facilitates extended-precision arithmetic operations. The unsigned contents of TREG are multiplied by the unsigned contents of the addressed data memory location, with the result placed in PREG. This process allows the operands of greater than 16 bits to be broken down into 16-bit words and processed separately to generate products of greater than 32 bits. The SQRA (square/add) and SQRS (square/subtract) instructions pass the same value to both inputs of the multiplier for squaring a data memory value.

After the multiplication of two 16-bit numbers, the 32-bit product is loaded into the 32-bit product register (PREG). The product from PREG can be transferred to the CALU or to data memory by way of the SPH (store product high) and SPL (store product low) instructions. Note: the transfer of PREG to either the CALU or data bus passes through the PSCALE shifter, and therefore is affected by the product shift mode defined by PM. This is important when saving PREG in an interrupt-service-routine context save as the PSCALE shift effects cannot be modeled in the restore operation. PREG can be cleared by executing the MPY #0 instruction. The product register can be restored by loading the saved low half into TREG and executing a MPY #1 instruction. The high half, then, is loaded using the LPH instruction.

central arithmetic logic unit

The TMS320LF2401A central arithmetic logic unit (CALU) implements a wide range of arithmetic and logical functions, the majority of which execute in a single clock cycle. This ALU is referred to as central to differentiate it from a second ALU used for indirect-address generation called the auxiliary register arithmetic unit (ARAU). Once an operation is performed in the CALU, the result is transferred to the accumulator (ACC) where additional operations, such as shifting, can occur. Data that is input to the CALU can be scaled by ISCALE when coming from one of the data buses (DRDB or PRDB) or scaled by PSCALE when coming from the multiplier.

The CALU is a general-purpose ALU that operates on 16-bit words taken from data memory or derived from immediate instructions. In addition to the usual arithmetic instructions, the CALU can perform Boolean operations, facilitating the bit-manipulation ability required for a high-speed controller. One input to the CALU is always provided from the accumulator, and the other input can be provided from the product register (PREG) of the multiplier or the output of the scaling shifter (that has been read from data memory or from the ACC). After the CALU has performed the arithmetic or logical operation, the result is stored in the accumulator.

The TMS320LF2401A device supports floating-point operations for applications requiring a large dynamic range. The NORM (normalization) instruction is used to normalize fixed-point numbers contained in the accumulator by performing left shifts. The four bits of the TREG define a variable shift through the scaling shifter for the LACT/ADDT/SUBT (load/add to/subtract from accumulator with shift specified by TREG) instructions. These instructions are useful in floating-point arithmetic where a number needs to be denormalized — that is, floating-point to fixed-point conversion. They are also useful in the execution of an automatic gain control (AGC) going into a filter. The BITT (bit test) instruction provides testing of a single bit of a word in data memory based on the value contained in the four LSBs of TREG.

The CALU overflow saturation mode can be enabled/disabled by setting/resetting the OVM bit of ST0. When the CALU is in the overflow saturation mode and an overflow occurs, the overflow flag is set and the accumulator is loaded with either the most positive or the most negative value representable in the accumulator, depending on the direction of the overflow. The value of the accumulator at saturation is 07FFFFFFh (positive) or 080000000h (negative). If the OVM (overflow mode) status register bit is reset and an overflow occurs, the overflowed results are loaded into the accumulator with modification. (Note that logical operations cannot result in overflow.)

The CALU can execute a variety of branch instructions that depend on the status of the CALU and the accumulator. These instructions can be executed conditionally based on any meaningful combination of these status bits. For overflow management, these conditions include OV (branch on overflow) and EQ (branch on accumulator equal to zero). In addition, the BACC (branch to address in accumulator) instruction provides the ability to branch to an address specified by the accumulator (computed goto). Bit test instructions (BIT and BITT), which do not affect the accumulator, allow the testing of a specified bit of a word in data memory.

central arithmetic logic unit (continued)

The CALU also has an associated carry bit that is set or reset depending on various operations within the device. The carry bit allows more efficient computation of extended-precision products and additions or subtractions. It is also useful in overflow management. The carry bit is affected by most arithmetic instructions as well as the single-bit shift and rotate instructions. It is not affected by loading the accumulator, logical operations, or other such non-arithmetic or control instructions.

The ADDC (add to accumulator with carry) and SUBB (subtract from accumulator with borrow) instructions use the previous value of carry in their addition/subtraction operation.

The one exception to the operation of the carry bit is in the use of ADD with a shift count of 16 (add to high accumulator) and SUB with a shift count of 16 (subtract from high accumulator) instructions. This case of the ADD instruction can set the carry bit only if a carry is generated, and this case of the SUB instruction can reset the carry bit only if a borrow is generated; otherwise, neither instruction affects it.

Two conditional operands, C and NC, are provided for branching, calling, returning, and conditionally executing, based upon the status of the carry bit. The SETC, CLRC, and LST #1 instructions also can be used to load the carry bit. The carry bit is set to one on a hardware reset.

accumulator

The 32-bit accumulator is the registered output of the CALU. It can be split into two 16-bit segments for storage in data memory. Shifters at the output of the accumulator provide a left shift of 0 to 7 places. This shift is performed while the data is being transferred to the data bus for storage. The contents of the accumulator remain unchanged. When the postscaling shifter is used on the high word of the accumulator (bits 16–31), the MSBs are lost and the LSBs are filled with bits shifted in from the low word (bits 0–15). When the postscaling shifter is used on the low word, the LSBs are zero-filled.

The SFL and SFR (in-place one-bit shift to the left/right) instructions and the ROL and ROR (rotate to the left/right) instructions implement shifting or rotating of the contents of the accumulator through the carry bit. The SXM bit affects the definition of the SFR (shift accumulator right) instruction. When SXM = 1, SFR performs an arithmetic right shift, maintaining the sign of the accumulator data. When SXM = 0, SFR performs a logical shift, shifting out the LSBs and shifting in a zero for the MSB. The SFL (shift accumulator left) instruction is not affected by the SXM bit and behaves the same in both cases, shifting out the MSB and shifting in a zero. Repeat (RPT) instructions can be used with the shift and rotate instructions for multiple-bit shifts.

auxiliary registers and auxiliary-register arithmetic unit (ARAU)

The 2401A provides a register file containing eight auxiliary registers (AR0–AR7). The auxiliary registers are used for indirect addressing of the data memory or for temporary data storage. Indirect auxiliary-register addressing allows placement of the data memory address of an instruction operand into one of the auxiliary registers. These registers are referenced with a 3-bit auxiliary register pointer (ARP) that is loaded with a value from 0 through 7, designating AR0 through AR7, respectively. The auxiliary registers and the ARP can be loaded from data memory, the ACC, the product register, or by an immediate operand defined in the instruction. The contents of these registers also can be stored in data memory or used as inputs to the CALU.

The auxiliary register file (AR0–AR7) is connected to the ARAU. The ARAU can autoindex the current auxiliary register while the data memory location is being addressed. Indexing either by ±1 or by the contents of the AR0 register can be performed. As a result, accessing tables of information does not require the CALU for address manipulation; therefore, the CALU is free for other operations in parallel.

internal memory

The TMS320LF2401A device is configured with the following memory modules:

- Dual-access random-access memory (DARAM)
- Single-access random-access memory (SARAM)
- Flash
- Boot ROM

dual-access RAM (DARAM)

There are 544 words × 16 bits of DARAM on the 2401A device. The 2401A DARAM allows writes to and reads from the RAM in the same cycle. The DARAM is configured in three blocks: block 0 (B0), block 1 (B1), and block 2 (B2). Block 1 contains 256 words and Block 2 contains 32 words, and both blocks are located only in data memory space. Block 0 contains 256 words, and can be configured to reside in either data or program memory space. The SETC CNF (configure B0 as program memory) and CLRC CNF (configure B0 as data memory) instructions allow dynamic configuration of the memory maps through software.

When using on-chip RAM, the 2401A runs at full speed with no wait states. The ability of the DARAM to allow two accesses to be performed in one cycle, coupled with the parallel nature of the 2401A architecture, enables the device to perform three concurrent memory accesses in any given machine cycle.

single-access RAM (SARAM)

There are 512 words × 16 bits of SARAM on the LF2401A. The PON and DON bits select SARAM (512 words) mapping in program space, data space, or both. See Table 15 for details on the SCSR2 register and the PON and DON bits. At reset, these bits are 11, and the on-chip SARAM is mapped in both the program and data spaces.

Flash EEPROM

Flash EEPROM provides an attractive alternative to masked program ROM. Like ROM, Flash is nonvolatile. However, it has the advantage of “in-target” reprogrammability. The LF2401A incorporates one 8K × 16-bit Flash EEPROM module in program space. The Flash module has two sectors that can be individually protected while erasing or programming. The sector size is partitioned as 4K/4K sectors.

Unlike most discrete Flash memory, the LF2401A Flash does not require a dedicated state machine, because the algorithms for programming and erasing the Flash are executed by the DSP core. This enables several advantages, including: reduced chip size and sophisticated, adaptive algorithms. For production programming, the IEEE Standard 1149.1† (JTAG) scan port provides easy access to the on-chip RAM for downloading the algorithms and Flash code. This Flash requires 5 V for programming (at V_{CCP} pin only) the array. The Flash runs at zero wait state while the device is powered at 3.3 V.

† IEEE Standard 1149.1–1990, IEEE Standard Test Access Port.

boot ROM

Boot ROM is a 256-word ROM mapped in program space 0000h–00FFh. This ROM will be enabled if the BOOT_EN mode is enabled during reset. Boot-enable function is implemented using combinational logic of the TDI, $\overline{\text{TRST}}$, and $\overline{\text{RS}}$ pins as described below. The on-chip bootloader is invoked when:

$\overline{\text{TRST}}$ = 0

$\overline{\text{RS}}$ = 0

TDI = 0

(In addition to the three pins mentioned above, the application must ensure that $\overline{\text{PDPINTA}}$ stays high during the execution of the boot ROM code.) Since it has an internal pulldown, the $\overline{\text{TRST}}$ pin will be low, provided the JTAG connector is not connected. Therefore, the BOOT_EN bit (bit 3 of the SCSR2 register) will be set to 0 if TDI is low upon reset. If on-chip bootloader is desired while debugging with the JTAG connector connected ($\overline{\text{TRST}}$ = 1), it can be achieved by writing a “0” into bit 3 of the SCSR2 register.

The boot ROM has a generic bootloader to transfer code through the SCI port. The incoming code should disable the BOOT_ROM bit by writing 1 to bit 3 of the SCSR2 register, or else, the whole Flash array will not be enabled.

The boot ROM code sets the PLL to x2 or x4 option based on the condition of the SCITXD pin during reset. The SCITXD pin should be pulled high/low to select the PLL multiplication factor. The choices made are as follows:

- If the SCITXD pin is pulled low, the PLL multiplier is set to 2.
- If the SCITXD pin is pulled high, the PLL multiplier is set to 4. (Default)
- If the SCITXD pin is not driven at reset, the internal pullup selects the default multiplier of 4.

Care should be taken such that a combination of CLKIN and the PLL multiplication factor should not result in a CPU clock speed of greater than 40 MHz, the maximum rated speed.

Furthermore, when the bootloader is used, only specific values of CLKIN would result in a baud-lock for the SCI. Refer to the *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357A) for more details about the bootloader operation.

Flash security

The 2401A device has a security feature that prevents external access to Flash memory. This feature is useful in preventing unauthorized duplication of proprietary code resident on the Flash memory.

If access to Flash contents are desired for debugging purposes, two actions need to be taken:

1. A “dummy” read of locations 40h, 41h, 42h and 43h (of program memory space) is necessary. The word “dummy” indicates that the destination address of this read is not relevant. If 40h–43h contain all zeros or ones, then Step 2 is not required.
2. A 64-bit password (split as four 16-bit words) must be written to the data-memory locations 77F0h, 77F1h, 77F2h, and 77F3h. The four 16-bit words written to these locations must match the four words stored in 40h, 41h, 42h, and 43h (of program memory space), respectively. The device becomes “unsecured” one cycle after the last instruction that unsecures the part.

PERIPHERALS

The integrated peripherals of the TMS320LF2401A are described in the following subsections:

- Event-manager module (EVA)
- Enhanced analog-to-digital converter (ADC) module
- Serial communications interface (SCI) module
- PLL-based clock module
- Digital I/O and shared pin functions
- Watchdog (WD) timer module

event manager module (EVA)

The event-manager module includes general-purpose (GP) timers, full-compare/PWM units, and a capture unit. Table 6 shows the module and signal names used. Table 6 also shows the features and functionality available for the event-manager module.

EVA's peripheral register set starts at 7400h. The paragraphs in this section describe the function of the GP timers, the compare units, and the capture unit.

Table 6. Module and Signal Names for EVA

EVENT MANAGER MODULES	MODULE	SIGNAL
GP Timers	Timer 1 Timer 2	— T2PWM/T2CMP
Compare Units	Compare 1 Compare 2 Compare 3	PWM1/2 PWM3/4 PWM5/6
Capture Unit	Capture 1	CAP1

event manager module (EVA) (continued)

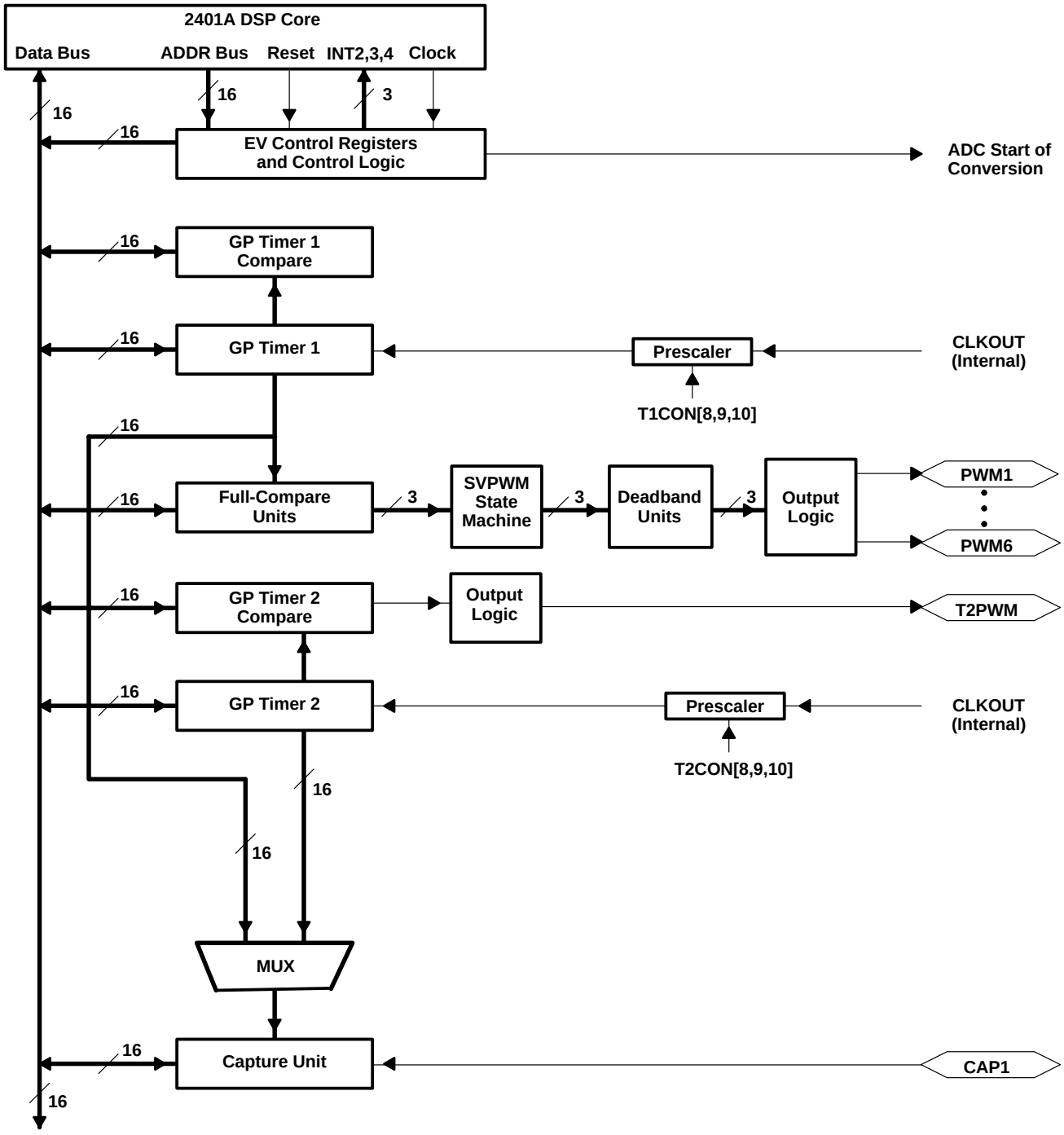


Figure 4. Event Manager A Block Diagram

general-purpose (GP) timers

There are two GP timers. GP timer x (x = 1 or 2) includes:

- A 16-bit timer, up-/down-counter, TxCNT, for reads or writes
- A 16-bit timer-compare register, TxCMPR (double-buffered with shadow register), for reads or writes
- A 16-bit timer-period register, TxPR (double-buffered with shadow register), for reads or writes
- A 16-bit timer-control register,TxCON, for reads or writes
- Internal input clock
- A programmable prescaler for internal clock input
- Control and interrupt logic, for four maskable interrupts: *underflow*, *overflow*, *timer compare*, and *period interrupts*

The GP timers can be operated independently or synchronized with each other. The compare register associated with GP timer 2 can be used for compare function and PWM-waveform generation. There are three continuous modes of operations for each GP timer in up- or up/down-counting operations. An internal input clock with programmable prescaler is used for each GP timer. GP timers also provide the time base for the other event-manager submodules: GP timer 1 for all the compares and PWM circuits, and GP timer 2/1 for the capture unit. Double-buffering of the period and compare registers allows programmable change of the timer (PWM) period and the compare/PWM pulse width as needed.

full-compare units

There are three full-compare units on the event manager (EVA). These compare units use GP timer1 as the time base and generate six outputs for compare and PWM-waveform generation using programmable deadband circuit. The state of each of the six outputs is configured independently. The compare registers of the compare units are double-buffered, allowing programmable change of the compare/PWM pulse widths as needed.

programmable deadband generator

The deadband generator circuit includes three 8-bit counters and an 8-bit compare register. Desired deadband values (from 0 to 16 μs) can be programmed into the compare register for the outputs of the three compare units. The deadband generation can be enabled/disabled for each compare unit output individually. The deadband-generator circuit produces two outputs (with or without deadband zone) for each compare unit output signal. The output states of the deadband generator are configurable and changeable as needed by way of the double-buffered ACTR register.

PWM waveform generation

Up to eight PWM waveforms (outputs) can be generated simultaneously by EVA: three independent pairs (six outputs) by the three full-compare units with *programmable deadbands*, and two independent PWMs by the GP-timer compares.

PWM characteristics

Characteristics of the PWMs are as follows:

- 16-bit registers
- Programmable deadband for the PWM output pairs, from 0 to 12 μs
- Minimum deadband width of 25 ns
- Change of the PWM carrier frequency for PWM frequency wobbling as needed
- Change of the PWM pulse widths within and after each PWM period as needed
- External-maskable power and drive-protection interrupts
- Pulse-pattern-generator circuit, for programmable generation of asymmetric, symmetric, and four-space vector PWM waveforms
- Minimized CPU overhead using auto-reload of the compare and period registers
- The PWM pins are driven to a high-impedance state when the $\overline{\text{PDPINTA}}$ pin is driven low and **after** $\overline{\text{PDPINTA}}$ signal qualification. The status of the $\overline{\text{PDPINTA}}$ pin (after qualification) is reflected in bit 8 of the COMCONA register.

capture unit

The capture unit provides a logging function for different events or transitions. The values of the selected GP timer counter is captured and stored in the two-level-deep FIFO stack when selected transitions are detected on the capture input pin, CAP1. The capture unit consists of three capture circuits.

- The capture unit includes the following features:
  - One 16-bit capture control register, CAPCONA (R/W)
  - One 16-bit capture FIFO status register, CAPFIFOA
  - Selection of GP timer 1/2 as the time base
  - One 16-bit 2-level-deep FIFO stack
  - One capture input pin (CAP1). [The input is synchronized with the device (CPU) clock. In order for a transition to be captured, the input must hold at its current level to meet two rising edges of the device clock.]
  - User-specified transition (rising edge, falling edge, or both edges) detection
  - One maskable interrupt flag

input qualifier circuitry

An input-qualifier circuitry qualifies the input signal to the CAP1, XINT1/2, ADCSOC, and $\overline{\text{PDPINTA}}$ pins in the 2401A device. (The I/O functions of these pins do not use the input-qualifier circuitry). The state of the internal input signal will change only after the pin is high/low for 6(12) clock edges. This ensures that a glitch smaller than 5(11) CLKOUT cycles wide will not change the internal pin input state. The user must hold the pin high/low for 6(12) cycles to ensure the device will see the level change. Bit 6 of the SCSR2 register controls whether 6 clock edges (bit 6 = 0) or 12 clock edges (bit 6 = 1) are used to block 5- or 11-cycle glitches.

enhanced analog-to-digital converter (ADC) module

A simplified functional block diagram of the ADC module is shown in Figure 5. The ADC module consists of a 10-bit ADC with a built-in sample-and-hold (S/H) circuit. Functions of the ADC module include:

- 10-bit ADC core with built-in S/H
- Fast conversion time (S/H + Conversion) of 500 ns
- 5-channel, muxed inputs
- Autosequencing capability provides up to 16 “autoconversions” in a single session. Each conversion can be programmed to select any 1 of 5 input channels
- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer (i.e., two cascaded 8-state sequencers)
- Sixteen result registers (individually addressable) to store conversion values
  - The digital value of the input analog voltage is derived by:

$$\text{Digital Value} = 1023 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{V_{REFHI} - V_{REFLO}}$$

  NOTE: V_{REFLO} is internally tied to V_{SSA}; V_{REFHI} is internally tied to V_{CCA}.
- Multiple triggers as sources for the start-of-conversion (SOC) sequence
  - S/W – software immediate start
  - EVA – Event manager A (multiple event sources within EVA)
  - Ext – External pin (ADCSOC)
- Flexible interrupt control allows interrupt request on every end-of-sequence (EOS) or every other EOS
- Sequencer can operate in “start/stop” mode, allowing multiple “time-sequenced triggers” to synchronize conversions
- EVA triggers can operate independently in dual-sequencer mode
- Sample-and-hold (S/H) acquisition time window has separate prescale control
- Built-in calibration mode
- Built-in self-test mode

NOTE: The 2401A ADC module is identical to the LF2407A ADC module. However, only channels ADC0 through ADC4 are bonded out of the device. For this reason, the valid values for the CONVnn bit fields in the CHSELSEQn registers are from 0 to 4. Attempting to convert channels 5 through 15 would yield indeterminate results.

enhanced analog-to-digital converter (ADC) module (continued)

The ADC module in the 2401A has been enhanced to provide flexible interface to the event manager (EVA). The ADC interface is built around a fast, 10-bit ADC module with total conversion time of 500 ns (S/H + conversion). The ADC module has 5 channels to service EVA. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module. Figure 5 shows the block diagram of the 2401A ADC module.

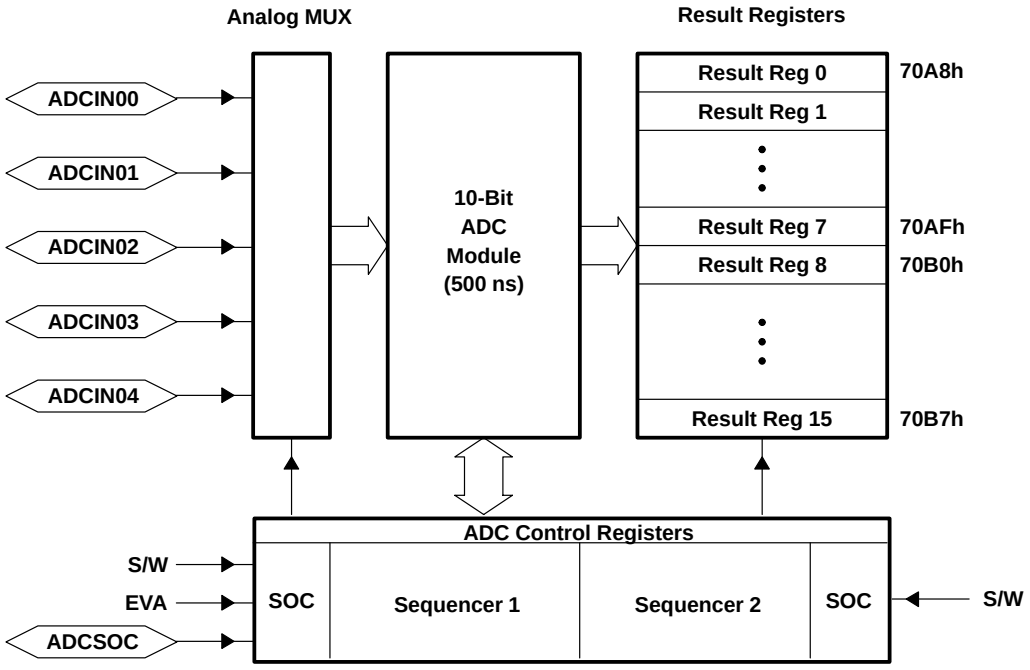


Figure 5. Block Diagram of the 2401A ADC Module

To obtain the specified accuracy of the ADC, proper board layout is very critical. To the best extent possible, traces leading to the ADCINn pins should not run in close proximity to the digital signal paths. This is to minimize switching noise on the digital lines from getting coupled to the ADC inputs. Furthermore, proper isolation techniques must be used to isolate the ADC module power pins (such as V_{CCA} and V_{SSA}) from the digital supply.

serial communications interface (SCI) module

The 2401A device includes a serial communications interface (SCI) module. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register. Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

NOTE: Both pins can be used as GPIO if not used for SCI.

- Baud rate programmable to 64K different rates
  - Up to 2500 Kbps at 40-MHz CPUCLK
- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (non-return-to-zero) format
- Ten SCI module control registers located in the control register frame beginning at address 7050h

NOTE: All registers in this module are 8-bit registers that are connected to the 16-bit peripheral bus. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Figure 6 shows the SCI module block diagram.

serial communications interface (SCI) module (continued)

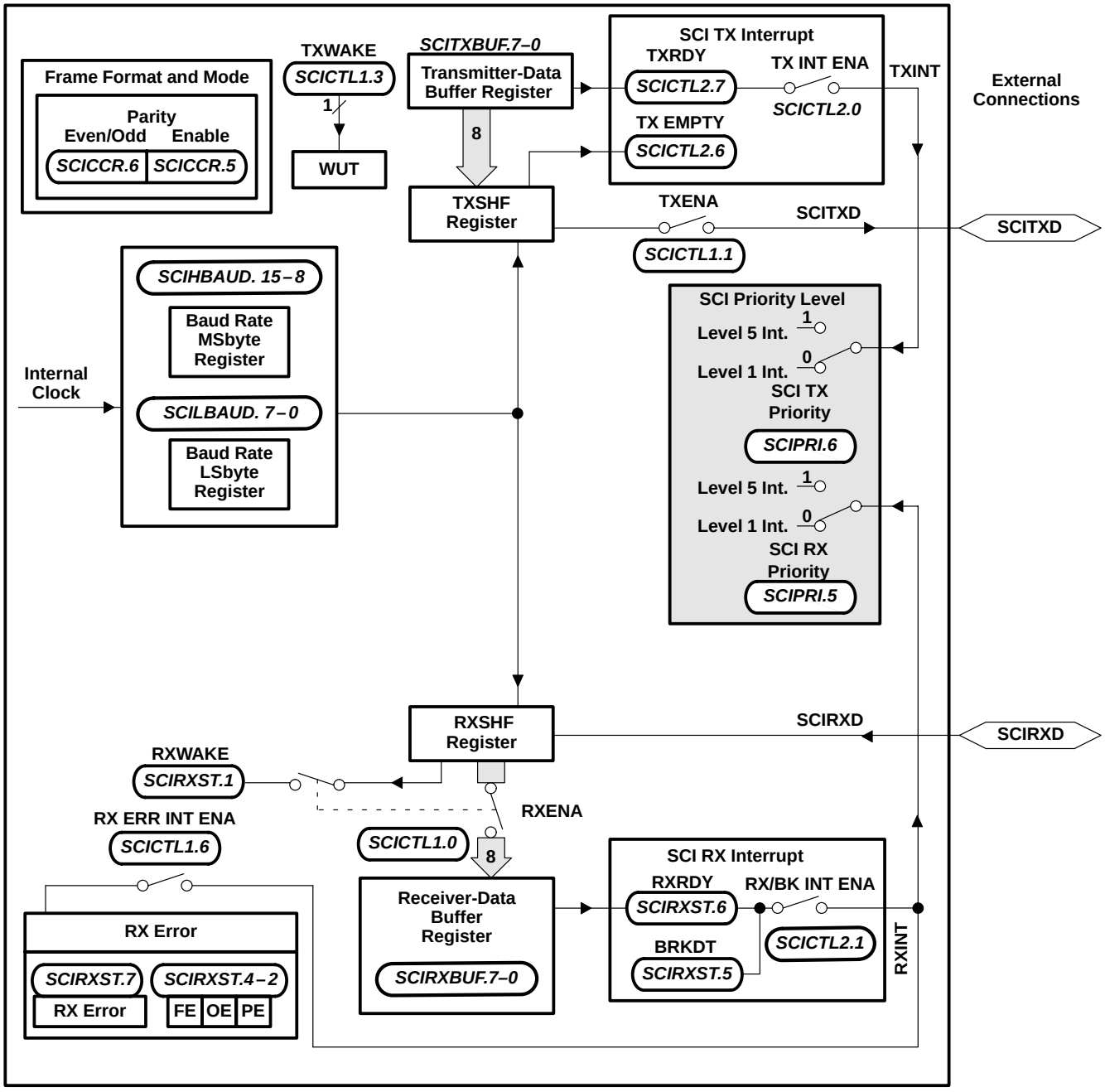


Figure 6. Serial Communications Interface (SCI) Module Block Diagram

PLL-based clock module

The 2401A has an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 3-bit ratio control to select different CPU clock rates. See Figure 7 for the PLL Clock Module Block Diagram and Table 7 for clock rates.

The PLL-based clock module provides two modes of operation:

- Crystal-operation
  This mode allows the use of an external crystal/resonator to provide the time base to the device.
- External clock source operation
  This mode allows the internal oscillator to be bypassed. The device clocks are generated from an external clock source input on the XTAL1/CLKIN pin. In this case, an external oscillator clock is connected to the XTAL1/CLKIN pin.

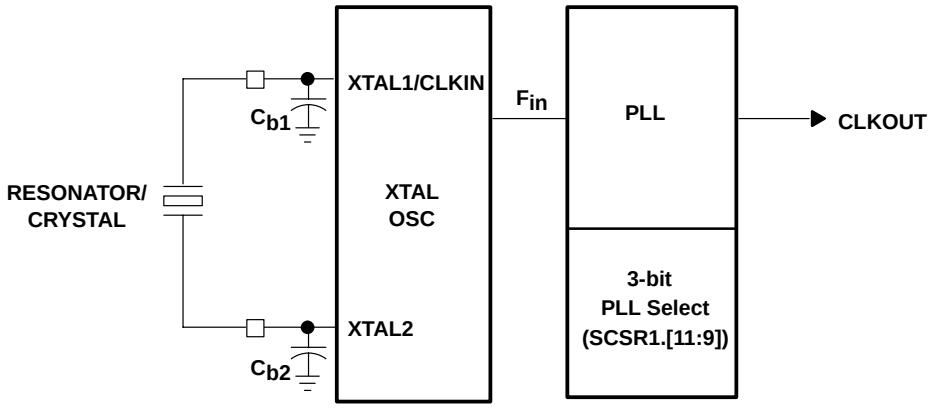


Figure 7. PLL Clock Module Block Diagram

Table 7. PLL Clock Selection Through Bits (11–9) in SCSR1 Register

CLK PS2	CLK PS1	CLK PS0	CLKOUT
0	0	0	$4 \times F_{in}$
0	0	1	$2 \times F_{in}$
0	1	0	$1.33 \times F_{in}$
0	1	1	$1 \times F_{in}$
1	0	0	$0.8 \times F_{in}$
1	0	1	$0.66 \times F_{in}$
1	1	0	$0.57 \times F_{in}$
1	1	1	$0.5 \times F_{in}$

Default multiplication factor after reset is (1,1,1), i.e., $0.5 \times F_{in}$.

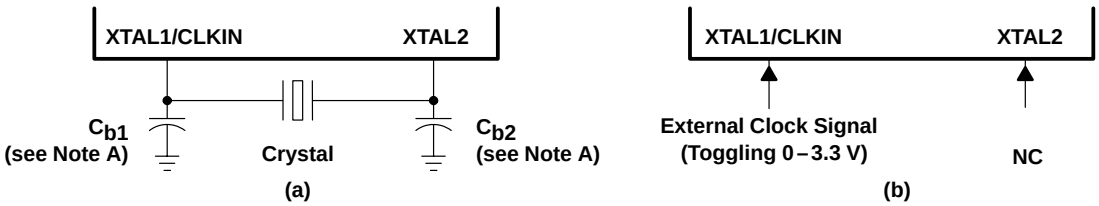
CAUTION:
The bootloader sets the PLL to x2 or x4 option. If the bootloader is used, the value of CLKIN used should not force CLKOUT to exceed the maximum rated device speed. See the "Boot ROM" section for more details.

external reference crystal clock option

The internal oscillator is enabled by connecting a crystal across the XTAL1/CLKIN and XTAL2 pins as shown in Figure 8a. The crystal should be in fundamental operation and parallel resonant, with an effective series resistance of 30 Ω–150 Ω and a power dissipation of 1 mW; it should be specified at a load capacitance of 20 pF.

external reference oscillator clock option

The internal oscillator is disabled by connecting a clock signal to XTAL1/CLKIN and leaving the XTAL2 input pin unconnected as shown in Figure 8b.



NOTE A: TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the DSP chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will ensure start-up and stability over the entire operating range.

Figure 8. Recommended Crystal / Clock Connection

low-power modes

The 2401A has an IDLE instruction. When executed, the IDLE instruction stops the clocks to all circuits in the CPU, but the clock output from the CPU continues to run. With this instruction, the CPU clocks can be shut down to save power while the peripherals (clocked with CLKOUT) continue to run. The CPU exits the IDLE state if it is reset, or, if it receives an interrupt request.

clock domains

All 2401A-based devices have two clock domains:

1. CPU clock domain – consists of the clock for most of the CPU logic
2. System clock domain – consists of the peripheral clock (which is derived from CLKOUT of the CPU) and the clock for the interrupt logic in the CPU.

When the CPU goes into IDLE mode, the CPU clock domain is stopped while the system clock domain continues to run. This mode is also known as IDLE1 mode. The 2401A CPU also contains support for a second IDLE mode, IDLE2. By asserting IDLE2 to the 2401A CPU, both the CPU clock domain and the system clock domain are stopped, allowing further power savings. A third low-power mode, HALT mode, the deepest, is possible if the oscillator and WDCLK are also shut down when in IDLE2 mode.

Two control bits, LPM1 and LPM0, specify which of the three possible low-power modes is entered when the IDLE instruction is executed (see Table 8). These bits are located in the System Control and Status Register 1 (SCSR1), and they are described in the *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357A).

clock domains (continued)

Table 8. Low-Power Modes Summary

LOW-POWER MODE	LPMx BITS SCSR1 [13:12]	CPU CLOCK DOMAIN	SYSTEM CLOCK DOMAIN	WDCLK STATUS	PLL STATUS	OSC STATUS	FLASH POWER	EXIT CONDITION
CPU running normally	XX	On	On	On	On	On	On	—
IDLE1 – (LPM0)	00	Off	On	On	On	On	On	Peripheral Interrupt, External Interrupt, Reset, $\overline{\text{PDPINTA}}$
IDLE2 – (LPM1)	01	Off	Off	On	On	On	On	Wakeup Interrupts, External Interrupt, Reset, $\overline{\text{PDPINTA}}$
HALT – (LPM2) [PLL/OSC power down]	1X	Off	Off	Off	Off	Off	Off†	Reset, $\overline{\text{PDPINTA}}$

† The Flash must be powered down by the user code prior to entering LPM2. For more details, see the *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357A).

other power-down options

2401A devices have clock-enable bits to the following on-chip peripherals: ADC, SCI, and EVA. Clock to these peripherals are disabled after reset; thus, start-up power can be low for the device.

Depending on the application, these peripherals can be turned on/off to achieve low power.

Refer to the SCSR1 register for details on the peripheral clock enable bits.

digital I/O and shared pin functions

The 2401A has up to 13 general-purpose, bidirectional, digital I/O (GPIO) pins—most of which are shared between primary functions and I/O. Most I/O pins of the 2401A are shared with other functions. The digital I/O ports module provides a flexible method for controlling both dedicated I/O and shared pin functions. All I/O and shared pin functions are controlled using eight 16-bit registers. These registers are divided into two types:

- Output Control Registers — used to control the multiplexer selection that chooses between the primary function of a pin or the general-purpose I/O function.
- Data and Control Registers — used to control the data and data direction of bidirectional I/O pins.

description of shared I/O pins

The control structure for shared I/O pins is shown in Figure 9, where each pin has three bits that define its operation:

- Mux control bit — this bit selects between the primary function (1) and I/O function (0) of the pin.
- I/O direction bit — if the I/O function is selected for the pin (mux control bit is set to 0), this bit determines whether the pin is an input (0) or an output (1).
- I/O data bit — if the I/O function is selected for the pin (mux control bit is set to 0) and the direction selected is an input, data is read from this bit; if the direction selected is an output, data is written to this bit.

The mux control bit, I/O direction bit, and I/O data bit are in the I/O control registers.

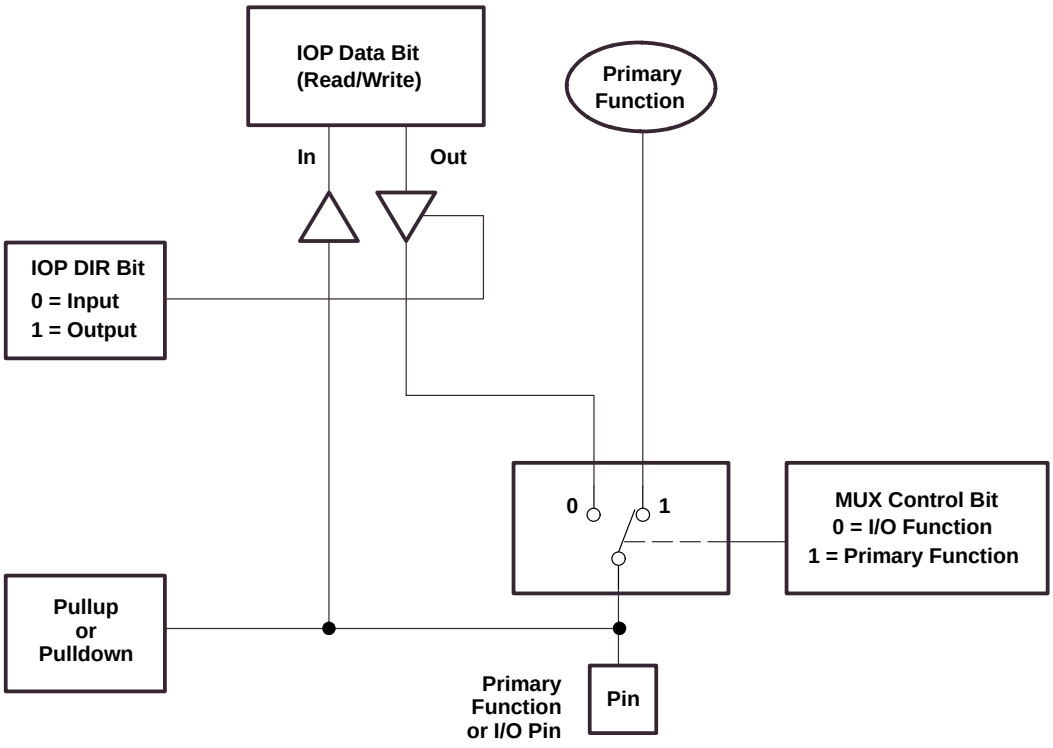


Figure 9. Shared Pin Configuration

A summary of shared pin configurations and associated bits is shown in Table 9.

description of shared I/O pins (continued)

Table 9. Shared Pin Configurations

PIN FUNCTION SELECTED		MUX CONTROL REGISTER (name.bit #)	MUX CONTROL VALUE AT RESET (MCRx.n)	I/O PORT DATA AND DIRECTION†		
(MCA.n = 1) Primary Function	(MCA.n = 0) Secondary Function			REGISTER	DATA BIT NO.‡	DIR BIT NO.§
				PORT A		
$\overline{\text{PDPINTA}}$	IOPA0	MCRA.0	0	PADATDIR	0	8
PWM1	IOPA1	MCRA.1	0	PADATDIR	1	9
PWM2	IOPA2	MCRA.2	0	PADATDIR	2	10
PWM3	IOPA3	MCRA.3	0	PADATDIR	3	11
PWM4	IOPA4	MCRA.4	0	PADATDIR	4	12
PWM5	IOPA5	MCRA.5	0	PADATDIR	5	13
PWM6	IOPA6	MCRA.6	0	PADATDIR	6	14
CLKOUT	XINT2/ADCSOC/ CAP1/IOPA7	MCRA.7	0	PADATDIR	7	15
				PORT B		
T2PWM	XINT1/IOPB0	MCRA.8	0	PBDATDIR	0	8
IOPB1	IOPB1	MCRA.9	0	PBDATDIR	1	9
IOPB2	IOPB2	MCRA.10	0	PBDATDIR	2	10
SCITXD	IOPB3	MCRA.11	0	PBDATDIR	3	11
SCIRXD	IOPB4	MCRA.12	0	PBDATDIR	4	12
OPB5	OPB5	MCRA.13	0	PBDATDIR	5	13
–		MCRA.14	0	PBDATDIR	6	14
–		MCRA.15	0	PBDATDIR	7	15

† Valid only if the I/O function is selected on the pin
‡ If the GPIO pin is configured as an output, these bits can be written to. If the pin is configured as an input, these bits are read from.
§ If the DIR bit is 0, the GPIO pin functions as an input. For a value of 1, the pin is configured as an output.

digital I/O control registers

Table 10 lists the registers available in the digital I/O module. As with other 2401A peripherals, these registers are memory-mapped to the data space.

Table 10. Addresses of Digital I/O Control Registers

ADDRESS	REGISTER	NAME
7090h	MCRA	I/O mux control register A
7098h	PADATDIR	I/O port A data and direction register
709Ah	PBDATDIR	I/O port B data and direction register

CAUTION:
The bit definitions of the MCRA, PADATDIR, and PBDATDIR registers are *not* compatible with those of other 24x/240x devices.

watchdog (WD) timer module

The 2401A device includes a watchdog (WD) timer module. The WD function of this module monitors software and hardware operation by generating a system reset if it is not periodically serviced by software by having the correct key written. The WD timer operates independently of the CPU. It does not need any CPU initialization to function. When a system reset occurs, the WD timer defaults to the fastest WD timer rate available (WDCLK signal = CLKOUT/512). As soon as reset is released internally, the CPU starts executing code, and the WD timer begins incrementing. This means that, to avoid a premature reset, WD setup should occur early in the power-up sequence. See Figure 10 for a block diagram of the WD module. The WD module features include the following:

- WD Timer
  - Seven different WD overflow rates
  - A WD-reset key (WDKEY) register that clears the WD counter when a correct value is written, and generates a system reset if an incorrect value is written to the register
  - WD check bits that initiate a system reset if an incorrect value is written to the WD control register (WDCR)
- Automatic activation of the WD timer, once system reset is released
  - Three WD control registers located in control register frame beginning at address 7020h.

NOTE: All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte, the upper byte is read as zeros. Writing to the upper byte has no effect.

Table 11 shows the different WD overflow (time-out) selections. Figure 10 shows the WD block diagram.

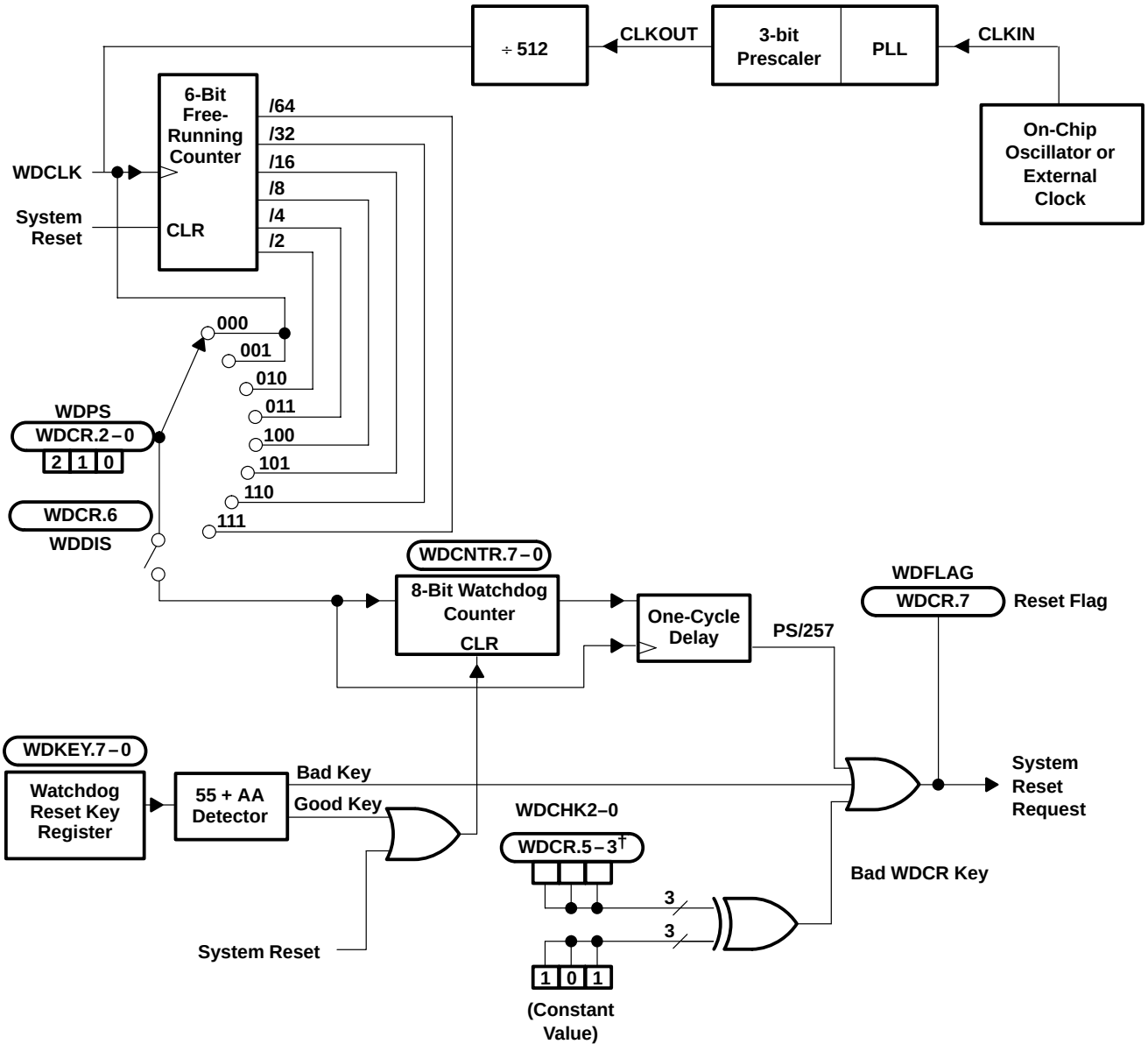
The watchdog can be disabled in software by writing ‘1’ to bit 6 of the WDCR register (WDCR.6) while bit 5 of the SCSR2 register (SCSR2.5) is 1. If SCSR2.5 is 0, the watchdog will not be disabled. SCSR2.5 is equivalent to the WDDIS pin of the TMS320F243/241 devices.

Table 11. WD Overflow (Time-out) Selections

WD PRESCALE SELECT BITS			WDCLK DIVIDER	WATCHDOG CLOCK RATE†
WDPS2	WDPS1	WDPS0		FREQUENCY (Hz)
0	0	X‡	1	WDCLK/1
0	1	0	2	WDCLK/2
0	1	1	4	WDCLK/4
1	0	0	8	WDCLK/8
1	0	1	16	WDCLK/16
1	1	0	32	WDCLK/32
1	1	1	64	WDCLK/64

† WDCLK = CLKOUT/512
‡ X = Don’t care

watchdog (WD) timer module (continued)



† Writing to bits WDCR.5 – 3 with anything but the correct pattern (101) generates a system reset.

Figure 10. Block Diagram of the WD Module

development support

Texas Instruments (TI) offers an extensive line of development tools for the 240x generation of DSPs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of 240x-based applications:

Software Development Tools:
Assembler/linker
Simulator
Optimizing ANSI C compiler
Application algorithms
C/Assembly debugger and code profiler

Hardware Development Tools:
Emulator XDS510™ (supports x24x multiprocessor system debug)
TMS320LF2407 EVM (Evaluation module for 2407 DSP)

The *TMS320 DSP Development Support Reference Guide* (literature number SPRU011) contains information about development support products for all TMS320™ DSP family member devices, including documentation. Refer to this document for further information about TMS320™ DSP documentation or any other TMS320™ DSP support products from Texas Instruments. There is also an additional document, the *TMS320 Third-Party Support Reference Guide* (literature number SPRU052), which contains information from other companies in the industry regarding products related to the TMS320™ DSPs . To receive copies of TMS320™ DSP literature, contact the Literature Response Center at 800-477-8924.

See Table 12 and Table 13 for complete listings of development support tools for the 240x. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

Table 12. Development Support Tools

DEVELOPMENT TOOL	PLATFORM	PART NUMBER
Software – Code Generation Tools		
Assembler/Linker	PC™, Windows™ 95	TMDS3242850-02
C Compiler/Assembler/Linker	PC, Windows 95	TMDS3242855-02
Software – Emulation Debug Tools		
LF2407 eZdsp	PC	TMDS3P761119
Code Composer 4.12, Code Generation 7.0	PC	TMDS324012xx
Hardware – Emulation Debug Tools		
XDS510XL™ Board (ISA card), w/JTAG cable	PC	TMDS00510
XDS510PP™ Pod (Parallel Port) w/JTAG cable	PC	TMDS00510PP

PRODUCT PREVIEW

PC is a trademark of International Business Machines Corp.
Windows is a registered trademark of Microsoft Corporation.
XDS510XL and XDS510PP are trademarks of Texas Instruments.

development support (continued)

Table 13. TMS320x24x-Specific Development Tools

DEVELOPMENT TOOL	PLATFORM	PART NUMBER
Hardware – Evaluation/Starter Kits		
TMS320LF2407A EVM	PC, Windows 95, Windows™ 98	TMDX3P701016
TMS320F240 EVM	PC	TMDX326P124X
TMS320F243 EVM	PC, Windows 95	TMDS3P604030

device and development support tool nomenclature

To designate the stages in the product development cycle, Texas Instruments assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS). This development flow is defined below.

Support tool development evolutionary flow:

TMDX Development support product that has not completed TI's internal qualification testing

TMDS Fully qualified development support product

TMX and TMP devices and TMDX development support tools are shipped against the following disclaimer:

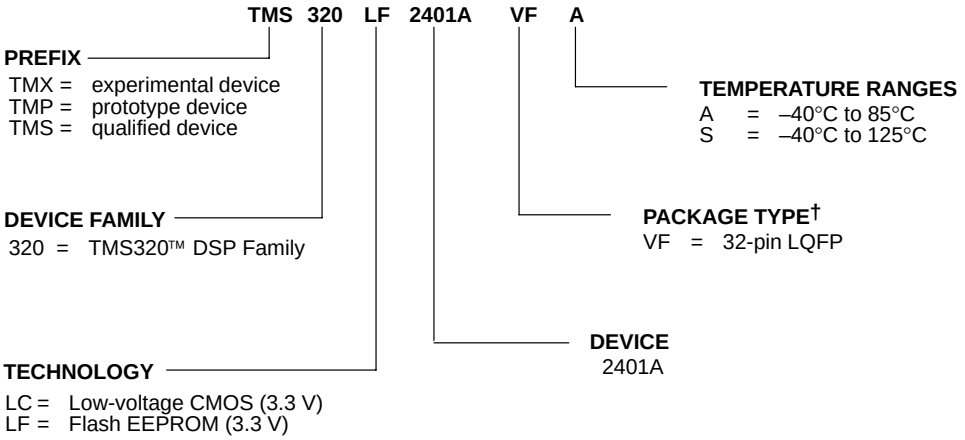
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development support tools have been fully characterized, and the quality and reliability of the device have been fully demonstrated. TI's standard warranty applies.

device and development support tool nomenclature (continued)

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, VF) and temperature range (for example, S). Figure 11 provides a legend for reading the complete TMS320LF2401A device name.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.



† LQFP = Low-Profile Quad Flatpack

Figure 11. TMS320LF2401A Device Nomenclature

PRODUCT PREVIEW

documentation support

Extensive documentation supports all of the TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's guides for all devices and development support tools; and hardware and software applications. Useful reference documentation includes:

- User Guides
  - *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357A)
  - *TMS320C240 DSP Controllers CPU, System, and Instruction Set Reference Guide* (literature number SPRU160)
- Data Sheets
  - *TMS320LF2407, TMS320LF2406, TMS320LF2402 DSP Controllers* (literature number SPRS094)
  - *TMS320LF2407A, TMS320LF2406A, TMS320LF2403A, TMS320LF2402A, TMS320LC2406A, TMS320LC2404A, TMS320LC2402A DSP Controllers* (literature number SPRS145)
- Application Reports
  - *3.3V DSP for Digital Motor Control* (literature number SPRA550)

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320™ DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320™ DSP customers on product information.

Updated information on the TMS320™ DSP controllers can be found on the worldwide web at: **http://www.ti.com**.

To send comments regarding the TMS320LF2401A data sheet (literature number SPRS161), use the *comments@books.sc.ti.com* email address, which is a repository for feedback. For questions and support, contact the Product Information Center listed at the **http://www.ti.com/sc/docs/pic/home.htm** site.

NOTE: The LF2401A device has reduced peripheral functionality compared to other 24x/240x devices. While peripherals such as SPI and CAN are absent on the LF2401A, peripherals such as EV and ADC have reduced functionality. For example, in the case of EV, there is no QEP unit and the Capture unit has only one capture pin (as opposed to three or six pins in other devices). The ADC has only five input channels (as opposed to eight or sixteen channels in other devices). For these reasons, some bits that are valid in other 24x/240x devices are not applicable in the LF2401A. The registers and their valid bits are described in Table 15, LF2401A DSP Peripheral Register Description. For a description of those registers and bits that are valid, refer to the *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357A). Any exceptions to SPRU357A has been described in the respective peripheral sections in this data sheet.

absolute maximum ratings over operating free-air temperature ranges (unless otherwise noted)†

Supply voltage range, V_{DD}, V_{DDO}, and V_{CCA} (see Note 1) . . . . . – 0.3 V to 4.6 V
V_{CCP} range . . . . . – 0.3 V to 5.5 V
Input voltage range, V_{IN} . . . . . – 0.3 V to 4.6 V
Output voltage range, V_O . . . . . – 0.3 V to 4.6 V
Input clamp current, I_{IK} ($V_{IN} < 0$ or $V_{IN} > V_{CC}$) . . . . . ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ± 20 mA
Operating free-air temperature ranges, T_A: A version . . . . . – 40°C to 85°C
S version . . . . . – 40°C to 125°C
Junction temperature range, T_J . . . . . – 40°C to 150°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Clamp current stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions‡

				MIN	NOM	MAX	UNIT
V_{DD}/V_{DDO}	Supply voltage		$V_{DDO} = V_{DD} \pm 0.3$ V	3	3.3	3.6	V
V_{SS}	Supply ground			0	0	0	V
V_{CCA}§	ADC supply voltage			3	3.3	3.6	V
V_{CCP}	Flash programming supply voltage			4.75	5	5.25	V
f_{CLKOUT}	Device clock frequency (system clock)			4		40	MHz
V_{IH}	High-level input voltage		All inputs	2			V
V_{IL}	Low-level input voltage		All inputs			0.8	V
I_{OH}	High-level output source current, V_{OH} = 2.4 V		Output pins Group 1¶			– 2	mA
			Output pins Group 2¶			– 4	mA
			Output pins Group 3¶			– 8	mA
I_{OL}	Low-level output sink current, $V_{OL} = V_{OL}$ MAX		Output pins Group 1¶			2	mA
			Output pins Group 2¶			4	mA
			Output pins Group 3¶			8	mA
T_A	Free-air temperature	A version		– 40		85	°C
		S version		– 40		125	
T_J	Junction temperature			– 40	25	150	°C
N_f	Flash endurance for the array (Write/erase cycles)		– 40°C to 85°C		10K		cycles

‡ Refer to the mechanical data package page for thermal resistance values, Θ_{JA} (junction-to-ambient) and Θ_{JC} (junction-to-case).

§ V_{CCA} should not exceed V_{DD} by 0.3 V.

¶ Primary signals and their groupings:
Group 1: $\overline{\text{PDPINTA}}$/IOPA0, T2PWM, PWM1–PWM6 (IOPA1–IOPA6), IOPB1, OPB5, TMS/XF
Group 2: SCITXD/IOPB3, SCIRXD/IOPB4, TDO/IOPB2
Group 3: CAP1

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature ranges (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 3.0 V, I_{OH} = I_{OH}MAX	2.4			V
			All outputs at 50 μA	V_{DDO} – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL}MAX			0.4	V
I_{IL}	Input current (low level)	With pullup	V_{DD} = 3.3 V, V_{IN} = 0 V	–9	–16	–25	μA
		With pulldown				±2	
I_{IH}	Input current (high level)	With pullup	V_{DD} = 3.3 V, V_{IN} = V_{DD}			±2	μA
		With pulldown		9	16	25	
I_{OZ}	Output current, high-impedance state (off-state)		V_O = V_{DD} or 0 V			±2	μA
C_i	Input capacitance				2		pF
C_o	Output capacitance				3		pF

current consumption by power-supply pins over recommended operating free-air temperature ranges at 40-MHz CLOCKOUT†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Operational Current	Clock to all peripherals is enabled. CPU is running a simple loop code and no I/O pins are switching.		60	95	mA
I_{CCA}	ADC module current			5	15	mA

† I_{DD} is the current flowing into the V_{DD} and V_{DDO} pins.

current consumption by power-supply pins over recommended operating free-air temperature ranges during low-power modes at 40-MHz CLOCKOUT†

PARAMETER		MODE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Operational Current	LPM0	Clock to all peripherals is enabled. No I/O pins are switching.		72	96	mA
I_{CCA}	ADC module current				0.2	1	mA
I_{DD}	Operational Current	LPM1	Clock to all peripherals is disabled. No I/O pins are switching.		48	72	mA
I_{CCA}	ADC module current				0	0	mA
I_{DD}	Operational Current	LPM2	Clock to all peripherals is disabled.		200		μA
I_{CCA}	ADC module current				0	0	mA

† I_{DD} is the current flowing into the V_{DD} and V_{DDO} pins.

current consumption graphs

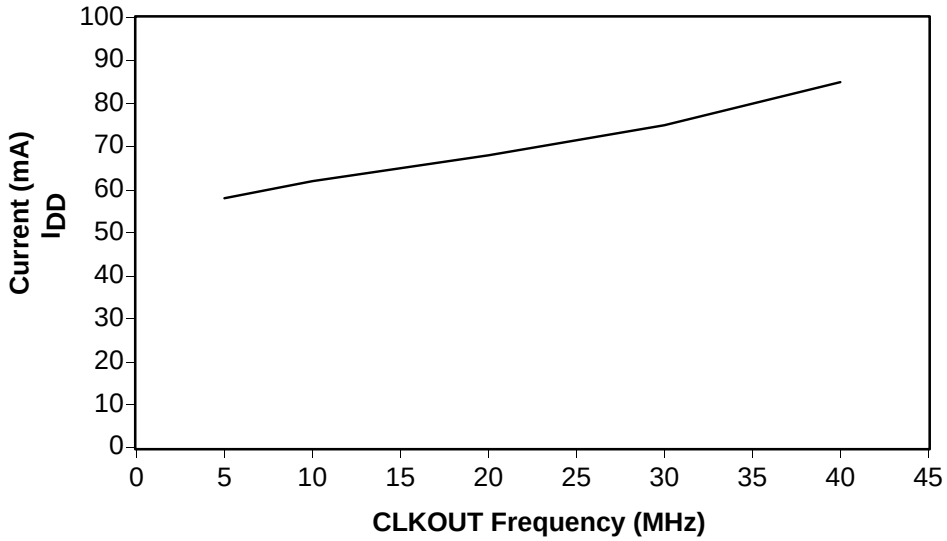


Figure 12. LF2401A Typical Current Consumption (With Peripheral Clocks Enabled)

reducing current consumption

240x DSPs incorporate a unique method to reduce the device current consumption. A reduction in current consumption can be achieved by turning off the clock to any peripheral module which is not used in a given application. Table 14 indicates the typical reduction in current consumption achieved by turning off the clocks to various peripherals. Refer to the *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357A) for further information on how to turn off the clock to the peripherals.

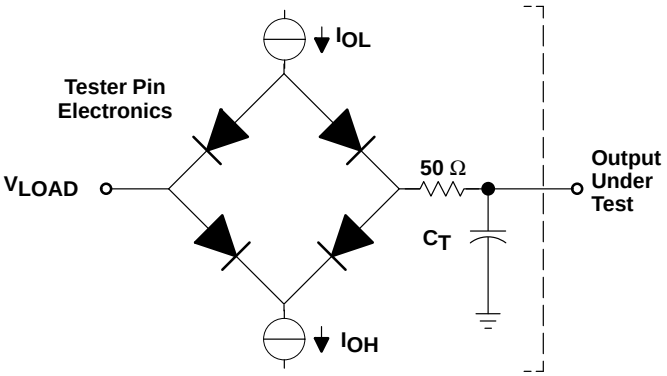
Table 14. Typical Current Consumption by Various Peripherals (at 40 MHz)

PERIPHERAL MODULE	CURRENT REDUCTION (mA)
EVA	6.1
ADC†	2.8†
SCI	1.9

† ADC current shown is at 30 MHz.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = 1.5 V
C_T = 50-pF typical load-circuit capacitance

Figure 13. Test Load Circuit

signal transition levels

The data in this section is shown for the 3.3-V version. Note that some of the signals use different reference voltages, see the recommended operating conditions table. Output levels are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.8 V.

Figure 14 shows output levels.

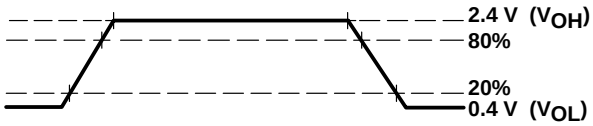


Figure 14. Output Levels

Output transition times are specified as follows:

- For a *high-to-low transition*, the level at which the output is said to be no longer high is below 80% of the total voltage range and lower and the level at which the output is said to be low is 20% of the total voltage range and lower.
- For a *low-to-high transition*, the level at which the output is said to be no longer low is 20% of the total voltage range and higher and the level at which the output is said to be high is 80% of the total voltage range and higher.

Figure 15 shows the input levels.

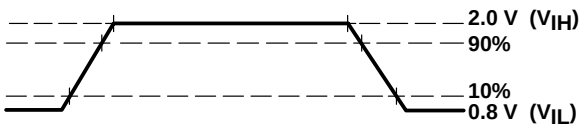


Figure 15. Input Levels

Input transition times are specified as follows:

- For a *high-to-low transition* on an input signal, the level at which the input is said to be no longer high is 90% of the total voltage range and lower and the level at which the input is said to be low is 10% of the total voltage range and lower.
- For a *low-to-high transition* on an input signal, the level at which the input is said to be no longer low is 10% of the total voltage range and higher and the level at which the input is said to be high is 90% of the total voltage range and higher.

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

CI	XTAL1
CO	CLKOUT
RS	RESET pin $\overline{RS}$
INT	XINT1, XINT2

Lowercase subscripts and their meanings:	
a	access time
c	cycle time (period)
d	delay time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)

Letters and symbols and their meanings:	
H	High
L	Low
V	Valid
X	Unknown, changing, or don’t care level
Z	High impedance

general notes on timing parameters

All output signals from the 2401A device (including CLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, refer to the appropriate cycle description section of this data sheet.

external reference crystal/clock with PLL circuit enabled

timings with the PLL circuit enabled

PARAMETER			MIN	MAX	UNIT
f_x	Input clock frequency†	Resonator	4	13	MHz
		Crystal	4	20	
		CLKIN	4	20	

† Input frequency should be adjusted (CLK PS bits in SCSR1 register) such that CLKOUT = 40 MHz maximum, 4 MHz minimum.

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$] (see Figure 16)

PARAMETER		PLL MODE	MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	×4 mode†	33			ns
$t_{f(CO)}$	Fall time, CLKOUT			4		ns
$t_{r(CO)}$	Rise time, CLKOUT			4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low		H–3	H	H+3	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high		H–3	H	H+3	ns
t_t	Transition time, PLL synchronized after $\overline{RS}$ pin high				$4096t_{c(CI)}$	ns

† Input frequency should be adjusted (CLK PS bits in SCSR1 register) such that CLKOUT = 40 MHz maximum, 4 MHz minimum.

timing requirements (see Figure 16)

		MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, XTAL1/CLKIN		250	ns
$t_{f(CI)}$	Fall time, XTAL1/CLKIN		5	ns
$t_{r(CI)}$	Rise time, XTAL1/CLKIN		5	ns
$t_{w(CIL)}$	Pulse duration, XTAL1/CLKIN low as a percentage of $t_{c(CI)}$	40	60	%
$t_{w(CIH)}$	Pulse duration, XTAL1/CLKIN high as a percentage of $t_{c(CI)}$	40	60	%

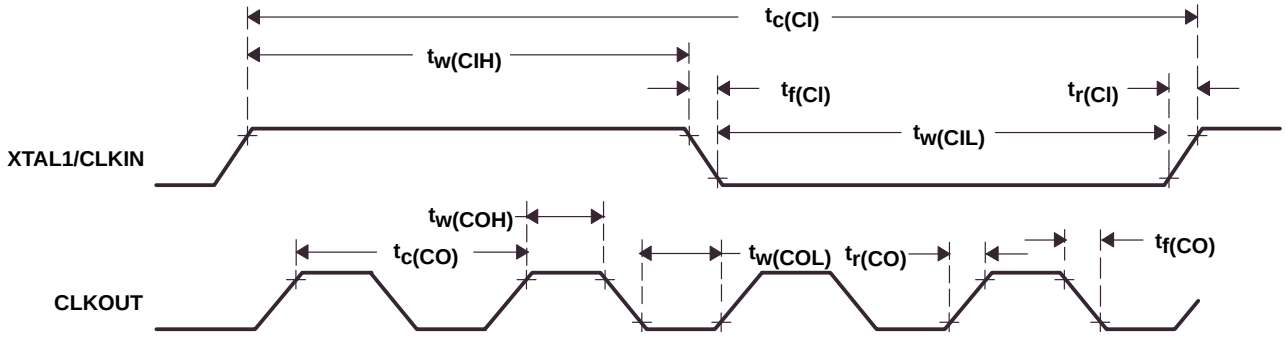
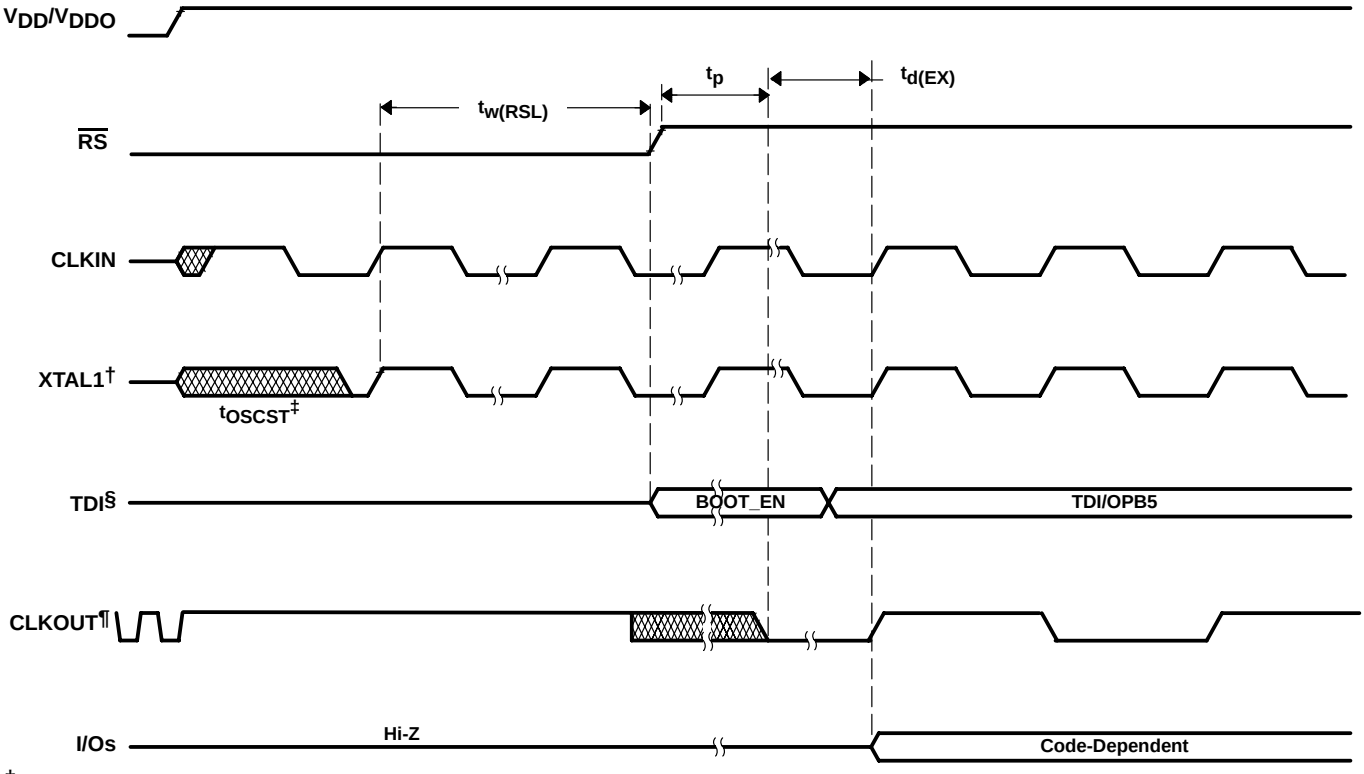


Figure 16. CLKIN-to-CLKOUT Timing with PLL and External Clock in ×4 Mode

$\overline{RS}$ timings

timing requirements for a reset [H = 0.5$t_{c(CO)}$] (see Figure 17 and Figure 18)

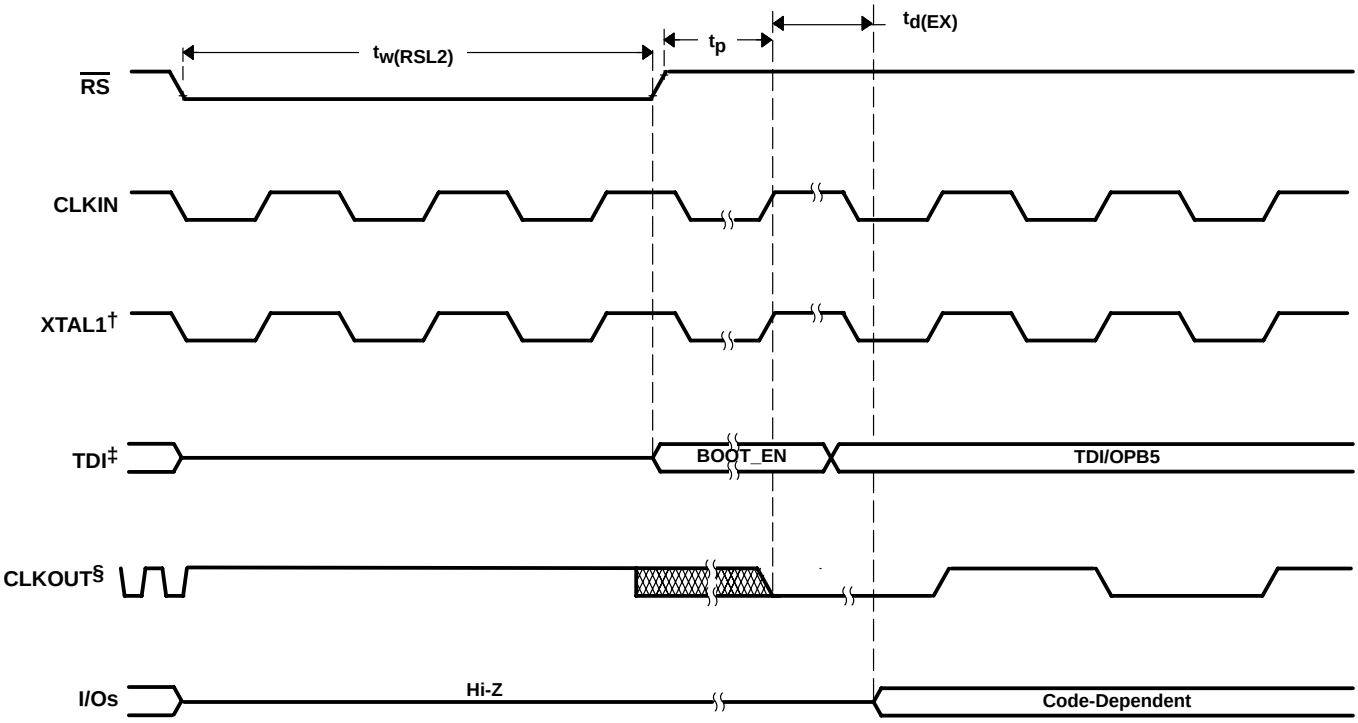
		MIN	NOM	MAX	UNIT
$t_{w(RSL)}$	Pulse duration, stable CLKIN to $\overline{RS}$ high	$8t_{c(CI)}$			cycles
$t_{w(RSL2)}$	Pulse duration, $\overline{RS}$ low	$8t_{c(CI)}$			cycles
t_p	PLL lock-up time			$4096t_{c(CI)}$	cycles
$t_{d(EX)}$	Delay time, reset vector executed after PLL lock time		36H		ns



† XTAL1 refers to internal oscillator clock if on-chip oscillator is used.
‡ t_{OSCST} is the oscillator start-up time, which is dependent on crystal/resonator and board design.
§ The TDI pin is used to determine whether or not the on-chip boot ROM is invoked in the BOOT_EN phase. In the "TDI/OPB5" phase, this pin functions as TDI (if $\overline{TRST}$ is high) or OPB5 (if $\overline{TRST}$ is low).
¶ Unlike other 24x/240x devices, the CLKOUT signal does not appear on the CLKOUT pin by default (after a device reset). The CLKOUT waveform depicted in the figure is present internally in the DSP. However, in order to route the internal CLKOUT signal to the XINT2/ADCSOC/CAP1/IOPA7/CLKOUT pin, bit 7 of the MCRA register must be programmed appropriately.

Figure 17. Power-on Reset

$\overline{RS}$ timings (continued)



† XTAL1 refers to internal oscillator clock if on-chip oscillator is used.
‡ The TDI pin is used to determine whether or not the on-chip boot ROM is invoked in the BOOT_EN phase. In the “TDI/OPB5” phase, this pin functions as TDI (if $\overline{TRST}$ is high) or OPB5 (if $\overline{TRST}$ is low).
§ Unlike other 24x/240x devices, the CLKOUT signal does not appear on the CLKOUT pin by default (after a device reset). The CLKOUT waveform depicted in the figure is present internally in the DSP. However, in order to route the internal CLKOUT signal to the XINT2/ADCSOC/CAP1/IOPA7/CLKOUT pin, bit 7 of the MCRA register must be programmed appropriately.

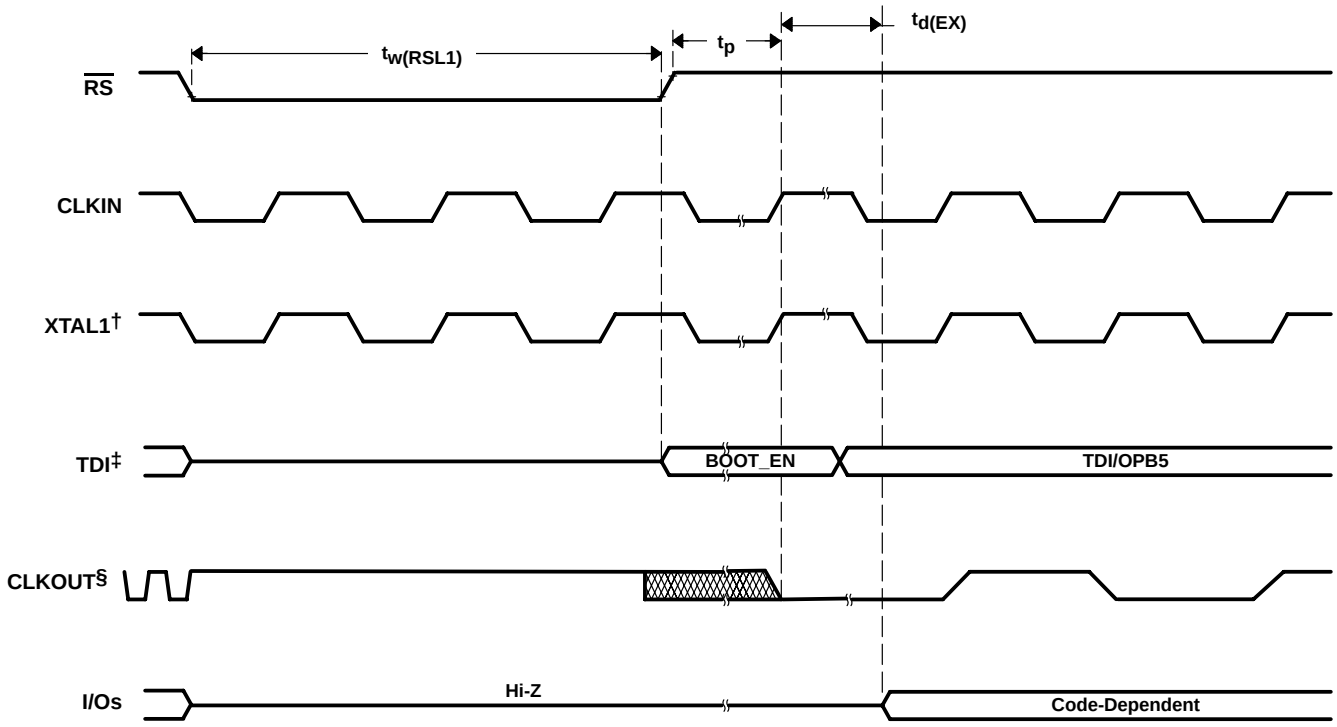
Figure 18. Warm Reset

$\overline{RS}$ timings (continued)

switching characteristics over recommended operating conditions for a reset [H = 0.5$t_{c(CO)}$] (see Figure 19)

PARAMETER		MIN	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, $\overline{RS}$ low†	$128t_{c(CI)}$		ns
$t_{d(EX)}$	Delay time, reset vector executed after PLL lock time	36H		ns
t_p	PLL lock time (input cycles)		$4096t_{c(CI)}$	ns

† The parameter $t_{w(RSL1)}$ refers to the time $\overline{RS}$ is an output.



† XTAL1 refers to internal oscillator clock if on-chip oscillator is used.

‡ The TDI pin is used to determine whether or not the on-chip boot ROM is invoked in the BOOT_EN phase. In the “TDI/OPB5” phase, this pin functions as TDI (if $\overline{TRST}$ is high) or OPB5 (if $\overline{TRST}$ is low).

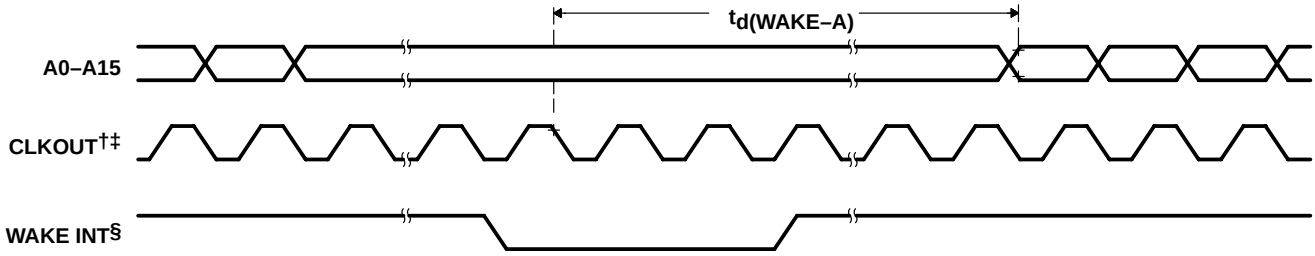
§ Unlike other 24x/240x devices, the CLKOUT signal does not appear on the CLKOUT pin by default (after a device reset). The CLKOUT waveform depicted in the figure is present internally in the DSP. However, in order to route the internal CLKOUT signal to the XINT2/ADCSOC/CAP1/IOPA7/CLKOUT pin, bit 7 of the MCRA register must be programmed appropriately.

Figure 19. Watchdog Initiated Reset

low-power mode timings

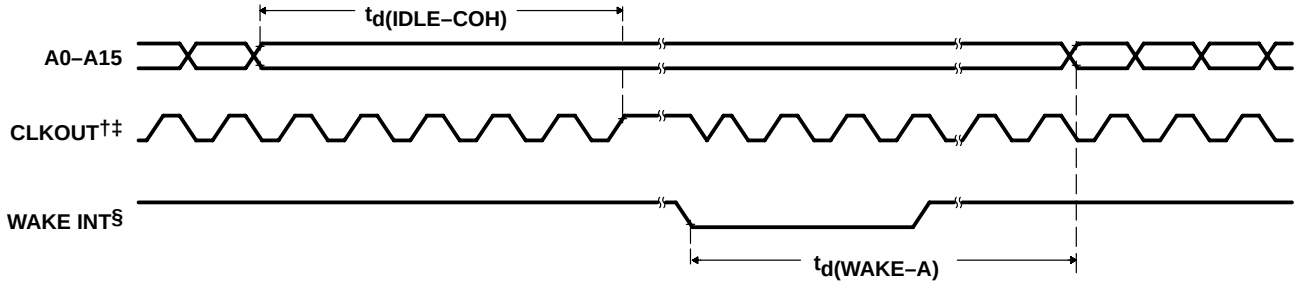
switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 20, Figure 21, and Figure 22)

PARAMETER		LOW-POWER MODES		MIN	TYP	MAX	UNIT
$t_{d(WAKE-A)}$	Delay time, CLKOUT switching to program execution resume	IDLE1	LPM0		$12 \times t_{c(CO)}$		ns
		IDLE2	LPM1		$15 \times t_{c(CO)}$		
$t_{d(IDLE-COH)}$	Delay time, Idle instruction executed to CLKOUT high	IDLE2	LPM1		$4t_{c(CO)}$		ns
$t_{d(WAKE-OSC)}$	Delay time, wakeup interrupt asserted to oscillator running	HALT {PLL/OSC power down}	LPM2		OSC start-up and PLL lock time		ms
$t_{d(IDLE-OSC)}$	Delay time, Idle instruction executed to oscillator power off				$4t_{c(CO)}$		ns
$t_{d(EX)}$	Delay time, reset vector executed after $\overline{RS}$ high				36H		ns



† In 2401A, CLKOUT will not be seen at the pin, only in some modes; it can be enabled in software.
‡ Unlike other 24x/240x devices, the CLKOUT signal does not appear on the CLKOUT pin by default (after a device reset). The CLKOUT waveform depicted in the figure is present internally in the DSP. However, in order to route the internal CLKOUT signal to the XINT2/ADCSOC/CAP1/IOPA7/CLKOUT pin, bit 7 of the MCRA register must be programmed appropriately.
§ WAKE INT can be any valid interrupt or RESET.

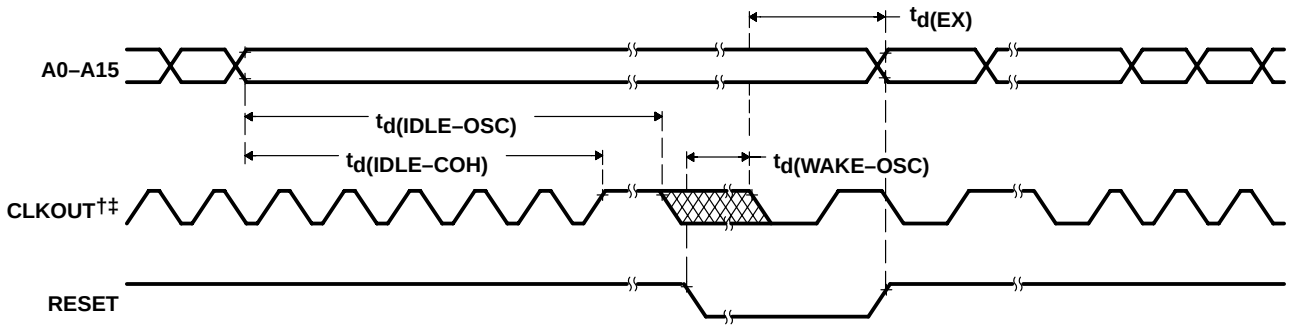
Figure 20. IDLE1 Entry and Exit Timing – LPM0



† In 2401A, CLKOUT will not be seen at the pin, only in some modes; it can be enabled in software.
‡ Unlike other 24x/240x devices, the CLKOUT signal does not appear on the CLKOUT pin by default (after a device reset). The CLKOUT waveform depicted in the figure is present internally in the DSP. However, in order to route the internal CLKOUT signal to the XINT2/ADCSOC/CAP1/IOPA7/CLKOUT pin, bit 7 of the MCRA register must be programmed appropriately.
§ WAKE INT can be any valid interrupt or RESET.

Figure 21. IDLE2 Entry and Exit Timing – LPM1

low-power mode timings (continued)



† In 2401A, CLKOUT will not be seen at the pin, only in some modes; it can be enabled in software.
‡ Unlike other 24x/240x devices, the CLKOUT signal does not appear on the CLKOUT pin by default (after a device reset). The CLKOUT waveform depicted in the figure is present internally in the DSP. However, in order to route the internal CLKOUT signal to the XINT2/ADCSOC/CAP1/IOPA7/CLKOUT pin, bit 7 of the MCRA register must be programmed appropriately.

Figure 22. HALT Mode – LPM2

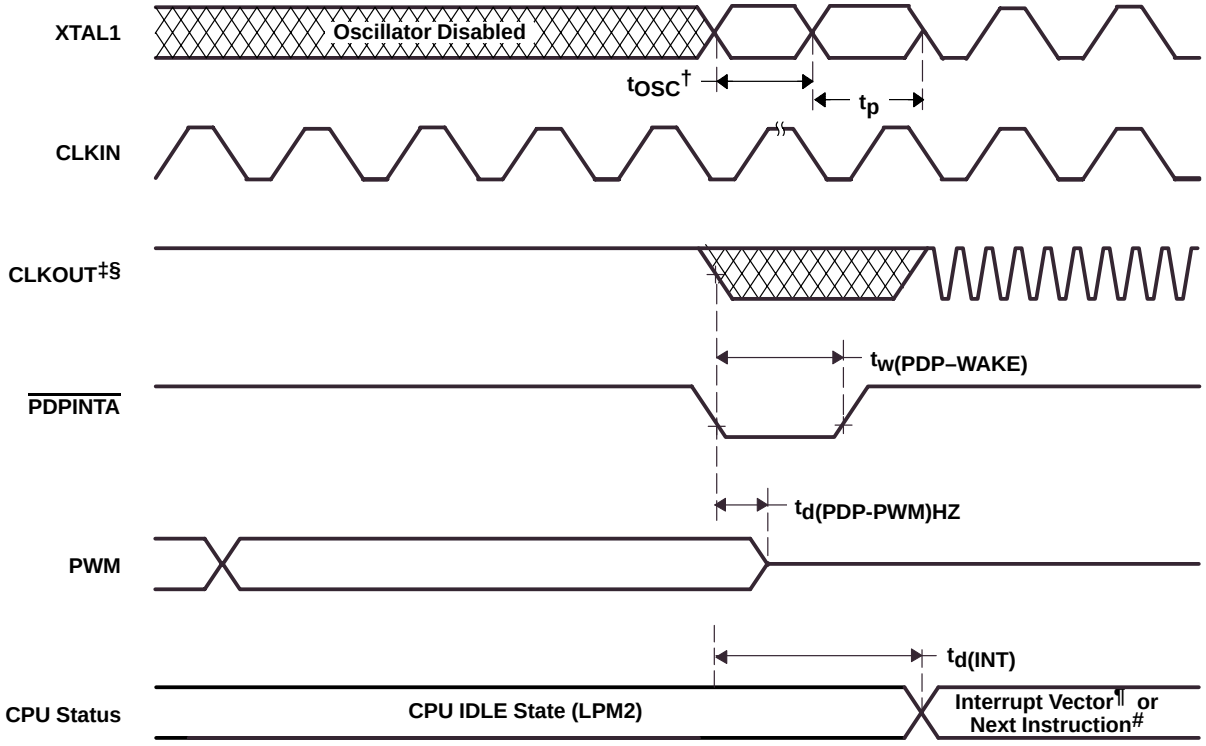
LPM2 wakeup timings

switching characteristics over recommended operating conditions (see Figure 23)

PARAMETER		MIN	MAX	UNIT
$t_{d(PDP-PWM)HZ}$	Delay time, $\overline{\text{PDPINTA}}$ low to PWM high-impedance state		12	ns
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch	$10t_{c(CO)}$		ns

timing requirements (see Figure 23)

			MIN	MAX	UNIT
$t_{w(PDP–WAKE)}$	Pulse duration, $\overline{\text{PDPINTA}}$ input low	if bit 6 of SCSR2 = 0	$6t_{c(CO)}$		ns
		if bit 6 of SCSR2 = 1	$12t_{c(CO)}$		
t_p	PLL lock-up time			$4096t_{c(CI)}$	cycles



† t_{OSC} is the oscillator start-up time.
‡ CLKOUT frequency after LPM2 wakeup will be the same as that upon entering LPM2 (x4 shown as an example).
§ Unlike other 24x/240x devices, the CLKOUT signal does not appear on the CLKOUT pin by default (after a device reset). The CLKOUT waveform depicted in the figure is present internally in the DSP. However, in order to route the internal CLKOUT signal to the XINT2/ADCSOC/CAP1/IOPA7/CLKOUT pin, bit 7 of the MCRA register must be programmed appropriately.
¶ PDPINTA interrupt vector, if PDPINTA interrupt is enabled.
# If PDPINTA interrupt is disabled.

Figure 23. LPM2 Wakeup Using $\overline{\text{PDPINTA}}$

XF timings

switching characteristics over recommended operating conditions (see Figure 24)

PARAMETER		MIN	MAX	UNIT
$t_{d(XF)}$	Delay time, CLKOUT high to XF high/low	–3	7	ns

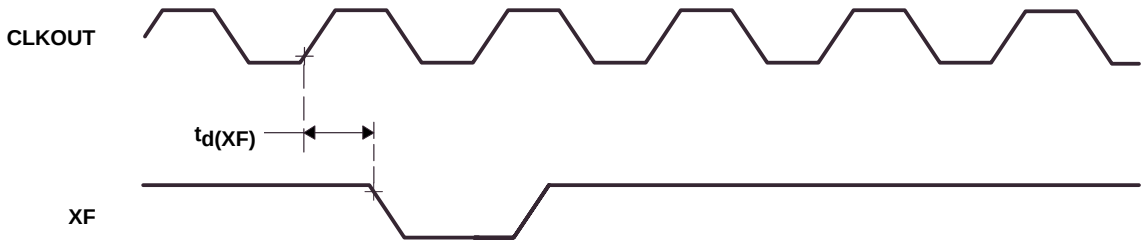


Figure 24. XF Timing

TIMING EVENT MANAGER INTERFACE

PWM timings

PWM refers to all PWM outputs on EVA.

switching characteristics over recommended operating conditions for PWM timing [H = 0.5$t_{c(CO)}$] (see Figure 25)

PARAMETER		MIN	MAX	UNIT
$t_{w(PWM)}$†	Pulse duration, PWMx output high/low	2H+5		ns
$t_{d(PWM)CO}$	Delay time, CLKOUT low to PWMx output switching		15	ns

† PWM outputs may be 100%, 0%, or increments of $t_{c(CO)}$ with respect to the PWM period.

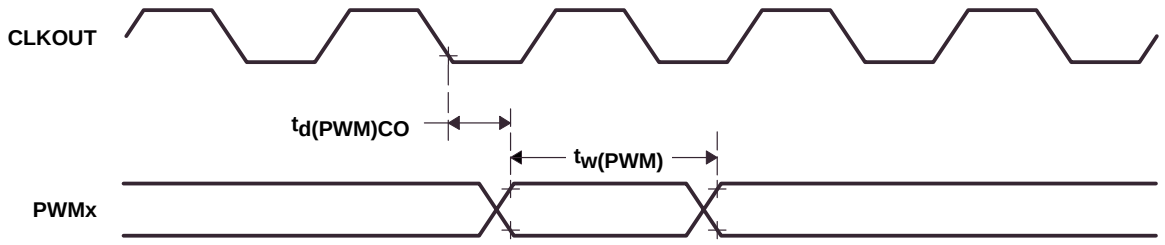


Figure 25. PWM Output Timing

capture timings

timing requirements (see Figure 26)

			MIN	MAX	UNIT
$t_{w(CAP)}$	Pulse duration, CAP1 input low/high	if bit 6 of SCSR2 = 0	$6t_{c(CO)}$		ns
		if bit 6 of SCSR2 = 1	$12t_{c(CO)}$		

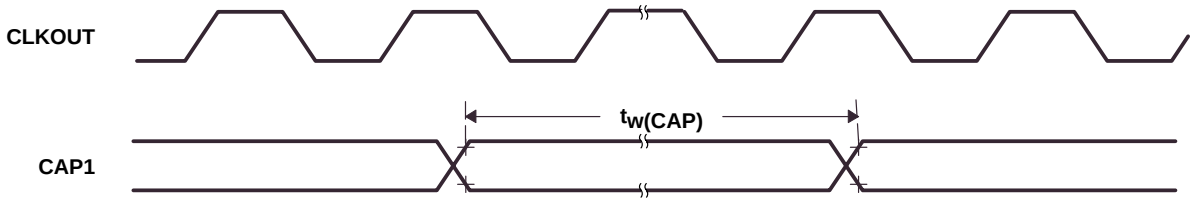


Figure 26. Capture Input Timing

interrupt timings

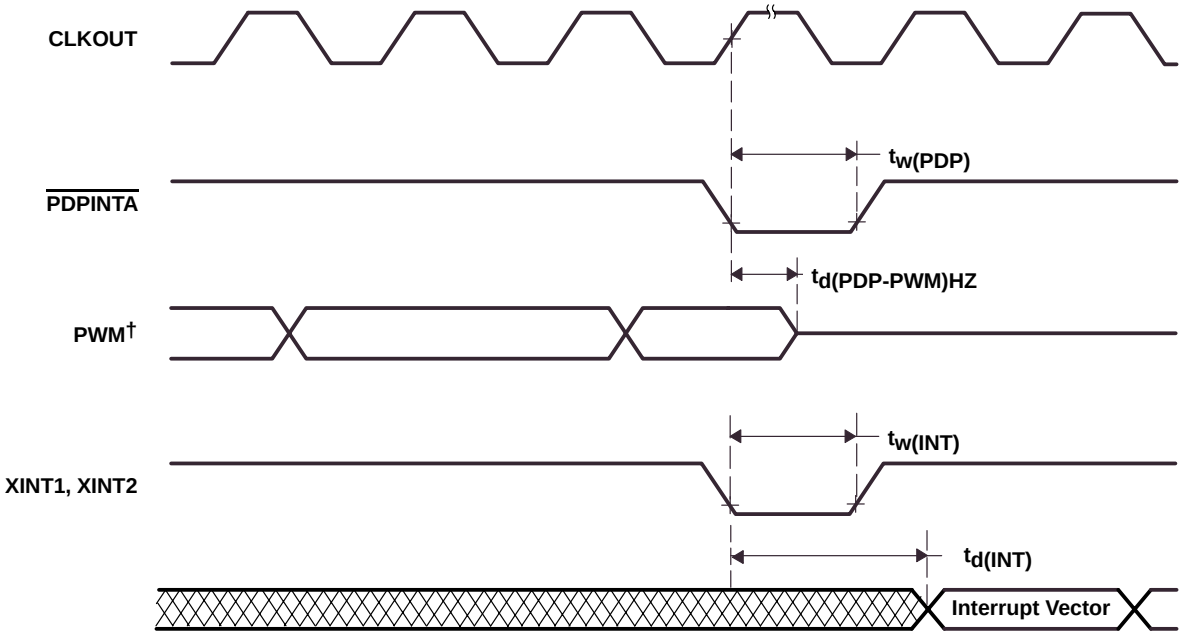
INT refers to XINT1 and XINT2.

switching characteristics over recommended operating conditions (see Figure 27)

PARAMETER		MIN	MAX	UNIT
$t_{d(PDP-PWM)HZ}$	Delay time, $\overline{\text{PDPINTA}}$ low to PWM high-impedance state		12	ns
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch	$10t_{c(CO)}$		ns

timing requirements (see Figure 27)

			MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	if bit 6 of SCSR2 = 0	$6t_{c(CO)}$		ns
		if bit 6 of SCSR2 = 1	$12t_{c(CO)}$		
$t_{w(PDP)}$	Pulse duration, $\overline{\text{PDPINTA}}$ input low	if bit 6 of SCSR2 = 0	$6t_{c(CO)}$		ns
		if bit 6 of SCSR2 = 1	$12t_{c(CO)}$		



† PWM refers to **all** the PWM pins in the device (i.e., PWMn and TnPWM pins). The state of the PWM pins after $\overline{\text{PDPINTA}}$ is taken high depends on the state of the FCOMPOE bit.

Figure 27. Power Drive Protection Interrupt Timing

general-purpose input/output timings

switching characteristics over recommended operating conditions (see Figure 28)

PARAMETER			MIN	MAX	UNIT
$t_{d(GPO)CO}$	Delay time, CLKOUT low to GPIO low/high	All GPIOs		9	ns
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		6	ns

timing requirements [H = 0.5$t_{c(CO)}$] (see Figure 29)

		MIN	MAX	UNIT
$t_{w(GPI)}$	Pulse duration, GPI high/low	2H+15		ns

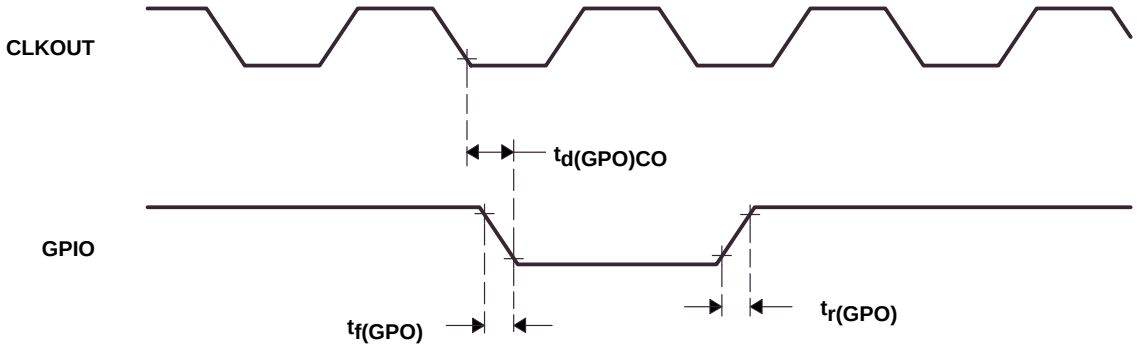


Figure 28. General-Purpose Output Timing

Figure 29. General-Purpose Input Timing

PRODUCT PREVIEW

10-bit analog-to-digital converter (ADC)

The 10-bit ADC has a separate power bus for its analog circuitry. These pins are referred to as V_{CCA} and V_{SSA}. The power bus isolation is to enhance ADC performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS} and V_{CC} from coupling into the ADC analog stage. All ADC specifications are given with respect to V_{SSA} unless otherwise noted.

Resolution . . . . . 10-bit (1024 values)
Monotonic . . . . . Assured
Output conversion mode . . . . . 000h to 3FFh (000h for $V_I \le V_{SSA}$; 3FFh for $V_I \ge V_{CCA}$)
Conversion time (including sample time) . . . . . 500 ns

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CCA}†	Analog supply voltage	3.0	3.3	3.6	V
V_{SSA}†	Analog ground		0		V
V_{AI}	Analog input voltage, ADCIN00–ADCIN07	V_{REFLO}		V_{REFHI}	V

† V_{CCA} and V_{SSA} must be stable, within ±1/2 LSB of the required resolution, during the entire conversion time.

ADC operating frequency

	MIN	MAX	UNIT
ADC operating frequency	4	40	MHz

PRODUCT PREVIEW

operating characteristics over recommended operating condition ranges†

PARAMETER		DESCRIPTION		MIN	TYP	MAX	UNIT
I_{CCA}	Analog supply current	V_{CCA} = 3.3 V			10	15	mA
		V_{CCA} = V_{REFHI} = 3.3 V	PLL or OSC power down			1	μA
I_{ADCIN}	Analog input leakage					1	μA
C_{ai}	Analog input capacitance	Typical capacitive load on analog input pin	Non-sampling		10		pF
			Sampling		30		
E_{DNL}	Differential nonlinearity error	Difference between the actual step width and the ideal value				±2	LSB
E_{INL}	Integral nonlinearity error	Maximum deviation from the best straight line through the ADC transfer characteristics, excluding the quantization error				±2	LSB
$t_{d(PU)}$	Delay time, power-up to ADC valid	Time to stabilize analog stage after power-up				10	μs
Z_{AI}	Analog input source impedance	Analog input source impedance needed for conversions to remain within specifications at min $t_{w(SH)}$				10	Ω

† Absolute resolution = 3.22 mV. At V_{REFHI} = 3.3 V and V_{REFLO} = 0 V, this is one LSB. As V_{REFHI} decreases, V_{REFLO} increases, or both, the LSB size decreases. Therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

internal ADC module timings† (see Figure 30)

		MIN	MAX	UNIT
$t_{c(AD)}$	Cycle time, ADC prescaled clock		33.3	ns
$t_{w(SHC)}$	Pulse duration, total sample/hold and conversion time‡		500	ns
$t_{w(SH)}$	Pulse duration, sample and hold time	$2t_{c(AD)}$§	$32t_{c(AD)}$	ns
$t_{w(C)}$	Pulse duration, total conversion time	$10t_{c(AD)}$		ns
$t_{d(SOC-SH)}$	Delay time, start of conversion to beginning of sample and hold	$3t_{c(CO)}$		ns
$t_{d(EOC)}$	Delay time, end of conversion to data loaded into result register	$2t_{c(CO)}$		ns
$t_{d(ADCINT)}$	Delay time, ADC flag to ADC interrupt	$2t_{c(CO)}$		ns

† The ADC timing diagram represents a typical conversion sequence. Refer to the ADC chapter in the *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357A) for more details.
‡ The total sample/hold and conversion time is determined by the summation of $t_{d(SOC-SH)}$, $t_{w(SH)}$, $t_{w(C)}$, and $t_{d(EOC)}$.
§ Can be varied by ACQ Prescalar bits in the ADCCTRL1 register

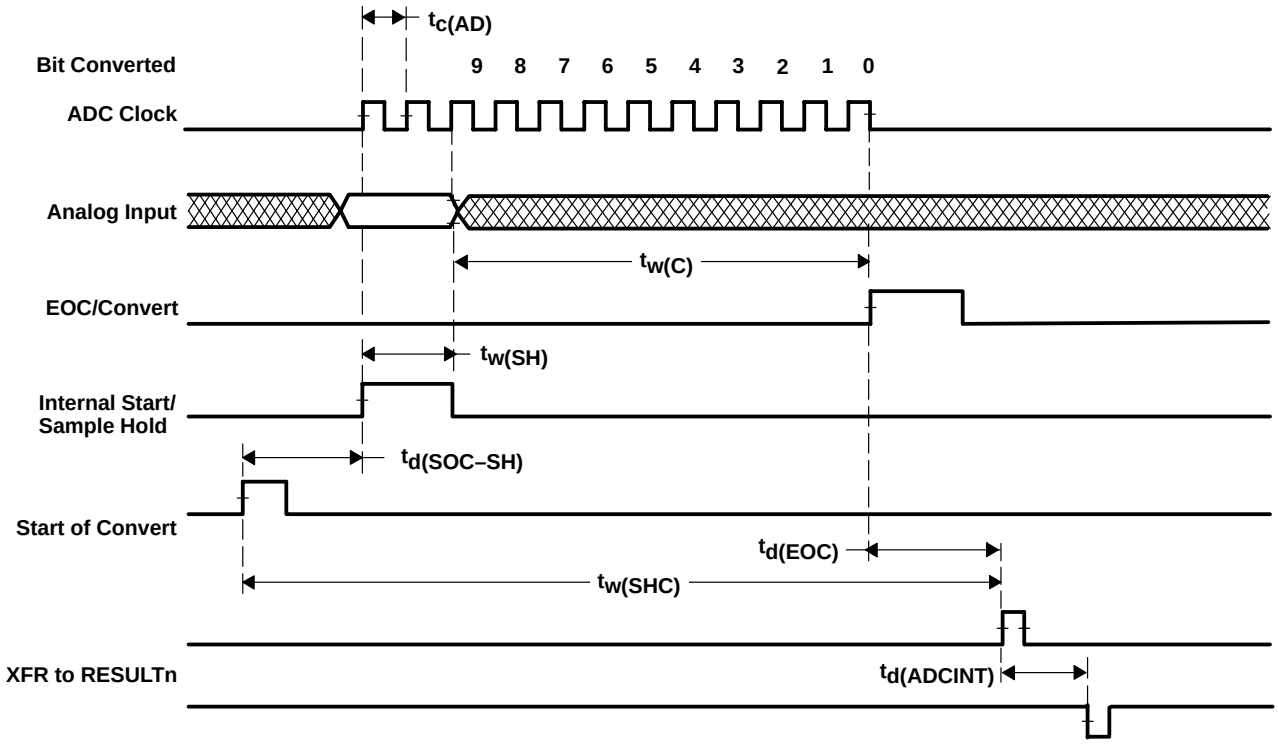


Figure 30. Analog-to-Digital Internal Module Timing

Flash parameters @40 MHz CLOCKOUT

PARAMETER		MIN	TYP	MAX	UNIT
Clear/Programming time†	Time/Word (16-bit)		30		µs
	Time/4K Sector		130		ms
Erase time†	Time/4K Sector		350		ms
I_{CCP} (V_{CCP} pin current)	Indicates the typical/maximum current consumption during the Clear-Erase-Program (C-E-P) cycle		5	15	mA

† The indicated time does not include the time it takes to load the C-E-P algorithm and the code (to be programmed) onto on-chip RAM. The values specified are when V_{DD} = 3.3 V and V_{CCP} = 5 V, and any deviation from these values could affect the timing parameters. Aging and process variance could also impact the timing parameters.

migrating from other 240xA devices to LF2401A

This section outlines some of the issues to be considered while migrating a design from the 240xA family to the LF2401A. The LF2401A shares the same CPU core (and hence, the same instruction set) as the 240xA. Furthermore, the peripherals implemented on the LF2401A are a subset of those found in the 240xA family. However, some features of a particular peripheral may not be present on the 2401A. This must be taken into consideration while porting code to the LF2401A. Other issues to be considered for migration are as follows.

PLL

The PLL used in the LF2401A is different than the one used in the 240xA family. The LF2401A PLL does not need the external loop-filter components.

on-chip bootloader

Boot ROM is a 256-word ROM mapped in program space 0000h–00FFh. This ROM will be enabled if the BOOT_EN mode is enabled during reset. Boot-enable function is implemented using combinational logic of the TDI, $\overline{\text{TRST}}$, and $\overline{\text{RS}}$ pins as described below. The on-chip bootloader is invoked when:

$\overline{\text{TRST}}$ = 0

$\overline{\text{RS}}$ = 0

TDI = 0

(In addition to the three pins mentioned above, the application must ensure that $\overline{\text{PDPINTA}}$ stays high during the execution of the boot ROM code.) Since it has an internal pulldown, the $\overline{\text{TRST}}$ pin will be low, provided the JTAG connector is not connected. Therefore, the BOOT_EN bit (bit 3 of the SCSR2 register) will be set to 0 if TDI is low upon reset. If on-chip bootloader is desired while debugging with the JTAG connector connected ($\overline{\text{TRST}}$ = 1), it can be achieved by writing a “0” into bit 3 of the SCSR2 register.

GPIO

The multiplexing scheme of the GPIO pins with other functional pins is different in the LF2401A. Because of this, the bit assignments for the MCRA, PADATDIR, and PBDATDIR registers of the LF2401A is *not* compatible with the bit assignments of the 240xA family.

EV

The Event Manager of the LF2401A has reduced functionality when compared to that of the 240xA family. Following are the important differences:

- There is no QEP unit.
- There is only one “Capture” input (CAP1).
- Although Timer 1 is present, there is no compare output pin (T1CMP/T1PWM).
- There is no provision to feed an external clock to the timers.
- There is no external direction control pin for the timers.

Due to these differences, some of the bits in the EV registers are not applicable in the LF2401A and are shaded gray. Refer to Table 15, LF2401A DSP Peripheral Register Description, for more details.

ADC

The LF2401A ADC has only five input channels as compared to eight or sixteen channels in the 240xA family. Therefore, the 4-bit fields in the CHSELSEQn registers should be programmed with values from 0–4 only.

The LF2401A ADC does not have dedicated V_{REFHI} and V_{REFLO} pins. Instead, the V_{CCA} and V_{SSA} pins provide the necessary reference.

pins

The following pins, which are available in other 240xA devices, have been internally tied as indicated:

CAP2, CAP3 – low

TDIRA – low

TCLKINA – low

$\overline{\text{BIO}}$ – high

peripheral register description

Table 15 is a collection of all the programmable registers of the LF2401A and is provided as a quick reference.

Table 15. LF2401A DSP Peripheral Register Description

ADDR	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	REG
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
	DATA MEMORY SPACE								
	CPU STATUS REGISTERS								
	ARP			OV	OVM	1	INTM	DP(8)	ST0
	DP(7)	DP(6)	DP(5)	DP(4)	DP(3)	DP(2)	DP(1)	DP(0)	
	ARB			CNF	TC	SXM	C	1	ST1
	1	1	1	XF	1	1	PM		
	GLOBAL MEMORY AND CPU INTERRUPT REGISTERS								
00004h	—	—	—	—	—	—	—	—	IMR
	—	—	INT6 MASK	INT5 MASK	INT4 MASK	INT3 MASK	INT2 MASK	INT1 MASK	
00005h	Reserved								GREG
00006h	—	—	—	—	—	—	—	—	IFR
	—	—	INT6 FLAG	INT5 FLAG	INT4 FLAG	INT3 FLAG	INT2 FLAG	INT1 FLAG	
	SYSTEM REGISTERS								
07010h	IRQ0.15	IRQ0.14	IRQ0.13	IRQ0.12	IRQ0.11	IRQ0.10	IRQ0.9	IRQ0.8	PIRQR0
	IRQ0.7	IRQ0.6	IRQ0.5	IRQ0.4	IRQ0.3	IRQ0.2	IRQ0.1	IRQ0.0	
07011h	IRQ1.15	IRQ1.14	IRQ1.13	IRQ1.12	IRQ1.11	IRQ1.10	IRQ1.9	IRQ1.8	PIRQR1
	IRQ1.7	IRQ1.6	IRQ1.5	IRQ1.4	IRQ1.3	IRQ1.2	IRQ1.1	IRQ1.0	
07012h	IRQ2.15	IRQ2.14	IRQ2.13	IRQ2.12	IRQ2.11	IRQ2.10	IRQ2.9	IRQ2.8	PIRQR2
	IRQ2.7	IRQ2.6	IRQ2.5	IRQ2.4	IRQ2.3	IRQ2.2	IRQ2.1	IRQ2.0	
07013h	Illegal								
07014h	IAK0.15	IAK0.14	IAK0.13	IAK0.12	IAK0.11	IAK0.10	IAK0.9	IAK0.8	PIACKR0
	IAK0.7	IAK0.6	IAK0.5	IAK0.4	IAK0.3	IAK0.2	IAK0.1	IAK0.0	
07015h	IAK1.15	IAK1.14	IAK1.13	IAK1.12	IAK1.11	IAK1.10	IAK1.9	IAK1.8	PIACKR1
	IAK1.7	IAK1.6	IAK1.5	IAK1.4	IAK1.3	IAK1.2	IAK1.1	IAK1.0	
07016h	IAK2.15	IAK2.14	IAK2.13	IAK2.12	IAK2.11	IAK2.10	IAK2.9	IAK2.8	PIACKR2
	IAK2.7	IAK2.6	IAK2.5	IAK2.4	IAK2.3	IAK2.2	IAK2.1	IAK2.0	
07017h	Illegal								
07018h	—	CLKSRC	LPM1	LPM0	CLK PS2	CLK PS1	CLK PS0	—	SCSR1
	ADC CLKEN	SCI CLKEN	SPI CLKEN	CAN CLKEN	EVB CLKEN	EVA CLKEN	—	ILLADR	
07019h	—	—	—	—	—	—	—	—	SCSR2
	—	I/P QUALIFIER CLOCKS	WD OVERRIDE	XMIF HI Z	$\overline{\text{BOOT\_EN}}$	MP/$\overline{\text{MC}}$	DON	PON	
0701Ah to 0701Bh	Illegal								
0701Ch	DIN15	DIN14	DIN13	DIN12	DIN11	DIN10	DIN9	DIN8	DINR
	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0	
0701Dh	Illegal								
0701Eh	V15	V14	V13	V12	V11	V10	V9	V8	PIVR
	V7	V6	V5	V4	V3	V2	V1	V0	
0701Fh	Illegal								

These bits are not applicable in the LF2401A since either (i) the peripheral functionality is absent or (ii) the corresponding pins have not been bonded out of the device.

peripheral register description (continued)

Table 15. LF2401A DSP Peripheral Register Description (Continued)

ADDR	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	REG
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
	WD CONTROL REGISTERS								
07020h to 07022h	Illegal								
07023h	D7	D6	D5	D4	D3	D2	D1	D0	WDCNTR
07024h	Illegal								
07025h	D7	D6	D5	D4	D3	D2	D1	D0	WDKEY
07026h to 07028h	Illegal								
07029h	WDFLAG	WDDIS	WDCHK2	WDCHK1	WDCHK0	WDPS2	WDPS1	WDPS0	WDCR
0702Ah to 0703Fh	Illegal								
07040h to 0704Fh	Reserved								
	SERIAL COMMUNICATIONS INTERFACE (SCI) CONFIGURATION CONTROL REGISTERS								
07050h	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	LOOP BACK ENA	ADDR/IDLE MODE	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
07051h	—	RX ERR INT ENA	SW RESET	—	TXWAKE	SLEEP	TXENA	RXENA	SCICTL1
07052h	BAUD15 (MSB)	BAUD14	BAUD13	BAUD12	BAUD11	BAUD10	BAUD9	BAUD8	SCIHBAUD
07053h	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	SCILBAUD
07054h	TXRDY	TX EMPTY	—	—	—	—	RX/BK INT ENA	TX INT ENA	SCICTL2
07055h	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	—	SCIRXST
07056h	ERXDT7	ERXDT6	ERXDT5	ERXDT4	ERXDT3	ERXDT2	ERXDT1	ERXDT0	SCIRXEMU
07057h	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	SCIRXBUF
07058h	Illegal								
07059h	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	SCITXBUF
0705Ah to 0705Eh	Illegal								
0705Fh	—	SCITX PRIORITY	SCIRX PRIORITY	SCI SOFT	SCI FREE	—	—	—	SCIPRI
07060h to 0706Fh	Illegal								

These bits are not applicable in the LF2401A since either (i) the peripheral functionality is absent or (ii) the corresponding pins have not been bonded out of the device.

peripheral register description (continued)

Table 15. LF2401A DSP Peripheral Register Description (Continued)

ADDR	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	REG
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
	EXTERNAL INTERRUPT CONTROL REGISTERS								
07070h	XINT1 FLAG	—	—	—	—	—	—	—	XINT1CR
	—	—	—	—	—	XINT1 POLARITY	XINT1 PRIORITY	XINT1 ENA	
07071h	XINT2 FLAG	—	—	—	—	—	—	—	XINT2CR
	—	—	—	—	—	XINT2 POLARITY	XINT2 PRIORITY	XINT2 ENA	
07072h to 0708Fh	Illegal								
	DIGITAL I/O CONTROL REGISTERS								
07090h	MCRA.15	MCRA.14	MCRA.13	MCRA.12	MCRA.11	MCRA.10	MCRA.9	MCRA.8	MCRA
	MCRA.7	MCRA.6	MCRA.5	MCRA.4	MCRA.3	MCRA.2	MCRA.1	MCRA.0	
07091h	Illegal								
07092h	MCRB.15	MCRB.14	MCRB.13	MCRB.12	MCRB.11	MCRB.10	MCRB.9	MCRB.8	MCRB
	MCRB.7	MCRB.6	MCRB.5	MCRB.4	MCRB.3	MCRB.2	MCRB.1	MCRB.0	
07093h	Illegal								
07094h	MCRC.15	MCRC.14	MCRC.13	MCRC.12	MCRC.11	MCRC.10	MCRC.9	MCRC.8	MCRC
	MCRC.7	MCRC.6	MCRC.5	MCRC.4	MCRC.3	MCRC.2	MCRC.1	MCRC.0	
07095h	E7DIR	E6DIR	E5DIR	E4DIR	E3DIR	E2DIR	E1DIR	E0DIR	PEDATDIR
	IOPE7	IOPE6	IOPE5	IOPE4	IOPE3	IOPE2	IOPE1	IOPE0	
07096h	—	F6DIR	F5DIR	F4DIR	F3DIR	F2DIR	F1DIR	F0DIR	PFDATDIR
	—	IOPF6	IOPF5	IOPF4	IOPF3	IOPF2	IOPF1	IOPF0	
07097h	Illegal								
07098h	A7DIR	A6DIR	A5DIR	A4DIR	A3DIR	A2DIR	A1DIR	A0DIR	PADATDIR
	IOPA7	IOPA6	IOPA5	IOPA4	IOPA3	IOPA2	IOPA1	IOPA0	
07099h	Illegal								
0709Ah	B7DIR	B6DIR	B5DIR	B4DIR	B3DIR	B2DIR	B1DIR	B0DIR	PBDATDIR
	IOPB7	IOPB6	IOPB5	IOPB4	IOPB3	IOPB2	IOPB1	IOPB0	
0709Bh	Illegal								
0709Ch	C7DIR	C6DIR	C5DIR	C4DIR	C3DIR	C2DIR	C1DIR	C0DIR	PCDATDIR
	IOPC7	IOPC6	IOPC5	IOPC4	IOPC3	IOPC2	IOPC1	IOPC0	
0709Dh	Illegal								
0709Eh	D7DIR	D6DIR	D5DIR	D4DIR	D3DIR	D2DIR	D1DIR	D0DIR	PDDATDIR
	IOPD7	IOPD6	IOPD5	IOPD4	IOPD3	IOPD2	IOPD1	IOPD0	
0709Fh	Illegal								

These bits are not applicable in the LF2401A since either (i) the peripheral functionality is absent or (ii) the corresponding pins have not been bonded out of the device.

PRODUCT PREVIEW

peripheral register description (continued)

Table 15. LF2401A DSP Peripheral Register Description (Continued)

ADDR	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	REG
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
	ANALOG-TO-DIGITAL CONVERTER (ADC) REGISTERS								
070A0h	—	ADC S/W RESET	SOFT	FREE	ACQ PRESCALE3	ACQ PRESCALE2	ACQ PRESCALE1	ACQ PRESCALE0	ADCCTRL1
	CONV PRE-SCALE (CPS)	CONTIN-UOUS RUN	INT PRIORITY	SEQ1/2 CASCADE	CALIB EN	BRIDGE EN	HI / LO	FSTEST EN	
070A1h	EVB SOC EN SEQ1	Reset SEQ1 Start CALIB	SOC SEQ1	SEQ1 BUSY	INT ENA SEQ1 Mode1	INT ENA SEQ1 Mode0	INT FLAG SEQ1	EVA SOC EN SEQ1	ADCCTRL2
	EXT SOC EN SEQ1	Reset SEQ2	SOC SEQ2	SEQ2 BUSY	INT ENA SEQ2 Mode1	INT ENA SEQ2 Mode0	INT FLAG SEQ2	EVB SOC EN SEQ2	
070A2h	—	—	—	—	—	—	—	—	MAXCONV
	—	MAXCONV2 2	MAXCONV2 1	MAXCONV2 0	MAXCONV1 3	MAXCONV1 2	MAXCONV1 1	MAXCONV1 0	
070A3h	CONV 3	CONV 3	CONV 3	CONV 3	CONV 2	CONV 2	CONV 2	CONV 2	CHSELSEQ1
	CONV 1	CONV 1	CONV 1	CONV 1	CONV 0	CONV 0	CONV 0	CONV 0	
070A4h	CONV 7	CONV 7	CONV 7	CONV 7	CONV 6	CONV 6	CONV 6	CONV 6	CHSELSEQ2
	CONV 5	CONV 5	CONV 5	CONV 5	CONV 4	CONV 4	CONV 4	CONV 4	
070A5h	CONV 11	CONV 11	CONV 11	CONV 11	CONV 10	CONV 10	CONV 10	CONV 10	CHSELSEQ3
	CONV 9	CONV 9	CONV 9	CONV 9	CONV 8	CONV 8	CONV 8	CONV 8	
070A6h	CONV 15	CONV 15	CONV 15	CONV 15	CONV 14	CONV 14	CONV 14	CONV 14	CHSELSEQ4
	CONV 13	CONV 13	CONV 13	CONV 13	CONV 12	CONV 12	CONV 12	CONV 12	
070A7h	—	—	—	—	SEQ CNTR3	SEQ CNTR2	SEQ CNTR1	SEQ CNTR0	AUTO_SEQ_SR
	SEQ2 STATE 3	SEQ2 STATE 2	SEQ2 STATE 1	SEQ2 STATE 0	SEQ1 STATE 3	SEQ1 STATE 2	SEQ1 STATE 1	SEQ1 STATE 0	
070A8h	D9	D8	D7	D6	D5	D4	D3	D2	RESULT0
	D1	D0	0	0	0	0	0	0	
070A9h	D9	D8	D7	D6	D5	D4	D3	D2	RESULT1
	D1	D0	0	0	0	0	0	0	
070AAh	D9	D8	D7	D6	D5	D4	D3	D2	RESULT2
	D1	D0	0	0	0	0	0	0	
070ABh	D9	D8	D7	D6	D5	D4	D3	D2	RESULT3
	D1	D0	0	0	0	0	0	0	
070ACh	D9	D8	D7	D6	D5	D4	D3	D2	RESULT4
	D1	D0	0	0	0	0	0	0	
070ADh	D9	D8	D7	D6	D5	D4	D3	D2	RESULT5
	D1	D0	0	0	0	0	0	0	
070AEh	D9	D8	D7	D6	D5	D4	D3	D2	RESULT6
	D1	D0	0	0	0	0	00	0	
070AFh	D9	D8	D7	D6	D5	D4	D3	D2	RESULT7
	D1	D0	0	0	0	0	0	0	

These bits are not applicable in the LF2401A since either (i) the peripheral functionality is absent or (ii) the corresponding pins have not been bonded out of the device.

peripheral register description (continued)

Table 15. LF2401A DSP Peripheral Register Description (Continued)

ADDR	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	REG
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
	ANALOG-TO-DIGITAL CONVERTER (ADC) REGISTERS (CONTINUED)								
070B0h	D9	D8	D7	D6	D5	D4	D3	D2	RESULT8
	D1	D0	0	0	0	0	0	0	
070B1h	D9	D8	D7	D6	D5	D4	D3	D2	RESULT9
	D1	D0	0	0	0	0	0	0	
070B2h	D9	D8	D7	D6	D5	D4	D3	D2	RESULT10
	D1	D0	0	0	0	0	0	0	
070B3h	D9	D8	D7	D6	D5	D4	D3	D2	RESULT11
	D1	D0	0	0	0	0	0	0	
070B4h	D9	D8	D7	D6	D5	D4	D3	D2	RESULT12
	D1	D0	0	0	0	0	0	0	
070B5h	D9	D8	D7	D6	D5	D4	D3	D2	RESULT13
	D1	D0	0	0	0	0	0	0	
070B6h	D9	D8	D7	D6	D5	D4	D3	D2	RESULT14
	D1	D0	0	0	0	0	0	0	
070B7h	D9	D8	D7	D6	D5	D4	D3	D2	RESULT15
	D1	D0	0	0	0	0	0	0	
070B8h	D9	D8	D7	D6	D5	D4	D3	D2	CALIBRATION
	D1	D0	0	0	0	0	0	0	
070B9h to 070FFh	Illegal								
07100h to 073FFh	Reserved								
	GENERAL-PURPOSE (GP) TIMER CONFIGURATION CONTROL REGISTERS – EVA								
07400h	—	T2STAT	T1STAT	—		T2TOADC		T1TOADC(1)	GPTCONA
	T1TOADC(0)	TCOMPOE	—		T2PIN		T1PIN		
07401h	D15	D14	D13	D12	D11	D10	D9	D8	T1CNT
	D7	D6	D5	D4	D3	D2	D1	D0	
07402h	D15	D14	D13	D12	D11	D10	D9	D8	T1CMPR
	D7	D6	D5	D4	D3	D2	D1	D0	
07403h	D15	D14	D13	D12	D11	D10	D9	D8	T1PR
	D7	D6	D5	D4	D3	D2	D1	D0	
07404h	FREE	SOFT	—	TMODE1	TMODE0	TPS2	TPS1	TPS0	T1CON
	—	TENABLE	TCLKS1	TCLKS0	TCLD1	TCLD0	TECMPR	—	

These bits are not applicable in the LF2401A since either (i) the peripheral functionality is absent or (ii) the corresponding pins have not been bonded out of the device.

peripheral register description (continued)

Table 15. LF2401A DSP Peripheral Register Description (Continued)

ADDR	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	REG
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
	GENERAL-PURPOSE (GP) TIMER CONFIGURATION CONTROL REGISTERS – EVA (CONTINUED)								
07405h	D15	D14	D13	D12	D11	D10	D9	D8	T2CNT
	D7	D6	D5	D4	D3	D2	D1	D0	
07406h	D15	D14	D13	D12	D11	D10	D9	D8	T2CMPR
	D7	D6	D5	D4	D3	D2	D1	D0	
07407h	D15	D14	D13	D12	D11	D10	D9	D8	T2PR
	D7	D6	D5	D4	D3	D2	D1	D0	
07408h	FREE	SOFT	—	TMODE1	TMODE0	TPS2	TPS1	TPS0	T2CON
	T2SWT1	TENABLE	TCLKS1	TCLKS0	TCLD1	TCLD0	TECMPR	SELT1PR	
07409h to 07410h	Illegal								
	FULL AND SIMPLE COMPARE UNIT REGISTERS – EVA								
07411h	CENABLE	CLD1	CLD0	SVENABLE	ACTRLD1	ACTRLD0	FCOMPOE	$\overline{\text{PDPINTA}}$ STATUS	COMCONA
	—	—	—	—	—	—	—	—	
07412h	Illegal								
07413h	SVRDIR	D2	D1	D0	CMP6ACT1	CMP6ACT0	CMP5ACT1	CMP5ACT0	ACTRA
	CMP4ACT1	CMP4ACT0	CMP3ACT1	CMP3ACT0	CMP2ACT1	CMP2ACT0	CMP1ACT1	CMP1ACT0	
07414h	Illegal								
07415h	—	—	—	—	DBT3	DBT2	DBT1	DBT0	DBTCONA
	EDBT3	EDBT2	EDBT1	DBTPS2	DBTPS1	DBTPS0	—	—	
07416h	Illegal								
07417h	D15	D14	D13	D12	D11	D10	D9	D8	CMPR1
	D7	D6	D5	D4	D3	D2	D1	D0	
07418h	D15	D14	D13	D12	D11	D10	D9	D8	CMPR2
	D7	D6	D5	D4	D3	D2	D1	D0	
07419h	D15	D14	D13	D12	D11	D10	D9	D8	CMPR3
	D7	D6	D5	D4	D3	D2	D1	D0	
0741Ah to 0741Fh	Illegal								

These bits are not applicable in the LF2401A since either (i) the peripheral functionality is absent or (ii) the corresponding pins have not been bonded out of the device.

peripheral register description (continued)

Table 15. LF2401A DSP Peripheral Register Description (Continued)

ADDR	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	REG
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
	CAPTURE UNIT REGISTERS – EVA								
07420h	CAPRES	CAPQEPN		CAP3EN	—	CAP3TSEL	CAP12TSEL	CAP3TOADC	CAPCONA
	CAP1EDGE		CAP2EDGE		CAP3EDGE		—		
07421h	Illegal								
07422h	—		CAP3FIFO		CAP2FIFO		CAP1FIFO		CAPFIFOA
	—	—	—	—	—	—	—	—	
07423h	D15	D14	D13	D12	D11	D10	D9	D8	CAP1FIFO
	D7	D6	D5	D4	D3	D2	D1	D0	
07424h	D15	D14	D13	D12	D11	D10	D9	D8	CAP2FIFO
	D7	D6	D5	D4	D3	D2	D1	D0	
07425h	D15	D14	D13	D12	D11	D10	D9	D8	CAP3FIFO
	D7	D6	D5	D4	D3	D2	D1	D0	
07426h	Illegal								
07427h	D15	D14	D13	D12	D11	D10	D9	D8	CAP1FBOT
	D7	D6	D5	D4	D3	D2	D1	D0	
07428h	D15	D14	D13	D12	D11	D10	D9	D8	CAP2FBOT
	D7	D6	D5	D4	D3	D2	D1	D0	
07429h	D15	D14	D13	D12	D11	D10	D9	D8	CAP3FBOT
	D7	D6	D5	D4	D3	D2	D1	D0	
0742Ah to 0742Bh	Illegal								
	EVENT MANAGER (EVA) INTERRUPT CONTROL REGISTERS								
0742Ch	—	—	—	—	—	T1OFINT ENA	T1UFINT ENA	T1CINT ENA	EVAIMRA
	T1PINT ENA	—	—	—	CMP3INT ENA	CMP2INT ENA	CMP1INT ENA	PDPINTA ENA	
0742Dh	—	—	—	—	—	—	—	—	EVAIMRB
	—	—	—	—	T2OFINT ENA	T2UFINT ENA	T2CINT ENA	T2PINT ENA	
0742Eh	—	—	—	—	—	—	—	—	EVAIMRC
	—	—	—	—	—	CAP3INT ENA	CAP2INT ENA	CAP1INT ENA	

These bits are not applicable in the LF2401A since either (i) the peripheral functionality is absent or (ii) the corresponding pins have not been bonded out of the device.

peripheral register description (continued)

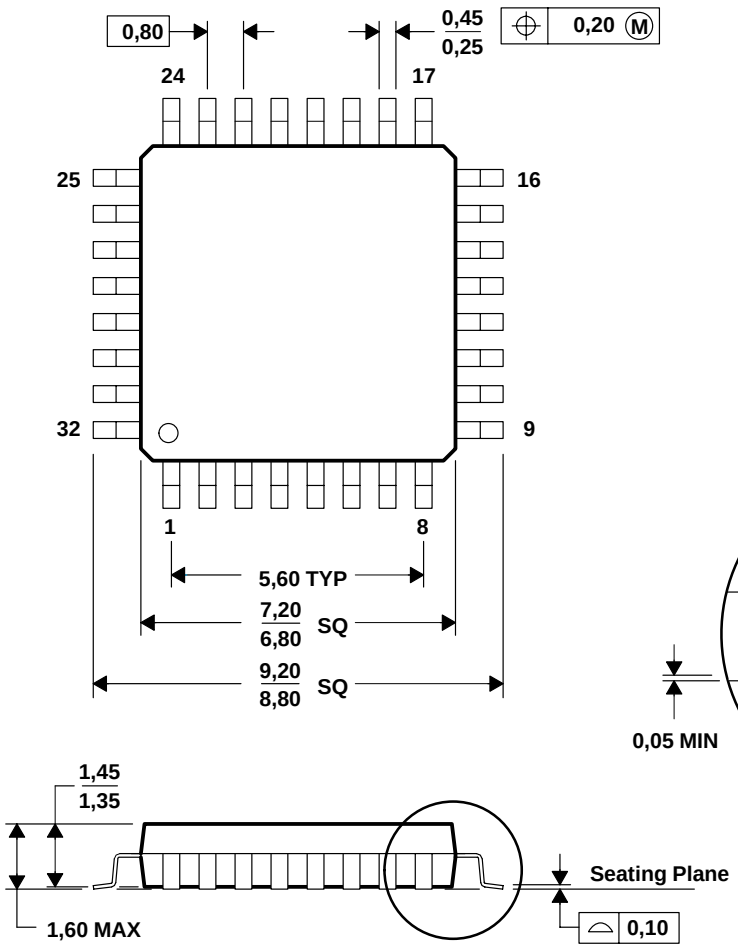
Table 15. LF2401A DSP Peripheral Register Description (Continued)

ADDR	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	REG
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
	EVENT MANAGER (EVA) INTERRUPT CONTROL REGISTERS (CONTINUED)								
0742Fh	—	—	—	—	—	T1OFINT FLAG	T1UFINT FLAG	T1CINT FLAG	EVAIFRA
	T1PINT FLAG	—	—	—	CMP3INT FLAG	CMP2INT FLAG	CMP1INT FLAG	PDPINTA FLAG	
07430h	—	—	—	—	—	—	—	—	EVAIFRB
	—	—	—	—	T2OFINT FLAG	T2UFINT FLAG	T2CINT FLAG	T2PINT FLAG	
07431h	—	—	—	—	—	—	—	—	EVAIFRC
	—	—	—	—	—	CAP3INT FLAG	CAP2INT FLAG	CAP1INT FLAG	
07432h to 074FFh	Illegal								
07500h to 0753Fh	Reserved								
	I/O MEMORY SPACE								
0FF0Fh	—	—	—	—	—	—	—	—	FCMR
	—	—	—	—	—	—	—	—	
	WAIT-STATE GENERATOR CONTROL REGISTER								
0FFFFh	—	—	—	—	—	BVIS.1	BVIS.0	ISWS.2	WSGR
	ISWS.1	ISWS.0	DSWS.2	DSWS.1	DSWS.0	PSWS.2	PSWS.1	PSWS.0	

These bits are not applicable in the LF2401A since either (i) the peripheral functionality is absent or (ii) the corresponding pins have not been bonded out of the device.

MECHANICAL DATA

VF (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



4040172/D 04/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PRODUCT PREVIEW

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with *statements different from or beyond the parameters* stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265