ANALOGIC TECH™

AAT3236
300mA CMOS High Performance LDO

PowerLinear™

General Description

The AAT3236 is a MicroPower™ Low Dropout Linear Regulator designed to deliver a continuous 300mA output load current and is capable of handling short duration current peaks up to 500mA. With a very small footprint SOT23-5 package it is ideally suited for portable applications where low noise, high power supply ripple rejection, extended battery life and small size are critical. The AAT3236 features fast transient response and low output self noise for powering sensitive RF circuitry. Other features include low quiescent current, typically 100µA, and low dropout voltage, typically 300mV at full output load current. The device has internal output short circuit protection and thermal shutdown to prevent damage under extreme conditions.

The AAT3236 also features a low-power shutdown mode for longer battery life. A bypass pin is provided to improve PSRR performance by connecting an external capacitor from the AAT3236's reference output to ground.

The AAT3236 is available in a space saving SOT23-5 or SC70JW-8 package in 9 factory programmed voltages of 2.5V, 2.7V, 2.8V, 2.85V, 3.0V, 3.1V, 3.3V, 3.5V, or 3.6V.

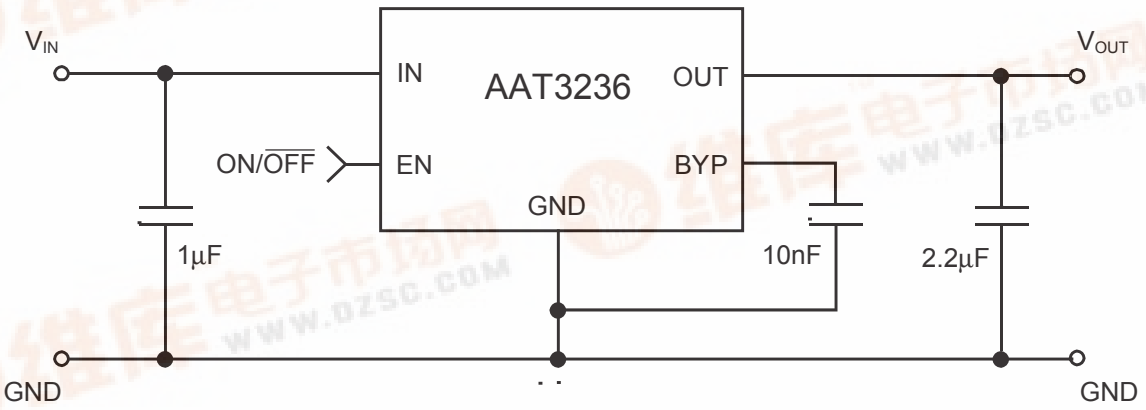
Features

- 500mA Peak Output Current
- Low Dropout - Typically 300mV at 300mA
- Guaranteed 300mA Output
- High accuracy ±1.5%
- 100µA Quiescent Current
- High Power Supply Ripple Rejection
  - 70 dB at 1kHz
  - 50 dB at 10kHz
- Very low self noise 45µVrms/rtHz
- Noise reduction bypass capacitor
- Short circuit protection
- Over-Temperature protection
- Shutdown mode for longer battery life
- Low temperature coefficient
- 9 Factory programmed output voltages
- SOT-23 5-pin or SC70JW 8-pin package

Applications

- Cellular Phones
- Notebook Computers
- Portable Communication Devices
- Personal Portable Electronics

Typical Application

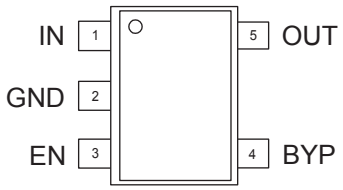


Pin Descriptions

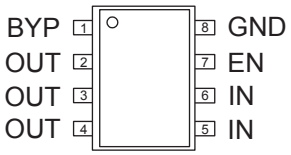
Pin #		Symbol	Function
SOT23-5	SC70JW-8		
1	5, 6	IN	Input voltage pin - should be decoupled with 1µF or greater capacitor.
2	8	GND	Ground connection pin
3	7	EN	Enable pin. When pulled low the PMOS pass transistor turns off and all internal circuitry enters low-power mode, consuming less than 1µA. This pin should not be left floating.
4	1	BYP	Bypass capacitor connection - to improve AC ripple rejection, connect a 10nF capacitor to GND. This will also provide a soft start function.
5	2, 3, 4	OUT	Output pin - should be decoupled with 2.2µF capacitor.

Pin Configuration

SOT-23-5
(Top View)



SC70JW-8
(Top View)



Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Description	Value	Units
V_{IN}	Input Voltage	6	V
$V_{ENIN(MAX)}$	Maximum EN to Input Voltage	0.3	V
I_{OUT}	DC Output Current	$P_D/(V_{IN}-V_O)$	mA
T_J	Operating Junction Temperature Range	-40 to 150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Thermal Information

Symbol	Description	Rating	Units
Θ_{JA}	Maximum Thermal Resistance[1] (SOT23-5, SC70JW-8)	190	°C/W
P_D	Maximum Power Dissipation[1] (SOT23-5, SC70JW-8)	526	mW

Note 1: Mounted on a demo board.

Recommended Operating Conditions

Symbol	Description	Rating	Units
V_{IN}	Input Voltage	(V_{OUT}+0.3) to 5.5	V
T	Ambient Temperature Range	-40 to +85	°C

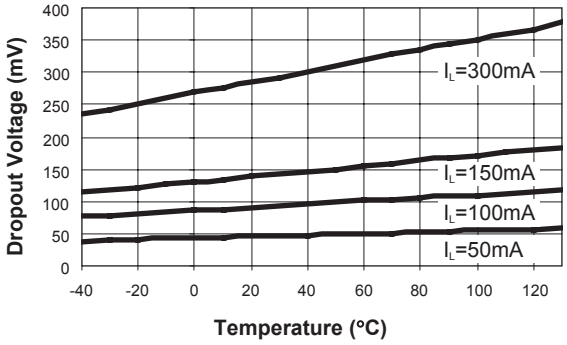
Electrical Characteristics ($V_{IN}=V_{OUT(NOM)}$+1V, I_{OUT}=1mA, C_{OUT} = 2.2µF, C_{IN} = 1µF, C_{BYP} = 10nF, T_A= -40 to 85°C unless otherwise noted. For typical values T_A=25°C)

Symbol	Description	Conditions		Min	Typ	Max	Units
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA to 300mA	T_A=25°C	-1.5		1.5	%
			T_A=-40 to 85°C	-2.5		2.5	%
I_{OUT}	Output Current	V_{OUT} > 1.2V		300			mA
V_{DO}	Dropout Voltage[2]	I_{OUT} = 300mA			300	500	mV
I_{SC}	Short Circuit Current	V_{OUT} < 0.4V			600		mA
I_Q	Ground Current	V_{IN} = 5V, no load,EN = V_{IN}			100	150	µA
I_{SD}	Shutdown Current	V_{IN} = 5V, EN = 0V				1	µA
$\Delta V_{OUT}/V_{OUT}*\Delta V_{IN}$	Line Regulation	V_{IN} = V_{OUT} + 1 to 5.5V				0.07	%/V
ΔV_{OUT}(line)	Dynamic Line Regulation	V_{IN}=V_{OUT}+1V to V_{OUT}+2V, I_{OUT}=150mA, T_R/T_F =2µs			1		mV
ΔV_{OUT}(load)	Dynamic Load Regulation	I_{OUT} = 1mA to 150mA, T_R<5µs			30		mV
$V_{EN(L)}$	Enable Threshold Low					0.6	V
$V_{EN(H)}$	Enable Threshold High			1.5			V
I_{EN}	Leakage Current Enable Pin	V_{EN}=5V				1	µA
PSRR	Power Supply Rejection Ratio	I_{OUT} = 10mA, C_{BYP} = 10nF	1 kHz		70		dB
			10kHz		50		
			1MHz		47		
T_{SD}	Over Temp Shutdown Threshold				150		°C
T_{HYS}	Over Temp Shutdown Hysteresis				10		°C
e_N	Output Noise	Noise Power BW= 300Hz to 50KHz			45		μV_{RMS}/rtHz
T_C	Output Voltage Temp. Coeff.				22		ppm/°C

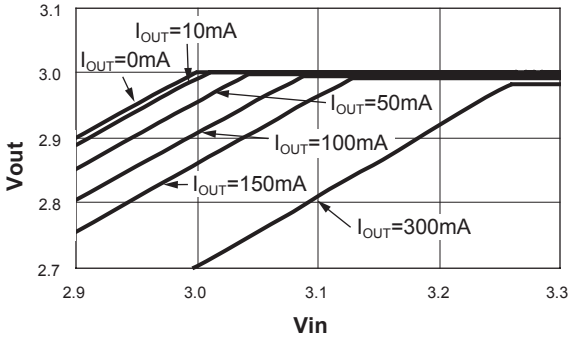
Note 2: V_{DO} is defined as V_{IN} - V_{OUT} when V_{OUT} is 98% of nominal.

Typical Characteristics

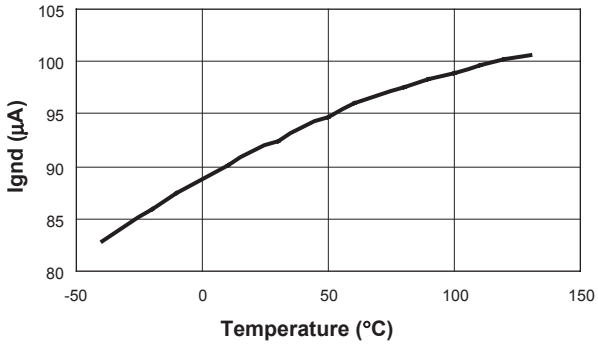
Dropout Voltage vs. Temperature



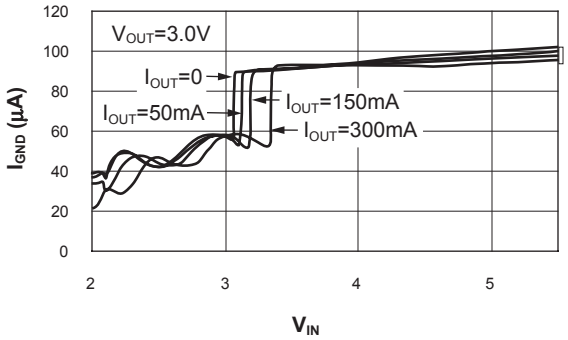
Dropout Characteristics



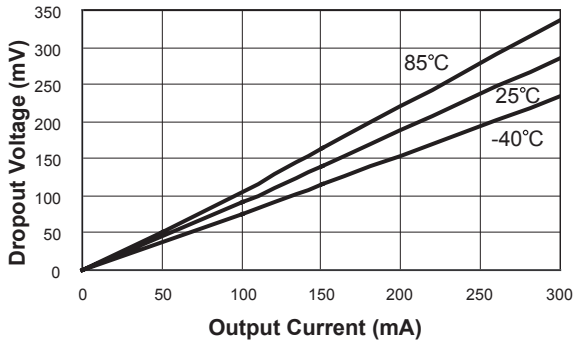
Ground Current vs. Temperature



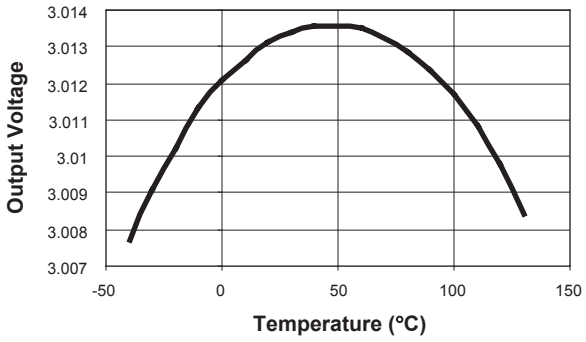
Ground Current vs. Input Voltage



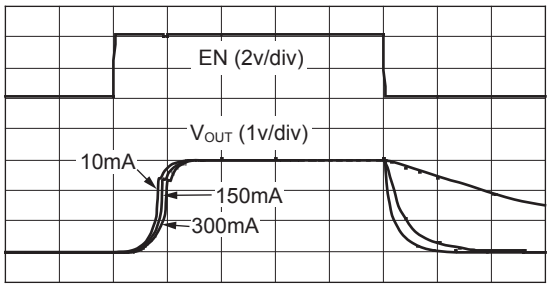
Dropout Voltage vs. I_{OUT}



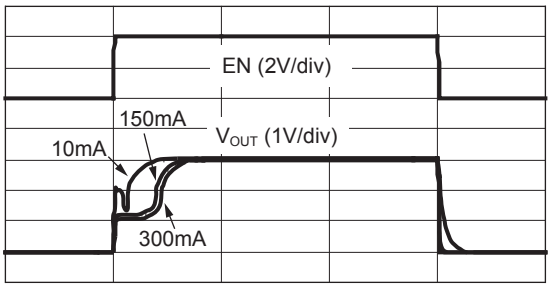
Output Voltage vs. Temperature



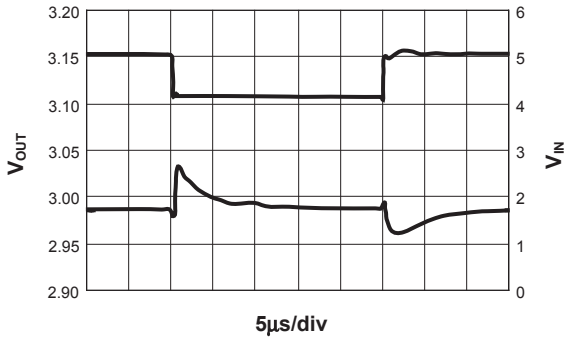
On/Off Transient Response
No C_{BYP} Capacitor



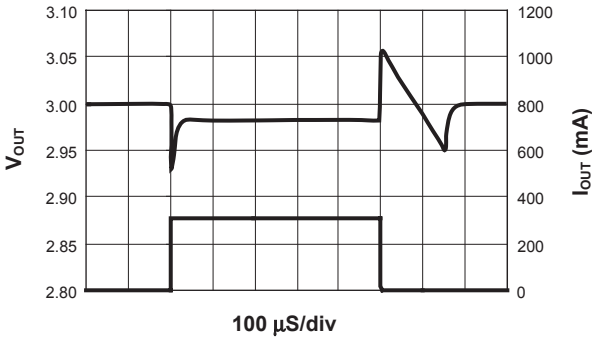
On/Off Transient Response
C_{BYP}=10nF



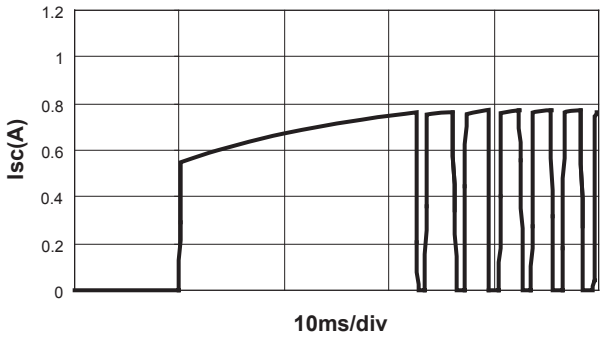
Line Transient Response



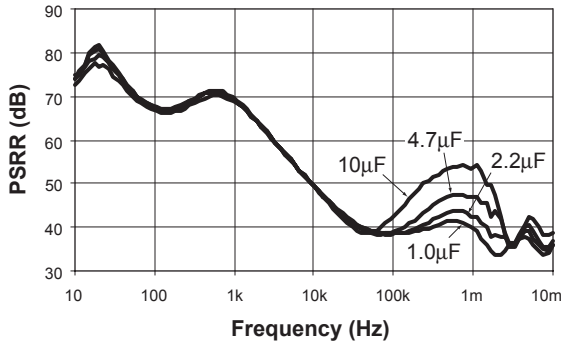
Load Transient Response



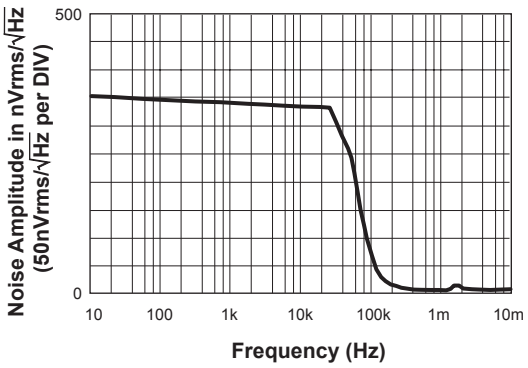
Short Circuit Current



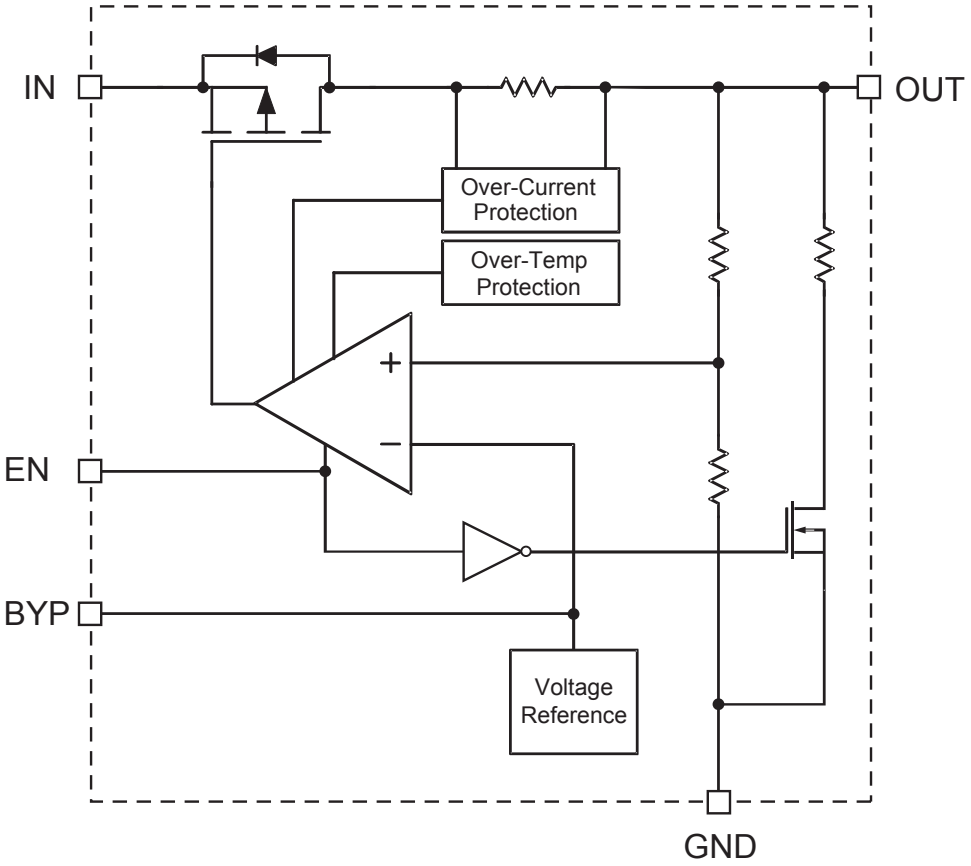
Power Supply Rejection Ratio
vs. Frequency



Output Self Noise



Functional Block Diagram



Functional Description

The AAT3236 is intended for LDO regulator applications where output current load requirements range from no load to 300mA. The AAT3236 is capable of handling peak output currents up to 500mA. Refer to the Thermal Considerations discussion in the section for details on device operation at 500mA peak loads.

The advanced circuit design of the AAT3236 provides excellent input to output isolation, which allows for good power supply ripple rejection characteristics. To optimize for very low output self noise performance, a bypass capacitor pin has been provided to decrease noise generated by the internal voltage reference.

The LDO regulator output has been specifically optimized to function with low cost, low ESR ceramic capacitors. However, the design will allow for operation over a wide range of capacitor types.

The device enable circuit is provided to shutdown the LDO regulator for power conservation in portable products. The enable circuit has an additional output capacitor discharge circuit to assure sharp application circuit turn off upon device shutdown.

This LDO regulator has complete short circuit and thermal protection. The integral combination of these two internal protection circuits give the AAT3236 a comprehensive safety system during extreme adverse operating conditions.

Applications Information

Input Capacitor

Typically a 1µF or larger capacitor is recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation. However, if the AAT3236 is physically located more than 6 centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation. C_{IN} should be located as close to the device V_{IN} pin as practically possible. C_{IN} values greater than 1µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

Ceramic, tantalum or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}. However, for 300mA LDO regulator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins V_{OUT} and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance.

The AAT3236 has been specifically designed to function with very low ESR ceramic capacitors. Although the device is intended to operate with these low ESR capacitors, it is stable over a very wide range of capacitor ESR, thus it will also work with higher ESR tantalum or aluminum electrolytic capacitors. However, for best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1µF to 10µF. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the AAT3236 should use 2.2µF or greater for C_{OUT}. If desired, C_{OUT} may be increased without limit.

In low output current applications where output load is less then 10mA, the minimum value for C_{OUT} can be as low as 0.47µF.

Bypass Capacitor and Low Noise Applications

A bypass capacitor pin is provided to enhance the very low noise characteristics of the AAT3236 LDO regulator. The bypass capacitor is not necessary for operation of the AAT3236. However, for best device performance, a small ceramic capacitor should be placed between the Bypass pin (BYP) and the device ground pin (GND). The value of C_{BYP} may range from 470pF to 10nF. For lowest noise and best possible power supply ripple rejection performance a 10nF capacitor should be used. To practically realize the highest power supply ripple rejection and lowest output noise performance, it is critical that the capacitor connection between the BYP pin and GND pin be direct and PCB traces should be as short as possible. Refer to the PCB Layout Recommendations section of this document for examples.

There is a relationship between the bypass capacitor value and the LDO regulator turn on time. In applications where fast device turn on time is desired, the value of C_{BYP} should be reduced.

In applications where low noise performance and/or ripple rejection are less of a concern, the bypass capacitor may be omitted. The fastest device turn on time will be realized when no bypass capacitor is used.

DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance. For this reason, the use of a low leakage, high quality ceramic (NPO or COG type) or film capacitor is highly recommended.

Capacitor Characteristics

Ceramic composition capacitors are highly recommended over all other types of capacitors for use with the AAT3236. Ceramic capacitors offer many advantages over their tantalum and aluminum electrolytic counterparts. A ceramic capacitor typically has very low ESR, is lower cost, has a smaller PCB footprint and is non-polarized. Line and load transient response of the LDO regulator is improved by using low ESR ceramic capacitors. Since ceramic capacitors are non-polarized, they are not prone to incorrect connection damage.

Equivalent Series Resistance (ESR): ESR is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance asso-

ciated with a capacitor, which includes lead resistance, internal connections, size and area, material composition and ambient temperature. Typically capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Ceramic Capacitor Materials: Ceramic capacitors less than 0.1µF are typically made from NPO or COG materials. NPO and COG materials are typically tight tolerance very stable over temperature. Larger capacitor values are typically composed of X7R, X5R, Z5U and Y5V dielectric materials. Large ceramic capacitors, typically greater then 2.2µF are often available in the low cost Y5V and Z5U dielectrics. These two material types are not recommended for use with LDO regulators since the capacitor tolerance can vary more than ±50% over the operating temperature range of the device. A 2.2µF Y5V capacitor could be reduced to 1µF over temperature, this could cause problems for circuit operation. X7R and X5R dielectrics are much more desirable. The temperature tolerance of X7R dielectric is better than ±15%.

Capacitor area is another contributor to ESR. Capacitors which are physically large in size will have a lower ESR when compared to a smaller sized capacitor of equivalent material and capacitance value. These larger devices can improve circuit transient response when compared to an equal value capacitor in a smaller package size.

Consult capacitor vendor data sheets carefully when selecting capacitors for LDO regulators.

Enable Function

The AAT3236 features an LDO regulator enable / disable function. This pin (EN) is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 2.0 volts. The LDO regulator will go into the disable shutdown mode when the voltage on the EN pin falls below 0.6 volts. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

When the LDO regulator is in the shutdown mode, an internal 1.5kΩ resistor is connected between V_{OUT} and GND. This is intended to discharge C_{OUT} when the LDO regulator is disabled. The internal 1.5kΩ has no adverse effect on device turn on time.

Short Circuit Protection

The AAT3236 contains an internal short circuit protection circuit that will trigger when the output load current exceeds 750mA. Under short circuit conditions the output will be limited to 750mA until the LDO regulator package power dissipation exceeds the device thermal limit or the until the short circuit condition is removed.

Thermal Protection

The AAT3236 has an internal thermal protection circuit which will turn on when the device die temperature exceeds 150°C. The internal thermal protection circuit will actively turn off the LDO regulator output pass device to prevent the possibility of over temperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 150°C trip point.

The combination and interaction between the short circuit and thermal protection systems allow the LDO regulator to withstand indefinite short circuit conditions without sustaining permanent damage.

No-Load Stability

The AAT3236 is designed to maintain output voltage regulation and stability under operational no-load conditions. This is an important characteristic for applications where the output current may drop to zero.

Reverse Output to Input Voltage Conditions and Protection

Under normal operating conditions a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage maintaining a reverse bias on the internal parasitic diode. Conditions where V_{OUT} might exceed V_{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the V_{OUT} pin possibly damaging the LDO regulator.

In applications where there is a possibility of V_{OUT} exceeding V_{IN} for brief amounts of time during normal operation, the use of a larger value C_{IN} capacitor is highly recommended. A larger value of C_{IN} with respect to C_{OUT} will effect a slower C_{IN} decay rate during shutdown, thus preventing V_{OUT} from exceeding V_{IN}. In applications where there is a greater danger of V_{OUT} exceeding V_{IN} for extended

periods of time, it is recommended to place a schottky diode across V_{IN} to V_{OUT} (connecting the cathode to V_{IN} and anode to V_{OUT}. The Schottky diode forward voltage should be less than 0.45 volts.

Thermal Considerations and High Output Current Applications

The AAT3236 is designed to deliver a continuous output load current of 300mA under normal operations and can supply up to 500mA during circuit start up conditions. This is desirable for circuit applications where there might be a brief high in rush current during a power on event.

The limiting characteristic for the maximum output load current safe operating area is essentially package power dissipation and the internal preset thermal limit of the device. In order to obtain high operating currents, careful device layout and circuit operating conditions need to be taken into account.

The following discussions will assume the LDO regulator is mounted on a printed circuit board utilizing the minimum recommended footprint as stated in the layout considerations section of the document.

At any given ambient temperature (T_A) the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = [T_{J(MAX)} - T_A] / \Theta_{JA}$$

Constants for the AAT3236 are $T_{J(MAX)}$, the maximum junction temperature for the device which is 125°C and Θ_{JA} = 190°C/W, the package thermal resistance. Typically, maximum conditions are calculated at the maximum operating temperature where T_A = 85°C, under normal ambient conditions T_A = 25°C. Given T_A = 85°, the maximum package power dissipation is 211mW. At T_A = 25°C, the maximum package power dissipation is 526mW

The maximum continuous output current for the AAT3236 is a function of the package power dissipation and the input to output voltage drop across the LDO regulator. Refer to the following simple equation:

$$I_{OUT(MAX)} < P_{D(MAX)} / (V_{IN} - V_{OUT})$$

For example, if V_{IN} = 4.2V, V_{OUT} = 3.3V and T_A = 25°, $I_{OUT(MAX)}$ < 584mA. If the output load current were to exceed 584mA or if the ambient temperature were to increase, the internal die temperature will increase. If the condition remained constant, the LDO regulator thermal protection circuit will activate.

To figure what the maximum input voltage would be for a given load current, refer to the following equation. This calculation accounts for the total power dissipation of the LDO Regulator, including that caused by ground current.

$$P_{D(MAX)} = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN} \times I_{GND})$$

This formula can be solved for V_{IN} to determine the maximum input voltage.

$$V_{IN(MAX)} = (P_{D(MAX)} + (V_{OUT} \times I_{OUT})) / (I_{OUT} + I_{GND})$$

The following is an example for an AAT3236 set for a 3.0 volt output:

From the discussion above, $P_{D(MAX)}$ was determined to equal 526mW at T_A = 25°C°.
V_{OUT} = 3.0 volts
I_{OUT} = 500mA
I_{GND} = 150uA

$V_{IN(MAX)}$=(526mW+(3.0Vx500mA))/(500mA +150µA)
$V_{IN(MAX)}$ = 4.05V

Thus, the AAT3236 can sustain a constant 3V output at a 500mA load current as long as V_{IN} is ≤ 4.05V at an ambient temperature of 25°C.

Higher input to output voltage differentials can be obtained with the AAT3236, while maintaining device functions within the thermal safe operating area. To accomplish this, the device thermal resistance must be reduced by increasing the heat sink area or by operating the LDO regulator in a duty cycled mode.

For example, an application requires V_{IN} = 4.2V while V_{OUT} = 3.0V at a 500mA load and T_A = 25°C. V_{IN} is greater then 4.05V, which is the maximum safe continuous input level for V_{OUT} = 3.0V at 500mA for T_A = 25°C. To maintain this high input voltage and output current level, the LDO regulator must be operated in a duty cycled mode. Refer to the following calculation for duty cycle operation:

$P_{D(MAX)}$ is assumed to be 526mW
I_{GND} = 150µA
I_{OUT} = 500mA

V_{IN} = 4.2 volts
V_{OUT} = 3.0 volt

%DC = 100($P_{D(MAX)}$/((V_{IN}-V_{OUT})I_{OUT}+(V_{IN}xI_{GND}))
%DC = 100(526mW/((4.2V-3.0V)500mA+(4.2Vx150µA))

%DC = 87.57%

For a 500mA output current and a 1.2 volt drop across the AAT3236 at an ambient temperature of 25°C, the maximum on time duty cycle for the device would be 87.57%.

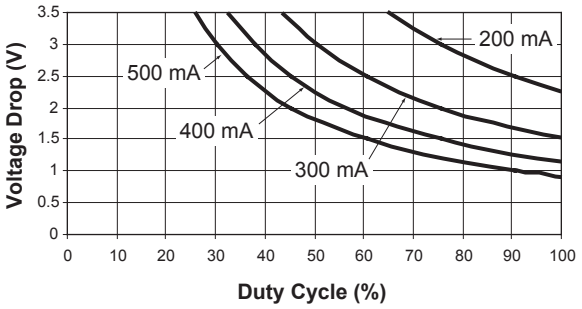
The following family of curves show the safe operating area for duty cycled operation from ambient room temperature to the maximum operating level.

High Peak Output Current Applications

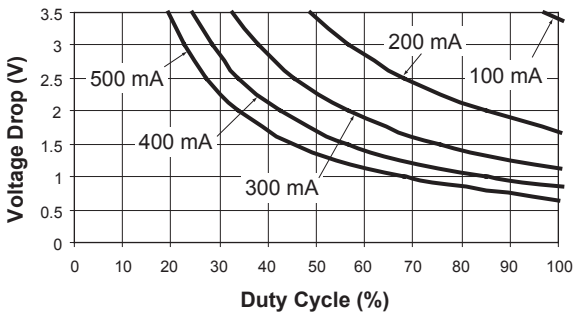
Some applications require the LDO regulator to operate at a continuous nominal level with short duration high current peaks. The duty cycles for both output current levels must be taken into account. To do so, one would first need to calculate the power dissipation at a nominal continuous level and then factor in the additional power dissipation due to the short duration high current peaks.

For example, a 3.3V system using a AAT3236IGV-3.3-T1 operates at a continuous 100mA load current level and has short 500mA current peaks. The current peak occurs for 378µs out of a 4.61ms period. It will be assumed the input voltage is 4.2V.

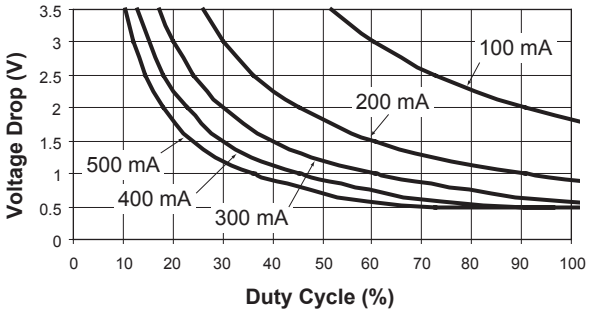
Device Duty Cycle vs. V_{DROP}
V_{OUT} = 2.5V @ 25 degrees C



Device Duty Cycle vs. V_{DROP}
V_{OUT} = 2.5V @ 50 degrees C



Device Duty Cycle vs. V_{DROP}
V_{OUT} = 2.5V @ 85 degrees C



First the current duty cycle in percent must be calculated:

% Peak Duty Cycle: X/100 = 378µs/4.61ms
% Peak Duty Cycle = 8.2%

The LDO Regulator will be under the 100mA load for 91.8% of the 4.61ms period and have 500mA peaks occurring for 8.2% of the time. Next, the continuous nominal power dissipation for the 100mA load should be determined and then multiplied by the duty cycle to conclude the actual power dissipation over time.

$P_{D(MAX)} = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN} \times I_{GND})$
$P_{D(100mA)} = (4.2V - 3.3V)100mA + (4.2V \times 150\mu A)$
$P_{D(100mA)} = 90.6mW$

$P_{D(91.8\%D/C)} = \%DC \times P_{D(100mA)}$
$P_{D(91.8\%D/C)} = 0.918 \times 90.6mW$
$P_{D(91.8\%D/C)} = 83.2mW$

The power dissipation for 100mA load occurring for 91.8% of the duty cycle will be 83.2mW. Now the power dissipation for the remaining 8.2% of the duty cycle at the 500mA load can be calculated:

$P_{D(MAX)} = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN} \times I_{GND})$
$P_{D(500mA)} = (4.2V - 3.3V)500mA + (4.2V \times 150\mu A)$
$P_{D(500mA)} = 450.6mW$

$P_{D(8.2\%D/C)} = \%DC \times P_{D(500mA)}$
$P_{D(8.2\%D/C)} = 0.082 \times 450.6mW$
$P_{D(8.2\%D/C)} = 37mW$

The power dissipation for 500mA load occurring for 8.2% of the duty cycle will be 37mW. Finally, the two power dissipation levels can summed to determine the total true power dissipation under the varied load.

$P_{D(total)} = P_{D(100mA)} + P_{D(500mA)}$
$P_{D(total)} = 83.2mW + 37mW$
$P_{D(total)} = 120.2mW$

The maximum power dissipation for the AAT3236 operating at an ambient temperature of 25°C is 526mW. The device in this example will have a total power dissipation of 120.2mW. This is well within the thermal limits for safe operation of the device.

Printed Circuit Board Layout Recommendations

In order to obtain the maximum performance from the AAT3236 LDO regulator, very careful attention must be considered in regard to the printed circuit board (PCB) layout. If grounding connections are not properly made, power supply ripple rejection, low output self noise and transient response can be compromised.

Figure 18 shows a common LDO regulator layout scheme. The LDO Regulator, external capacitors (C_{IN}, C_{OUT} and C_{BYP}) and the load circuit are all connected to a common ground plane. This type of layout will work in simple applications where good power supply ripple rejection and low self noise are not a design concern. For high performance applications, this method is not recommended.

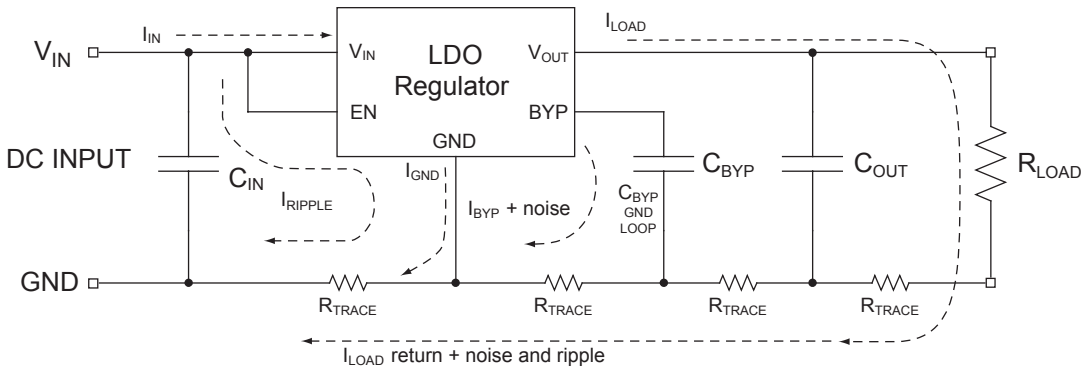


Figure 18: Common LDO Regulator Layout with C_{BYP} Ripple feedback loop

The problem with the layout in Figure 18 is the bypass capacitor and output capacitor share the same ground path to the LDO regulator ground pin along with the high current return path from the load back to the power supply. The bypass capacitor node is connected directly to the LDO regulator internal reference, making this node very sensitive to noise or ripple. The internal reference output is fed into the error amplifier, thus any noise or ripple from the bypass capacitor will be subsequently amplified by the gain of the error amplifier. This effect can increase noise seen on the LDO regulator output as well as reduce the maximum possible power supply ripple rejection. There is PCB trace impedance between the bypass capacitor connection to ground and the LDO regulator ground connection. When the high load current returns through this path, a small ripple voltage is created, feeding into the C_{BYP} loop.

Figure 19 shows the preferred method for the bypass and output capacitor connections. For low output noise and highest possible power supply ripple rejection performance, it is critical to connect the bypass and output capacitor directly to the LDO regulator ground pin. This method will eliminate any load noise or ripple current feedback through the LDO regulator.

Evaluation Board Layout

The AAT3236 evaluation layout follows the recommend printed circuit board layout procedures and can be used as an example for good application layouts.

Note: Board layout shown is not to scale.

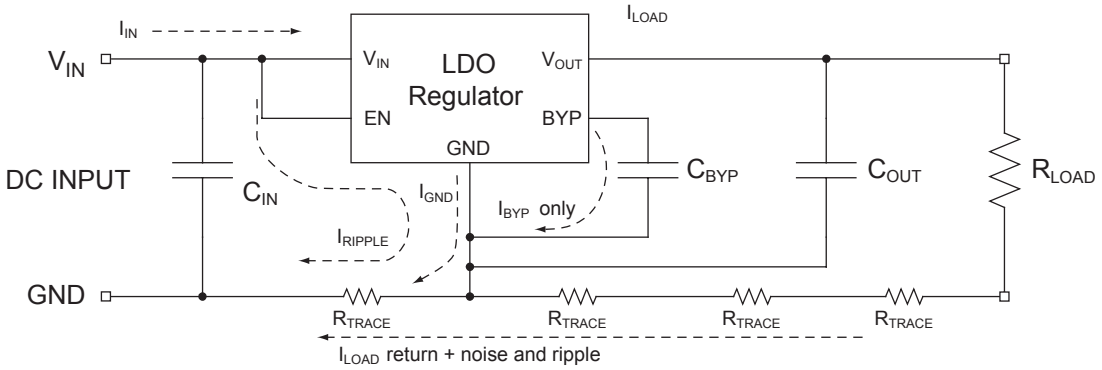


Figure 19: Recommended LDO Regulator Layout

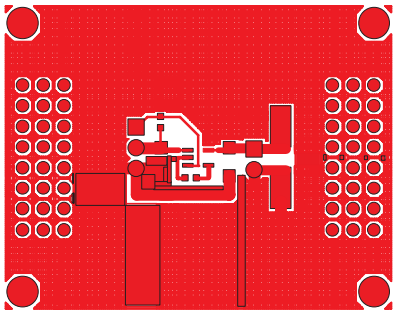


Figure 20: Evaluation board component side layout

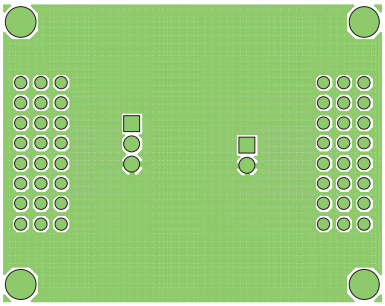


Figure 21: Evaluation board solder side layout

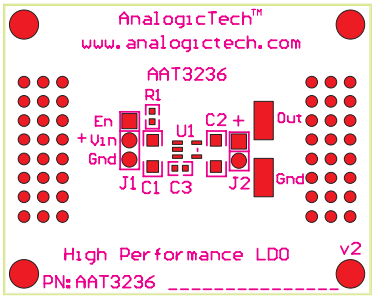


Figure 22: Evaluation board top side silk screen layout / assembly drawing

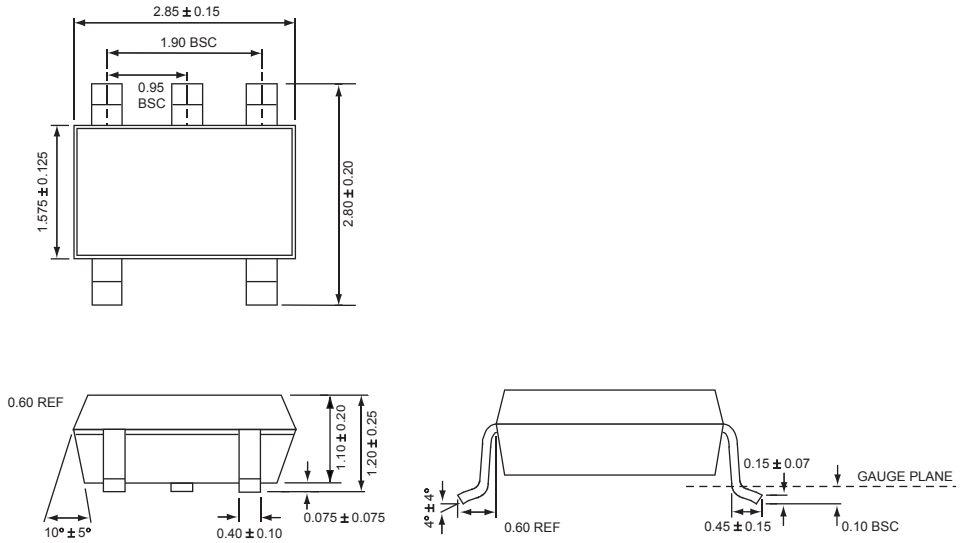
Ordering Information

Output Voltage	Package	Marking[1]	Part Number (Tape and Reel)
2.5V	SOT23-5	BRXYY	**AAT3236IGV-2.5-T1**
2.7V	SOT23-5	CPXYY	**AAT3236IGV-2.7-T1**
2.8V	SOT23-5	CQXYY	**AAT3236IGV-2.8-T1**
2.85V	SOT23-5	CRXYY	**AAT3236IGV-2.85-T1**
3.0V	SOT23-5	CSXYY	**AAT3236IGV-3.0-T1**
3.1V	SOT23-5	GAXYY	**AAT3236IGV-3.1-T1**
3.3V	SOT23-5	CDXYY	**AAT3236IGV-3.3-T1**
3.5V	SOT23-5	CUXYY	**AAT3236IGV-3.5-T1**
3.6V	SOT23-5		AAT3236IGV-3.6-T1
2.5V	SC70JW-8	BRXYY	**AAT3236IJS-2.5-T1**
2.7V	SC70JW-8	CPXYY	**AAT3236IJS-2.7-T1**
2.8V	SC70JW-8	CQXYY	**AAT3236IJS-2.8-T1**
2.85V	SC70JW-8	CRXYY	**AAT3236IJS-2.85-T1**
2.9V	SC70JW-8		AAT3236IJS-2.9-T1
3.0V	SC70JW-8	CSXYY	**AAT3236IJS-3.0-T1**
3.1V	SC70JW-8	GAXYY	AAT3236IJS-3.1-T1
3.3V	SC70JW-8	CDXYY	**AAT3236IJS-3.3-T1**
3.5V	SC70JW-8		AAT3236IJS-3.5-T1
3.6V	SC70JW-8		AAT3236IJS-3.6-T1

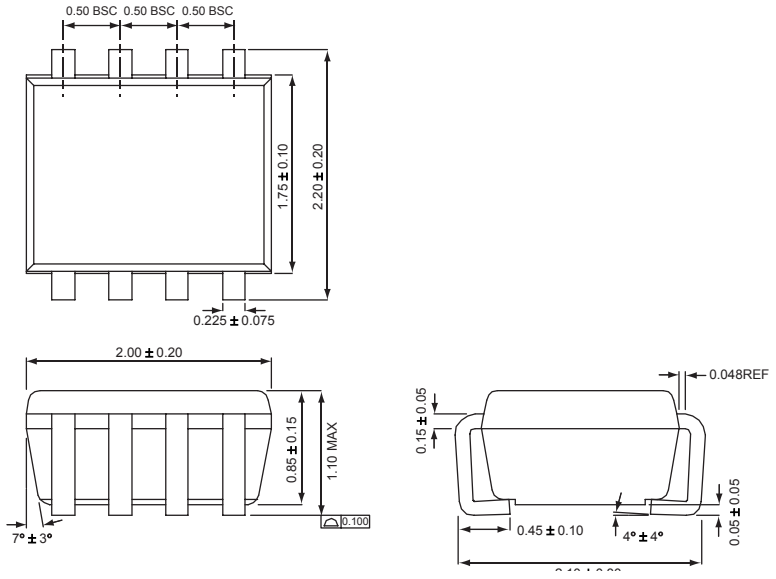
Note: Sample stock is generally held on all part numbers listed in **BOLD**.
Note 1: XYY = assembly and date code.

Package Information

SOT23-5



SC70JW-8



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