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MOTOROLA

Product Preview

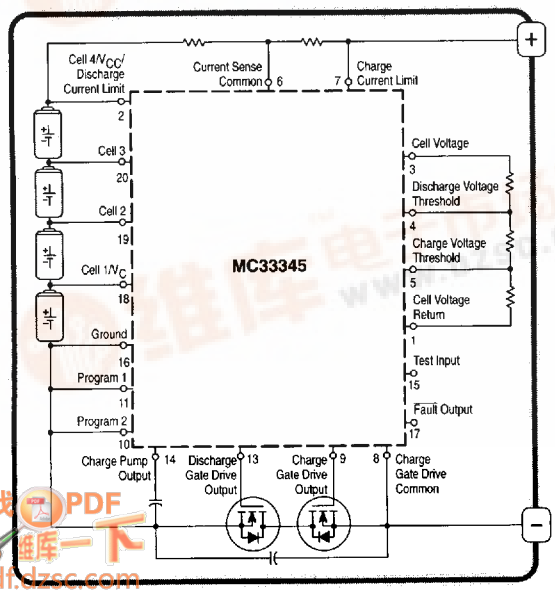
Lithium Battery Protection Circuit for One to Four Cell Battery Packs

3

The MC33345 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one to four cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, cell voltage balancing with on–chip balancing resistors, and a virtually zero current sleepmode state when the cells are discharged. Additional features include an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack, and the programmability for a one to four cell battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. The MC33345 is available in standard and low profile 20 lead surface mount packages.

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Charge and Discharge Current Limit Detection with Delayed Shutdown
- Cell Voltage Balancing
- On–Chip Balancing Resistors
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Programmable for One, Two, Three or Four Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Four Cell Smart Battery Pack

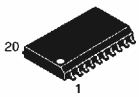


This device contains 1808 active transistors.

MC33345

LITHIUM BATTERY PROTECTION CIRCUIT FOR ONE TO FOUR CELL SMART BATTERY PACKS

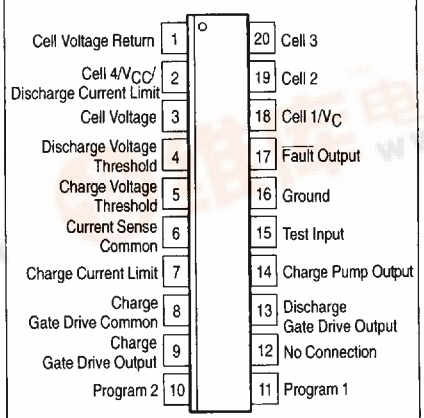
SEMICONDUCTOR TECHNICAL DATA



DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

DTB SUFFIX
PLASTIC PACKAGE
CASE 948E
(TSSOP–20)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33345DW	T_A = –25° to +85°C	SO–20L
MC33345DTB		TSSOP–20

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MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Measured with Respect to Ground, Pin 16)	V_{IR}		V
Cell Voltage Divider (Pins 1, 3, 4 and 5)		18	
Cell 1/V_C (Pin 18)		7.5	
Cell 2 (Pin 19)		10	
Cell 3 (Pin 20)		18	
Cell 4/V_{CC}/Discharge Current Limit (Pin 2)		20	
Current Sense Common (Pin 6)		30	
Charge Current Limit (Pin 7)		30	
Charge Gate Drive Common (Pin 8)		±20	
Charge Gate Drive Output (Pin 9)		18 to –20	
Program 1 (Pin 11)		7.5	
Program 2 (Pin 10)		7.5	
Discharge Gate Drive Output (Pin 13)		18	
Charge Pump Output (Pin 14)		12	
Test (Pin 15)		7.5	
$\overline{\text{Fault}}$ Output (Pin 17)		20	
Cell Voltage Divider Current	I_{div}		mA
Source Current (Pin 4 to 6)		0.5	
Sink Current (Pin 5 to 16)		0.5	
$\overline{\text{Fault}}$ Output Sink Current (Pin 17)	I_{flt}	10	mA
Thermal Resistance, Junction to Air	$R_{\theta JA}$		°C/W
DTB Suffix, TSSOP–20 Plastic Package, Case 948E		135	
DW Suffix, SO–20 Plastic Package, Case 751D		105	
Operating Junction Temperature (Notes 1, 2 and 3)	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} (Pin 2) = 8.0 V, V_C (Pin 18) = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Notes 2 and 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Charge or Discharge Voltage Inputs (Pin 4 or 5 to Pin 1)					
Threshold Voltage	V_{th}	–	1.23	–	V
Input Bias Current	I_{IB}	–	20	–	nA
Input Hysteresis Source Current (Pin 5)	I_H	–	2.0	–	µA
Cell Charge or Discharge Programmable Input Voltage Range (Pin 4 or 5)	$V_{IR(pgm)}$	–	V_{th} to 7.5	–	V
Cell Selector Series Resistance					Ω
Cell Positive to Top of Divider (Pin 2, 20, 19, or 18 to Pin 3)	R_{S+}	–	100	–	
Cell Negative to Bottom of Divider (Pin 20, 19, 18 or 16 to Pin 1)	R_{S-}	–	100	–	
Cell Voltage Sampling Rate	$t_{(smpl)}$	–	1.0	–	s
Test Input Threshold Voltage (Pin 15)	V_{th}	–	V_{Cell} 1/2.0	–	V
CELL VOLTAGE BALANCING					
Internal Balancing Resistance (Pins 2, 20, 19 and 18)	R_{bal}	–	140	–	Ω
CURRENT SENSING					
Charge Current Limit (Pin 7 to Pin 6)					
Threshold Voltage	$V_{th(chg)}$	–	18	–	mV
Input Bias Current	$I_{IB(chg)}$	–	200	–	nA
Delay	$I_{dly(chg)}$	–	1.0	–	s

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33345:
T_{low} = –25°C T_{high} = +85°C

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} (Pin 2) = 8.0 V, V_C (Pin 18) = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Notes 2 and 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSING					
Discharge Current Limit (Pin 2 to Pin 6)					
Threshold Voltage	$V_{th(dschg)}$	–	50	–	mV
Input Bias Current	$I_{IB(dschg)}$	–	200	–	nA
Delay	$I_{dly(dschg)}$	–	3.0	–	ms
CHARGE PUMP					
Output Voltage (Pin 14, $R_L \geq 10^{10}\ \Omega$)	V_O	–	10.2	–	V
TOTAL DEVICE					
Average Cell Current	I_{CC}				
Operating (V_{CC} = 8.0 V)		–	15	–	μA
Sleepmode (V_{CC} = 5.0 V)		–	5.0	–	nA
Minimum Operating Cell Voltage for Logic and Gate Drivers	V_{CC}				V
Programmed for One Cell Operation					
Cell 1 Voltage		–	2.2	–	
Programmed for Two, Three, or Four Cell Operation					
Cell 1 Voltage		–	1.5	–	
Cell 2, Cell 3, or Cell 4 Voltage, Sum Voltage of Cells		–	0.7	–	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33345:
T_{low} = −25°C T_{high} = +85°C

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Cell Voltage Return	The bottom side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the negative terminal of the cell that is to be monitored.
2	Cell 4/V_{CC}/ Discharge Current Limit	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 4 and to provide positive supply voltage for the protection IC. This pin is also used to monitor the voltage drop across the discharge current limit resistor and it provides a discharge path for the internal balancing of Cell 4.
3	Cell Voltage	The top side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the positive terminal of the cell that is to be monitored.
4	Discharge Voltage Threshold	The upper tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has fallen below the programmed level, discharge switch Q2 is disabled, and the protection circuit enters into a low current sleepmode state. This prevents further discharging of the battery pack.
5	Charge Voltage Threshold	The lower tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has risen above the programmed level, charge switch Q1 is disabled, preventing further charging of the battery pack. A 2.0 μA current source pull–up is internally applied to this pin creating input hysteresis.
6	Current Sense Common	This pin is a common point that is used to monitor the voltage drop across the charge and discharge current limit resistors.
7	Charge Current Limit	This pin is used to monitor the voltage drop across the charge current limit resistor.
8	Charge Gate Drive Common	This pin provides a gate turn–off path for charge switch Q1. The charge switch source and the battery pack negative terminal connect to this point.
9	Charge Gate Drive Output	This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging.
10	Program 2	This pin is used in conjunction with Pin 11 to program the number of cells.
11	Program 1	This pin is used in conjunction with Pin 10 to program the number of cells.
12	No Connection	This pin is not internally connected.
13	Discharge Gate Drive Output	This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging.
14	Charge Pump Output	This is the charge pump output. A reservoir capacitor is connected from this pin to ground.
15	Test Input	This input is used to facilitate circuit testing and is normally not connected. It has an internal 2.0 k pull–up resistor.
16	Ground	This is the protection IC ground and all voltage ratings are with respect to this pin.
17	Fault Output	This is on open drain output that is active low when a charging fault limit has been exceeded. The limits sensed are both charge voltage and current.
18	Cell 1/V_C	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 1 and the negative terminal of Cell 2. This pin also provides logic biasing and a discharge path for the internal balancing of Cell 1.
19	Cell 2	This pin connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 2 and the negative terminal of Cell 3. This pin also provides a discharge path for the internal balancing of Cell 2.
20	Cell 3	This pin connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 3 and the negative terminal of Cell 4. This pin also provides a discharge path for the internal balancing of Cell 3.

INTRODUCTION

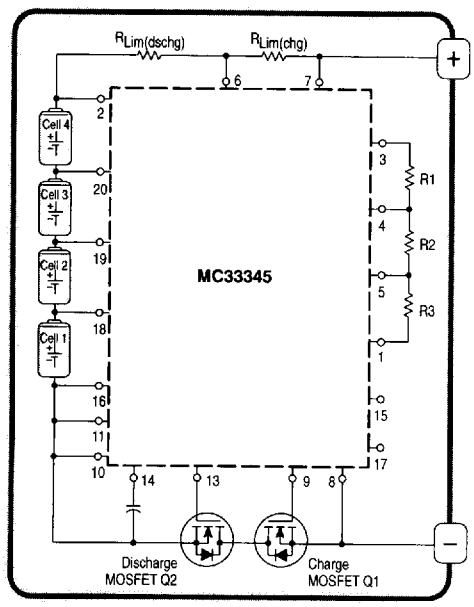
The insatiable demand for smaller lightweight portable electronic equipment has dramatically increased the requirements of battery performance. Batteries are expected to have higher energy densities, superior cycle life, be safe in operation and environmentally friendly. To address these high expectations, battery manufacturers have invested heavily in developing rechargeable lithium–based cells. Today's most attractive chemistries include lithium–polymer, lithium–ion, and lithium–metal. Each of these chemistries require electronic protection in order to constrain cell operation to within the manufacturers limits.

Rechargeable lithium–based cells require precise charge and discharge termination limits for both voltage and current in order to maximize cell capacity, cycle life, and to protect the end user from a catastrophic event. The termination limits are not as well defined as with older non–lithium chemistries. These limits are dependent upon a manufacturer's particular lithium chemistry, construction technique, and intended application. Battery pack assemblers may also choose to enhance cell capacity at the expense of cycle life. In order to address these requirements the MC33345 was developed. This device features programmable voltage and current limits, cell voltage balancing, low operating current, a virtually zero current sleepmode state, and requires few external components to implement a complete one to four cell smart battery pack.

OPERATING DESCRIPTION

The MC33345 is specifically designed to be placed in the battery pack where it is continuously powered from either one, two, three, or four lithium cells. In order to maintain cell operation within specified limits, the protection circuit senses both cell voltage and current, and correspondingly controls the state of two N–channel MOSFET switches. These switches, Q1 and Q2, are placed in series with the negative terminal of Cell 1 and the negative terminal of the battery pack.

Figure 1. Simplified Four Cell Smart Battery Pack



This configuration allows the protection circuit to interrupt the appropriate charge or discharge path FET in the event that a programmed voltage or current limit for any cell has been exceeded.

A functional description of the protection circuit blocks follows. Refer to the detailed block diagram shown in Figure 6.

Voltage Sensing

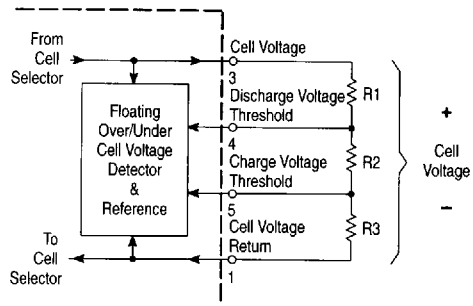
Individual cell voltage sensing is accomplished by the use of the Cell Selector in conjunction with the Floating Over/Under Voltage Detector and Reference block. The Cell Selector applies the voltage of each cell across an external resistor divider string that connects from Pins 3 to 1. The voltage at each of the tap points is sequentially polled and compared to an internal reference. If a limit has been exceeded, the result is stored in the Over/Under Data Latch and Control Logic block. The Cell Selector is gated on for an 8.0 ms period at a one second repetition rate. This low duty cycle sampling technique reduces the average load current that the divider presents across each cell, thus extending the useful battery pack capacity. The cells are sensed in the following sequence:

Figure 2. Cell Sensing Sequence

Polling Sequence	Time (ms)	Cell Sensed	Tested Limit
1	1.0	Cell 4	Overvoltage
2	1.0	Cell 3	Overvoltage
3	1.0	Cell 2	Overvoltage
4	1.0	Cell 1	Overvoltage
5	1.0	Cell 4	Undervoltage
6	1.0	Cell 3	Undervoltage
7	1.0	Cell 2	Undervoltage
8	1.0	Cell 1	Undervoltage

By incorporating this polling technique with a single floating comparator and voltage divider, a significant reduction of circuitry and trim elements is achieved. This results in a smaller die size, lower cost, and reduced operating current.

Figure 3. Cell Voltage Limit Programming



The cell charge and discharge voltage limits are controlled by the values selected for the resistor divider string and the 1.23 V input threshold of Pins 4 and 5. As the battery pack reaches full charge, the Cell Voltage Detector will sense an overvoltage fault condition on the first cell that exceeds the programmed overvoltage limit. The fault information is stored

in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. An internal 2.0 μA current source pull–up is then applied to Pin 5 creating an input hysteresis voltage. As a result of an overvoltage fault, the battery pack is available for discharging only.

The overvoltage fault is reset by applying a load to the battery pack. As the voltage across each cell falls below the input hysteresis level, charge MOSFET Q1 will turn on. The battery pack will now be available for charging or discharging. The over voltage limit and hysteresis voltage are given by:

$$V_{OV} = V_{th\ (Pin\ 5)}\left(\frac{R1 + R2 + R3}{R3}\right)$$

$$V_H = I_{H\ (Pin\ 5)}(R1 + R2)$$

As the load eventually depletes the battery pack charge, the Cell Voltage Detector will sense an undervoltage fault condition on the first cell that falls below the programmed undervoltage limit. After an undervoltage cell is detected, discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. The protection circuit will now enter a low current sleepmode state drawing just 5.0 nA typically, thus preventing any further cell discharging. As a result of the undervoltage fault, the battery pack is available for charging only. The undervoltage limit is given by:

$$V_{UV} = V_{th\ (Pin\ 4)}\left(\frac{R1 + R2 + R3}{R2 + R3}\right)$$

The undervoltage fault is reset by applying charge current to the battery pack. When the voltage on Pin 16 exceeds Pin 8 by 0.6 V, discharge MOSFET Q2 will turned on. The battery pack will now be available for charging or discharging.

Since the thresholds of Pins 4 and 5 are equal, the above equations can be rewritten to directly solve for specific resistor values as shown in the example below.

Let the desired limits be:

V_{OV} = 4.2 V, V_H = 0.4 V, and V_{UV} = 2.5 V

With nominal values for:

V_{th} = 1.23 V, and I_H = 2.0 μA

$$R3 = \frac{\left(\frac{V_H}{I_H}\right)}{\left(\frac{V_{OV}}{V_{th}} - 1\right)} = \frac{\left(\frac{0.4}{2.0 \times 10^{-6}}\right)}{\left(\frac{4.2}{1.23} - 1\right)} = 82{,}828\ \Omega$$

$$R2 = R3\left(\frac{V_{OV}}{V_{UV}} - 1\right) = 82{,}828\left(\frac{4.2}{2.5} - 1\right) = 56{,}323\ \Omega$$

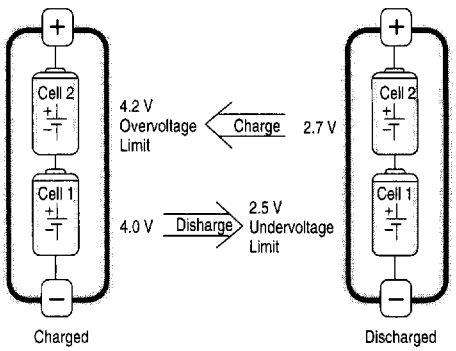
$$R1 = \left(\frac{V_H}{I_H}\right) - R2 = \left(\frac{0.4}{2.0 \times 10^{-6}}\right) - 56{,}323 = 143{,}677\ \Omega$$

Note that the Cell Selector has a typical total series resistance of 200 Ω. This will have a minimal effect on the programmed limits if the total divider resistance is in excess of 100 kΩ.

Cell Voltage Balancing

With series connected cells, successive charge and discharge cycles can result in a significant difference in cell voltage with a corresponding degradation of battery pack capacity. Figure 4 illustrates the operation of an unbalanced two cell pack. As the cells become unbalanced, the full battery pack capacity is not realized. This is due to the requirement that charging must terminate when Cell 2 reaches the overvoltage limit, and discharging must terminate when Cell 1 reaches the undervoltage limit. By employing a method of keeping the cell voltages equal, both cells can be charged and discharged to their specified limits, thus attaining the maximum possible capacity .

Figure 4. Unbalanced Battery Pack Operation



The MC33345 contains a Cell Voltage Balancing Logic circuit that controls four N–channel MOSFETs. The circuit samples the voltage of each cell during the polling period. If all of the cells are below the programmed overvoltage fault limit, no cell balancing takes place. If one or more cells reach the overvoltage fault limit, a specific latch is set for each cell. At the end of the polling period, charge MOSFET Q1 is turned off and the latches are interrogated. If all of the latches were set, no cell balancing takes place. If one, two, or three latches were set, the required cell balancing MOSFETs are then activated. The overvoltage cells are discharged to the programmed level of $V_{OV} - V_H$. As each cell attains this level, the discharge MOSFETs successively turn off. Upon completion of cell balancing, charge MOSFET Q1 is turned on. Cell voltage balancing is active during charge and discharge, but disabled during the low current sleepmode state.

Cell Programming and Test

The protection circuit can be programmed for operation with either one, two, three, or four cell battery packs. Programming inputs 1 and 2 are used to set up the internal logic for the number of cells to be monitored. If less than four cells are required, the input for each empty cell position must be connected to V_{CC}. This process starts with Cell 4 decending down to Cell 2 if required. Refer to the Cell Programming table shown below and the specific application figure.

Figure 5. Cell Sensing Sequence

Number of Cells	Program 1 (Pin 11)	Program 2 (Pin 10)	Application Figure
1	Ground	Cell 1/V_C	16
2	Cell 1/V_C	Ground	15
3	Cell 1/V_C	Cell 1/V_C	14
4	Ground	Ground	13

A test option is provided to speed up device and battery pack testing. By connecting Pin 15 to ground, the internal logic is held in a reset state and both MOSFET switches are turned on. Upon release, the Control Logic becomes active and the cells are polled within 8.0 ms.

Current Sensing

Charge and discharge current limit protection can be selectively added to the battery pack with the addition of a sense resistor. The resistors are placed in series with the positive terminal of the battery pack and the cells. Refer to Figure 1.

As the battery pack charges, Pins 6 and 7 sense the voltage drop across $R_{Lim(chg)}$. A charge current limit fault is detected if the voltage at Pin 7 exceeds Pin 6 by 18 mV for the entire delay period of 1.0 second. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. As a result of the charge current fault, the battery pack is available for discharging only. The charge current limit is given by:

$$I_{Lim(chg)} = \frac{V_{th(chg)}}{R_{Lim(chg)}} = \frac{18\ mV}{R_{Lim(chg)}}$$

The charge current fault is reset by either disconnecting the battery pack from the charger, or by connecting a load to the battery pack. When the voltage on Pin 16 no longer exceeds Pin 8 by approximately 2.0 V, the Sense Enable circuit will turn on charge MOSFET Q1. Charge current sensing can be disabled by connecting Pin 7 to Pin 6.

The discharge current limiting operates in a similar manner. As the battery pack discharges, Pins 2 and 6 sense the voltage drop across $R_{Lim(dschg)}$. A discharge current limit fault is detected if the voltage at Pin 2 is less than Pin 6 by 50 mV for more than 3.0 ms. The fault information is stored in a data latch and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. As a result of the discharge current fault, the battery pack is available for charging only. The discharge current limit is given by:

$$I_{Lim(dschg)} = \frac{V_{th(dschg)}}{R_{Lim(dschg)}} = \frac{50\ mV}{R_{Lim(dschg)}}$$

The discharge current fault is reset by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. When the voltage on Pin 8 no longer exceeds Pin 16 by approximately 2.0 V, the Sense Enable circuit will turn on discharge MOSFET Q2. Discharge current sensing can be disabled by connecting Pin 2 to Pin 6.

The charge and discharge current protection circuits contain a built in response delay of 1.0 s and 3.0 ms respectively. This helps to prevent fault activation when the battery pack is subjected to pulsed currents during charging or discharging.

Charge Pump and MOSFET Switches

The MC33345 contains an on chip Charge Pump to ensure that the MOSFET switches are fully enhanced for reduced power losses. An external reservoir capacitor normally connects from the Charge Pump output to ground, Pins 14 and 16. The capacitor value is not critical and is usually within the range of 10 nF to 100 nF. The Charge Pump output is regulated at 10.2 V allowing the use of economical logic level MOSFETs in one and two cell applications. The main requirement in selecting a particular type of MOSFET switch is to consider the desired on–resistance at the lowest anticipated operating voltage of the battery pack. A table of small outline surface mount devices is given in Figure 6. When using extremely low threshold MOSFETs, it may be desirable to disable the Charge Pump so that the maximum gate to source voltage is not exceeded. This is accomplished by connecting Pin 14 to Pin 19 with two, three, or four cell battery packs.

Battery Pack Application

Upon assembly of the battery pack, it is imperative that Cell 1 be connected first so that V_C is properly biased. The remaining cells can then be connected in any order. This assembly method prevents forward biasing the protection IC substrate which can result in overheating and non–functionality.

Each of the application figures show a capacitor labeled C_{ESD}. This capacitor provides a path around the MOSFET switches in the event of an electrostatic discharge.

Figure 6. Small Outline Surface Mount MOSFET Switches

Device Type	On–Resistance (Ω) versus Gate to Source Voltage (V)						
	2.5 V	3.0 V	4.0 V	5.0 V	6.0 V	7.5 V	9.0 V
MMFT3055VL	–	–	–	0.120 Ω	0.115 Ω	0.108 Ω	0.100 Ω
MMDF3N03HD	–	0.525 Ω	0.080 Ω	0.065 Ω	0.063 Ω	0.062 Ω	0.060 Ω
MMDF4N01HD	0.047 Ω	0.042 Ω	0.037 Ω	0.035 Ω	0.034 Ω	0.033 Ω	See Note
MMSF5N02HD	–	0.065 Ω	0.023 Ω	0.021 Ω	0.020 Ω	0.018 Ω	0.018 Ω
MMDF6N02HD	0.043 Ω	0.035 Ω	0.029 Ω	0.028 Ω	0.026 Ω	0.025 Ω	0.023 Ω

NOTE: Exceeds maximum V_{GS} voltage rating.

PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs			
		MOSFET Switches		Function	
		Charge Q1	Discharge Q2	Charge Pump	Cell Balancing (See Note)
CELL CHARGING/DISCHARGING					
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On	Active	Active
CELL CHARGING FAULT/RESET					
Charge Current Limit Fault: $V_{Pin\ 7} \geq (V_{Pin\ 6} + 18\ mV)$ for 1.0 s	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. Q1 will remain in the off state as long as $V_{Pin\ 16}$ exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Current Limit Reset: $V_{Pin\ 16} - V_{Pin\ 8} < 2.0\ V$	The Sense Enable circuit will reset and turn on charge MOSFET Q1 when $V_{Pin\ 16}$ no longer exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the charger from the battery pack, or by connecting a load to the battery pack.	Off to On	On	Active	Active
Charge Voltage Limit Fault: $V_{Pin\ 5} \geq 1.23\ V$ for 1.0 s	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. An internal current source pull–up of 2.0 μA is applied to Pin 8 creating an input hysteresis voltage of V_H with divider resistors R1 and R2. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Voltage Limit Reset: $V_{Pin\ 5} < 1.23\ V$ for 1.0 s	Charge MOSFET Q1 will turn on when the voltage across each cell falls sufficiently to overcome the input hysteresis voltage. This can be accomplished by applying a load to the battery pack.	Off to On	On	Active	Active
CELL DISCHARGING FAULT/RESET					
Discharge Current Limit Fault: $V_{Pin\ 6} \leq (V_{Pin\ 2} - 50\ mV)$ for 3.0 ms	Discharge MOSFET Q2 is latched off and the cells are disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 11}$ exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. The battery pack is available for charging.	On	On to Off	Active	Active
Discharge Current Limit Reset: $V_{Pin\ 8} - V_{Pin\ 16} < 2.0\ V$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 11}$ no longer exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On	Active	Active
Discharge Voltage Limit Fault: $V_{Pin\ 4} \leq 1.23\ V$ for 1.0 s	Discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging.	On	On to Off	Disabled	Disabled
Discharge Voltage Limit Reset: $V_{Pin\ 16} > (V_{Pin\ 8} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 16}$ exceeds $V_{Pin\ 8}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On	Active	Active
FAULTY CELL					
Simultaneous Charge and Discharge Voltage Limit Faults: $V_{Pin\ 5} \geq 1.23\ V$ for 1.0 s and $V_{Pin\ 4} \leq 1.23\ V$ for 1.0 s	This condition can happen if there is a defective cell in the battery pack. The protection circuit will remain in the sleepmode state until the battery pack is connected to a charger. If Cell 2, 3, or 4 is faulty and a charger is connected, the protection circuit will cycle in and out of sleepmode. If Cell 1 is faulty (<1.5 V), the protection circuit logic will not function and the battery pack cannot be charged.	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty

NOTE: Cell balancing is not active when programmed for one cell operation.

3

Figure 7. Four Cell Smart Battery Pack

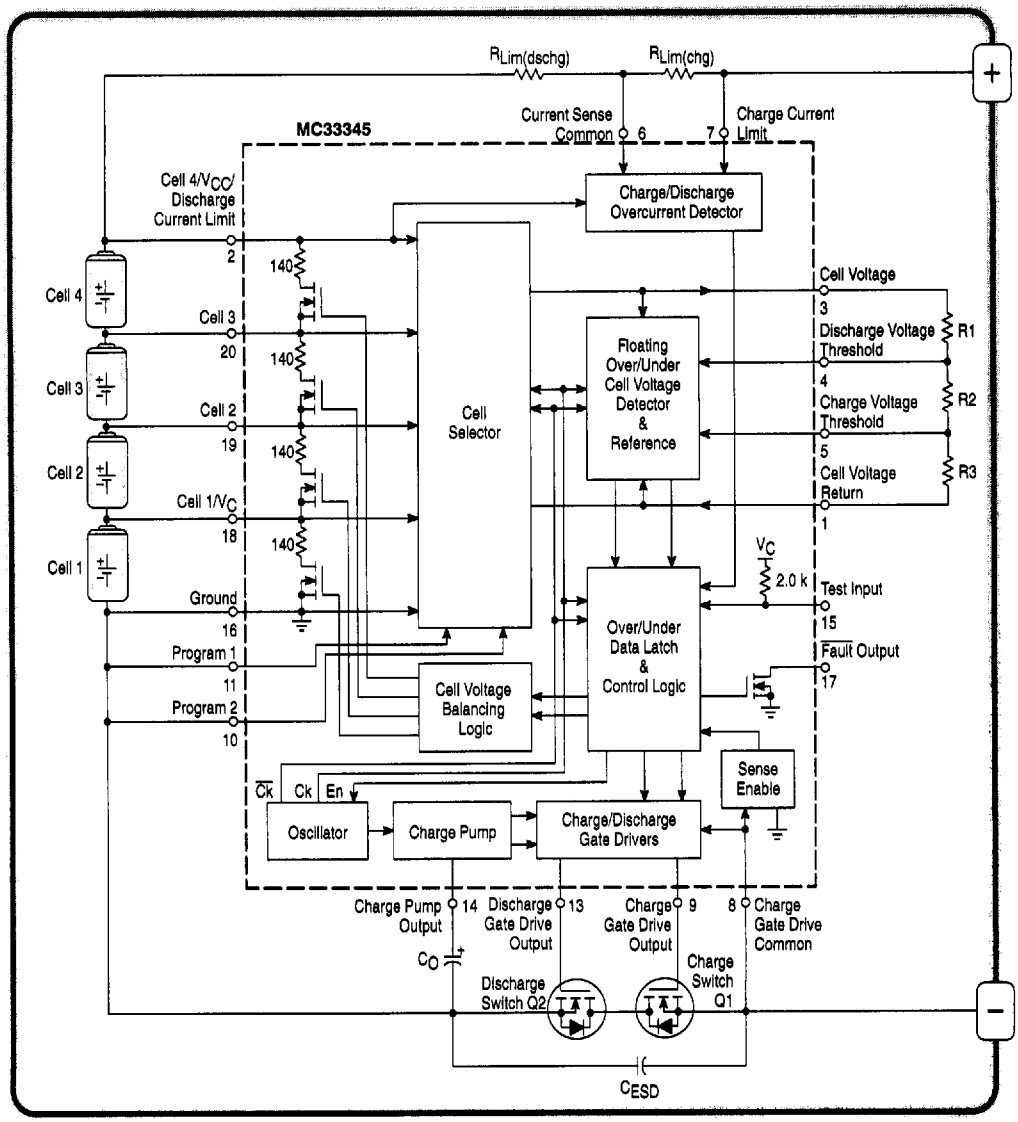


Figure 8. Three Cell Smart Battery Pack

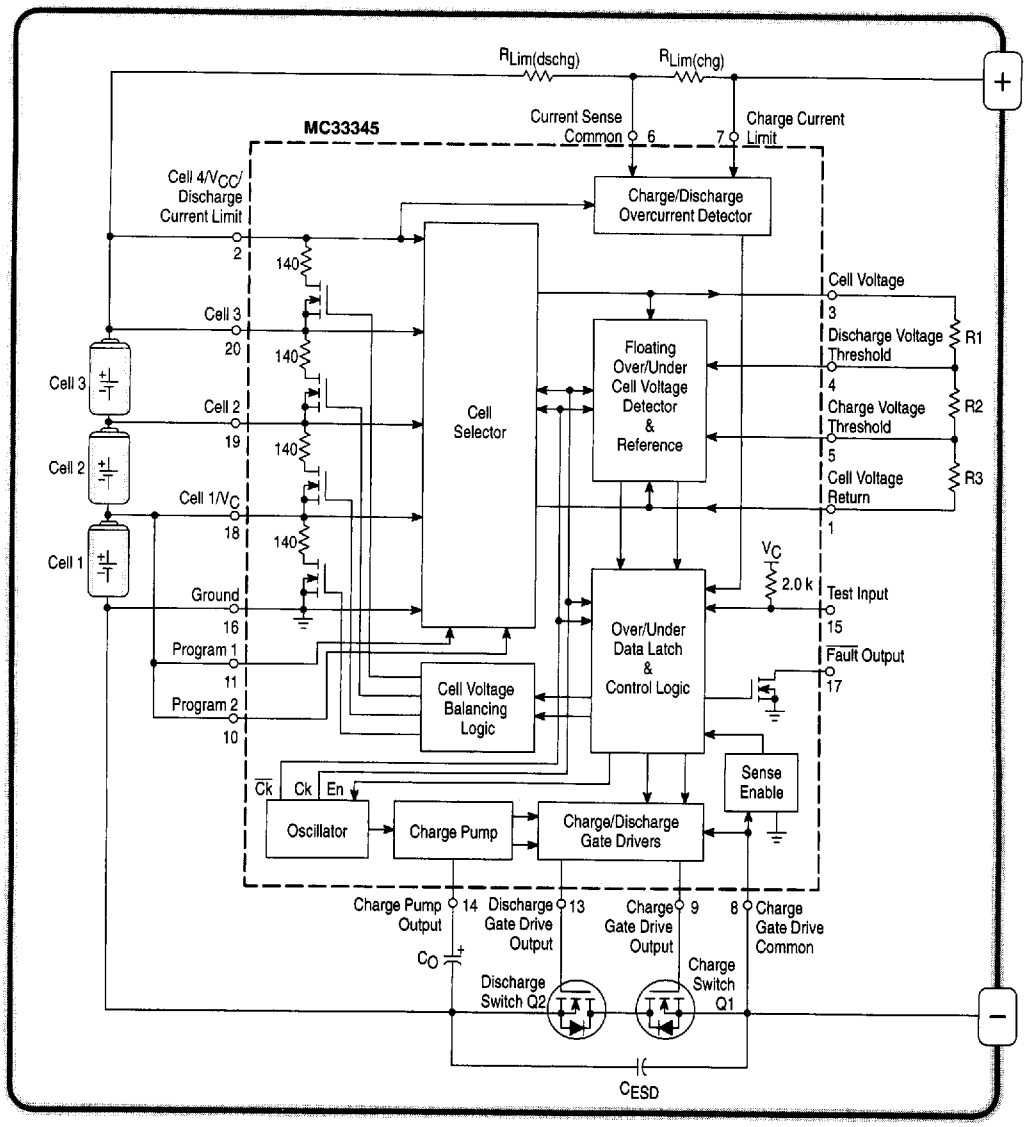


Figure 9. Two Cell Smart Battery Pack

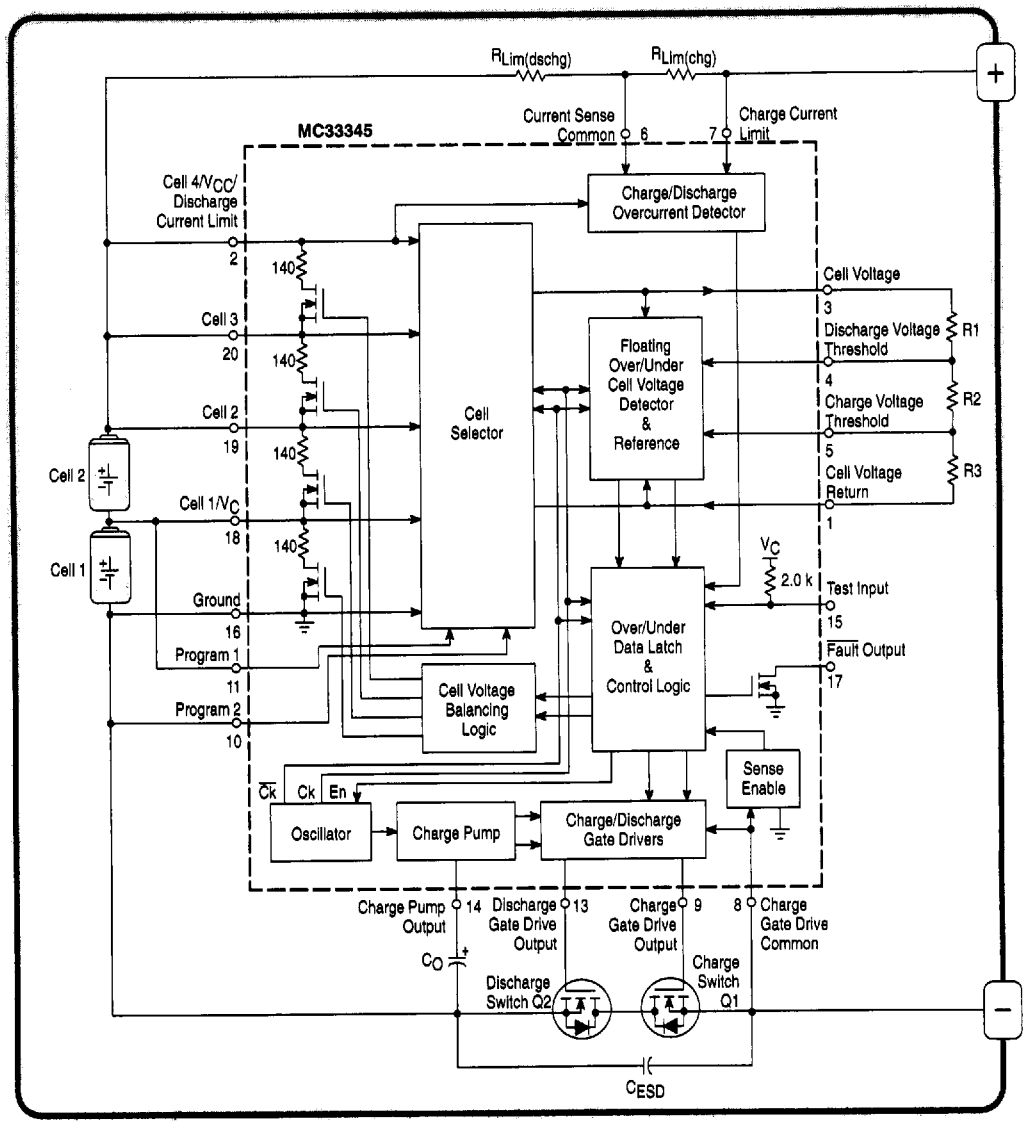


Figure 10. One Cell Smart Battery Pack