NEC Electronics Inc.

μPD75116F Family (μPD75108F/112F/116F) 4-Bit High-End Single-Chip Microcontrollers

October 1994

Description

The μPD75116F family of high-performance single-chip CMOS microcontrollers offers the same functions as the μPD75116 family. The μPD75116F family is optimized for operation at low voltages with a faster cycle time at 2.7 volts and a maximum operating voltage of 5.0 volts. The μPD75116F family includes the following devices:

μPD75108F μPD75112F μPD75116F

The μPD75116F family features a 4-bit programmable threshold comparator and 58 I/O lines. The μPD75116F family uses the high-end 75x instruction set, which is rich in 8-bit operations including 8-bit add and subtract. The instruction set operates on 1-, 4-, and 8-bit operands.

Timing is generated by a single oscillator. Since CMOS power dissipation is proportional to clock rate, the μPD75116F provides a software selectable instruction cycle time from 0.95 μs to 15.3 μs at 4.19 MHz. The STOP and HALT modes turn off parts of the microcontroller for additional power saving. The data retention mode retains RAM contents down to 2.0 V.

Features

- 4-input programmable threshold comparator
- 58 I/O lines
  - 32 outputs can directly drive LEDs
  - 12 n-channel, open-drain output lines at 10 V maximum
  - 44 bidirectional I/O lines
  - 14 input-only lines
- 8-bit clock-synchronous serial interface
  - Full-duplex, three-wire mode
  - Half-duplex, two-wire mode
- Timers: three channels
  - Two 8-bit timer/event counters
  - 8-bit interval timer
- Bit sequential buffer
  - 16-bit, bit addressable memory
- Hi-end 75x instruction set
  - Bit manipulation
  - 8- and 4-bit transfer, arithmetic, logical, comparison, and increment/decrement instructions
  - 1-byte relative branch
  - GETI instruction; converts one 2-byte, one 3-byte branch or call, or two 1-byte instructions into a single 1-byte instruction
- Minimum instruction execution times
  - 0.95, 1.91, and 15.3 μs using 4.19-MHz system clock
- Four banks of eight 4-bit registers
  - Usable as four 8-bit registers
- Memory-mapped on-chip peripherals
  - Special function registers
- Vectored interrupt controller
  - Five external and four internal sources
  - Five edge-detect inputs
  - Five vectored interrupts
- Power saving and battery backup
  - Variable CPU clock rate; 3 mA typical at 5 V, 4.19 MHz
  - HALT mode stops CPU; 0.6 mA typical current drain
  - STOP mode, stops oscillator; 0.1 μA typical power drain
  - 2.0 volt data retention mode
- CMOS operation
  - ROM versions; V_{DD} from 2.7 to 5.0 V

Internal High Capacity ROM and RAM

	75108F	75112F	75116F	75P108B*	75P116*
ROM	8064 bytes	12,160 bytes	16,256 bytes	—	—
PROM	—	—	—	8064 bytes	16,256 bytes
RAM	512 nibbles	512 nibbles	512 nibbles	512 nibbles	512 nibbles

* See the μPD75116 family data sheet for the μPD75P108B and the μPD75P116 electrical and functional specifications.

Ordering Information

Part Number	Quality Grade	ROM	Package Type	Package Drawing No.
μPD75108FGF-xxx-3BE	Standard	Mask	64-pin plastic QFP	P64GF-100-3B8, 3BE-1
μPD75112FGF-xxx-3BE				
μPD75116FGF-3BE				

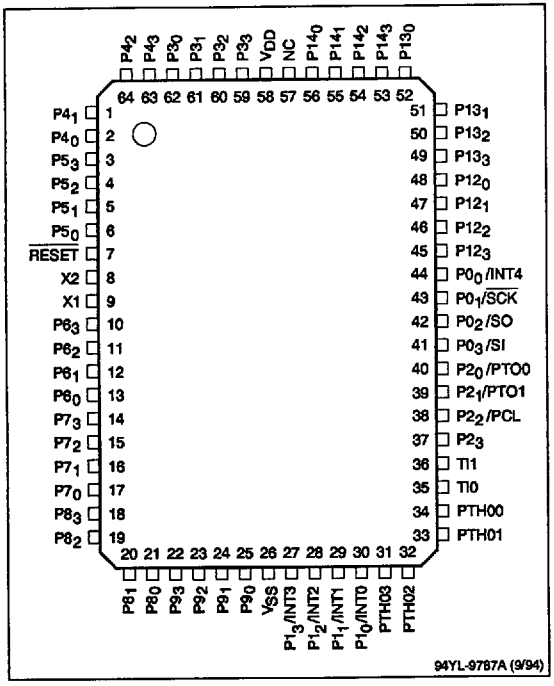
Notes:

(1) Engineering samples are supplied in a 64-pin ceramic QFP.

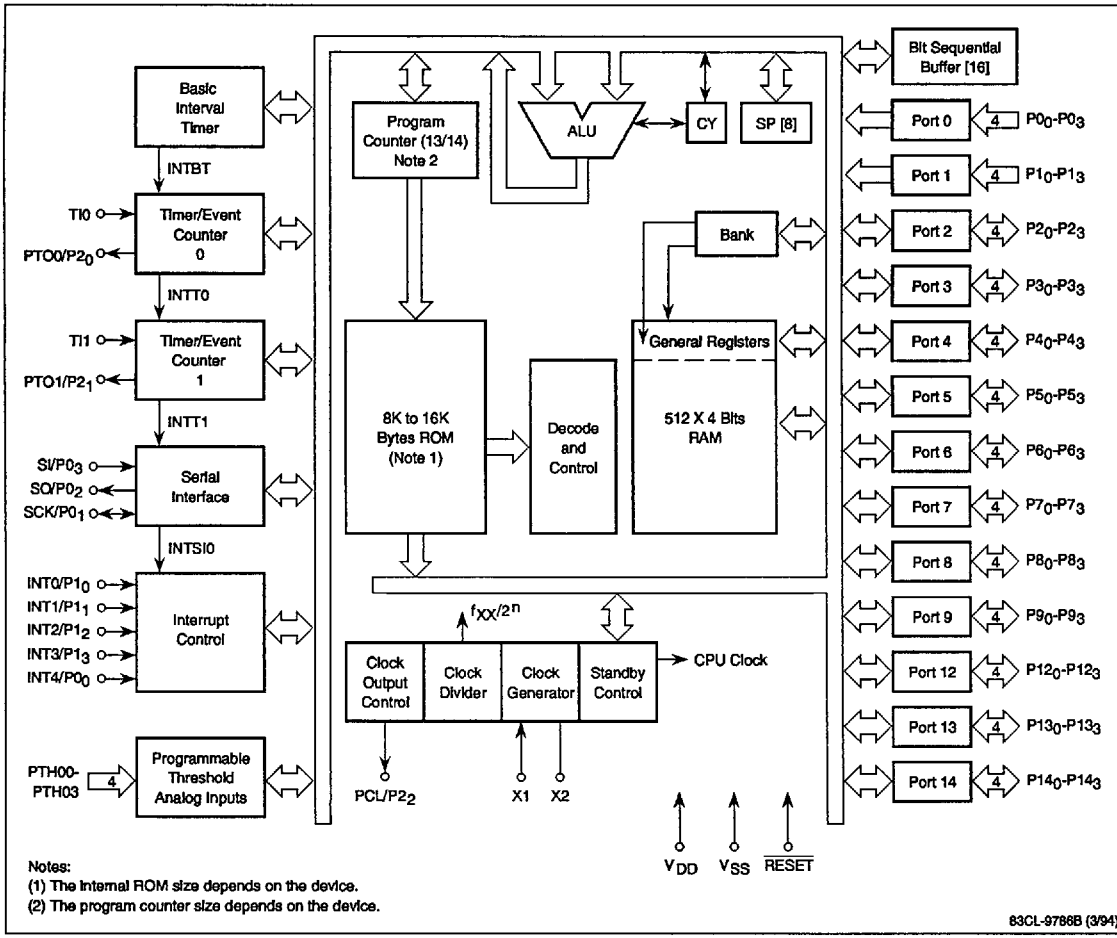
(2) xxx indicates ROM code suffix.

Pin Configurations

64-Pin Plastic QFP



Block Diagram



Notes:
(1) The internal ROM size depends on the device.
(2) The program counter size depends on the device.

83CL-9788B (3/94)

Pin Identification

Symbol	Function
$P0_0$/INT4	Port 0 input; interrupt 4
$P0_1$/$\overline{SCK}$	Port 0 input; serial clock
$P0_2$/SO	Port 0 input; serial out
$P0_3$/SI	Port 0 input; serial in
$P1_0$/INT0	Port 1 input; interrupt 0
$P1_1$/INT1	Port 1 input; interrupt 1
$P1_2$/INT2	Port 1 input; interrupt 2
$P1_3$/INT3	Port 1 input; interrupt 3
$P2_0$/PTO0	Port 2 I/O; timer/event counter 0
$P2_1$/PTO1	Port 2 I/O; timer/event counter 1
$P2_2$/PCL	Port 2 I/O; clock output
$P2_3$	Port 2 I/O
$P3_0$	Port 3 I/O
$P3_1$	Port 3 I/O
$P3_2$	Port 3 I/O
$P3_3$	Port 3 I/O
$P4_0$ - $P4_3$	Port 4 I/O
$P5_0$ - $P5_3$	Port 5 I/O
$P6_0$ - $P6_3$	Port 6 I/O
$P7_0$ - $P7_3$	Port 7 I/O
$P8_0$ - $P8_3$	Port 8 I/O
$P9_0$ - $P9_3$	Port 9 I/O
$P12_0$ - $P12_3$	Port 12 I/O
$P13_0$ - $P13_3$	Port 13 I/O
$P14_0$ - $P14_3$	Port 14 I/O
PTH00 - PTH03	4-bit programmable threshold comparator analog input port
$\overline{RESET}$	Reset input
TI0/TI1	Event timer/counter external input
V_{DD}	Positive power supply
V_{SS}	Ground
X1, X2	Main clock inputs
NC	No connection

PIN FUNCTIONS

$P0_0$/INT4, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI. These pins can be used as the 4-bit input port 0. $P0_0$ can be used for vectored interrupt 4, which interrupts on both the leading edge and the trailing edge of the signal. $P0_1$ - $P0_3$ may also be used for the serial interface; SI is the serial input, SO is the serial output, and $\overline{SCK}$ is the serial clock. Reset causes these pins to default to the port 0 input mode.

$P1_0$/INT0, $P1_1$/INT1, $P1_2$/INT2, $P1_3$/INT3. These pins can be used as 4-bit input port 1. They can also be used, respectively, for edge-triggered interrupts INT0, INT1, INT2, and INT3. INT0 and INT1 are triggered by rising or falling edges, while INT2 and INT3 respond to rising edges only and generate an interrupt request but not an interrupt. Reset causes these pins to default to the port 1 input mode.

$P2_0$/PTO0, $P2_1$/PTO1, $P2_2$/PCL, $P2_3$. These pins can be used as 4-bit I/O port 2. This port has latched outputs and can directly drive LEDs. PTO0 and PTO1 are the timer/event counter output pins; PCL is the clock output pin. Reset causes these pins to default to the port 2 input mode.

$P3_0$/MD0, $P3_1$/MD1, $P3_2$/MD2, $P3_3$/MD3. These pins are used for I/O port 3. Each bit in this port can be independently programmed to be either an input or an output. This port has latched outputs and can directly drive LEDs. A reset signal causes this port to default to the input mode.

$P4_0$ - $P4_3$, $P5_0$ - $P5_3$. Port 4 and port 5 are identical 4-bit I/O ports that can be combined together to function as a single 8-bit port. Latched outputs will directly drive LEDs. A reset signal causes these ports to default to the input mode.

$P6_0$ - $P6_3$, $P7_0$ - $P7_3$. Port 6 and port 7 are 4-bit I/O ports; port 6 is I/O bit programmable. These ports may be combined together to function as a single 8-bit port. Latched outputs will directly drive LEDs. A reset signal causes these ports to default to the input mode.

$P8_0$ - $P8_3$, $P9_0$ - $P9_3$. Port 8 and port 9 are identical 4-bit I/O ports that can be combined together to function as a single 8-bit port. Latched outputs will directly drive LEDs. A reset signal causes these ports to default to the input mode.

$P12_0$ - $P12_3$, $P13_0$ - $P13_3$. Port 12 and port 13 are identical 4-bit I/O ports that can be combined together to function as a single 8-bit port. Latched outputs will directly drive LEDs. Outputs are n-channel open drain, and can withstand up to 10 volts; pullup resistor mask options are available for these ports. A reset signal causes these ports to default to the input mode.

$P14_0$ - $P14_3$. Port 14 is a 4-bit I/O port. Latched outputs will directly drive LEDs. Outputs are n-channel open drain, and can withstand up to 10 volts; pullup resistor mask options are available for this port. A reset signal causes the port to default to the input mode.

PTH00 - PTH03. 4-channel comparator with 4-bit resolution and on-chip resistor ladder.

TI0, TI1. External event input for the timer/event counters. Each pin can also act as an edge-triggered vectored interrupt and a 1-bit input port.

NC. This pin may be left unconnected when using the μPD751xxF. Pin must be connected to V_{DD} if the same circuit board is used for both programmable and non-programmable devices.

X1, X2. These pins are the system clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

$\overline{RESET}$. This is the reset input and it is active low.

V_{DD}. The system positive power supply pin.

V_{SS}. System ground.

The table below compares the mask ROM parts with the two OTP/EPROM devices used for prototyping (μPD75P108B and the μPD75P116). For full specifications on the μPD75P108B and the μPD75P116 devices, refer to the μPD75116 data sheet.

Product Comparison

Item	μPD75108F	μPD75112F	μPD75116F	μPD75P108B *	μPD75P116 *
Program memory	Mask ROM 8064 x 8 bits 000H–1F7FH	Mask ROM 12,160 x 8 bits 000H–2F7FH	Mask ROM 16,256 x 8 bits 000H–3F7FH	OTP; EPROM 8064 x 8 bits 000H-1F7FH	OTP; EPROM 16,256 x 8 bits 000H-3FFFH
Data memory	512 x 4 bits				
3-byte branch instructions	Yes				
Other instructions	Common to the products				
Program counter	13-bit	14-bit	14-bit	13-bit	14-bit
Ports 12, 13, and 14 pullup resistor	Mask option			No	
N-channel open drain output, maximum voltage	+ 10 V			+12 V	
Power-on reset circuit and flag	No				
V_{PP}, PROM programming pins	No			Yes	
Operating voltage and temperature ranges	2.7 to 5.0 V (T_A = −40 to +50°C)			2.7 to 6.0 V (T_A = −40 to +85°C)	4.5 to 5.5 V (T_A = −40 to +85°C)
	2.8 to 5.0 V (T_A = −40 to +60°C)				
Minimum instruction execution time (4.19 MHz)	1.91 μs (V_{DD} = 2.7 V; T_A = −40 to +50°C) 0.95 μs (V_{DD} = 4.5 V; T_A = −40 to +60°C)			3.8 μs (V_{DD} = 2.7 V); 0.95 μs (V_{DD} = 4.5 V)	1.1 μs (V_{DD} = 4.5 V); 0.95 μs (V_{DD} = 4.75 V)
Package	See ordering information for a complete listing of the packages				

* See the μPD75116 family data sheet for the μPD75P108B and the μPD75P116 electrical and functional specifications.

Differences Among the μPD75116, μPD75116F, and μPD75117H Families

		75116 Family *	75116F Family	75117H Family *
Power-on reset circuit and flag		Mask Option	No	No
N-channel open-drain output lines		12	12	12
Specified for direct LED drive		Yes	Yes	No
N-channel open-drain output, maximum voltage		+12 V	+10 V	+6 V
Minimum instruction execution time (4.19 MHz)	4.5 V	0.95 μs	0.95 μs	0.95 μs
	2.7 V	3.8 μs	1.91 μs (T_A = −40 to +50°C)	0.95 μs
	1.8 V			1.91 μs
Voltage operation and temperature ranges		2.7 to 6.0 V (T_A = −40 to +85°C)	2.7 to 5.0 V (T_A = −40 to +50°C)	1.8 to 5.0 V (T_A = −40 to +60°C)
			2.8 to 5.0 V (T_A = −40 to +60°C)	

* Refer to the μPD75116 and 75117H family data sheets for more information.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +5.5 V
Input voltage, V_{I1} (except ports 12-14)	−0.3 to V_{DD} + 0.3 V
Input voltage, V_{I2} (ports 12-14; internal pullup resistor)	−0.3 to V_{DD} + 0.3 V
Input voltage, V_{I2} (ports 12-14; open drain)	−0.3 to +11 V (Note 1)
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
High-level output current, I_{OH} (Single pin)	−15 mA
High-level output current, I_{OH} (Total of all pins)	−30 mA
Low-level output current, I_{OL} (Single pin)	30 mA peak
	15 mA rms (Note 2)
Low-level output current, I_{OL} (Total of ports 0, 2–4, 12–14)	100 mA peak
	60 mA rms (Note 2)
Low-level output current, I_{OL} (Total of ports 5–9)	100 mA peak
	60 mA rms (Note 2)
Operating temperature, t_{OPT}	−40 to + 60°C
Storage temperature, t_{STG}	−65 to +150°C

Notes:

(1) When applying more than 10 V to ports 12, 13, or 14, the external pullup resistor must be at least 50 kΩ

(2) rms value = peak x (duty cycle)$^{1/2}$.

(3) Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Capacitance

V_{DD} = 0 V; T_A = 25°C

Parameter	Symbol	Max	Unit	Conditions
Input capacitance	C_{IN}	15	pF	f = 1 MHz; all unmeasured pins returned to ground
Output capacitance	C_{OUT}	15	pF	
I/O capacitance	C_{IO}	15	pF	

Oscillator Characteristics

T_A = −40 to +60°C; V_{DD} = 2.7 to 5.0 V

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Ceramic resonator (figure 1A)	Oscillation frequency (Note 1)	f_{XX}	2.0		5.0	MHz	
	Oscillation stabilization time (Note 2)				4 (Note 3)	ms	After V_{DD} reaches oscillation voltage
Crystal resonator (figure 1A)	Oscillation frequency (Note 1)	f_{XX}	2.0	4.19	5.0 (Note 4)	MHz	
	Oscillation stabilization time (Note 2)				10 (Note 3)	ms	V_{DD} = 4.5 to 5.0 V
					30 (Note 3)	ms	
External clock (figure 1B)	X1 input frequency (Note 1)	f_{XX}	2.0		5.0	MHz	
	X1 input high/low-level width	t_{XH}, t_{XL}	100		250	ns	

Notes:

(1) The oscillation frequency and X1 input frequency are included only to show the characteristics of the oscillators. Refer to the AC Characteristics table for actual instruction execution times.

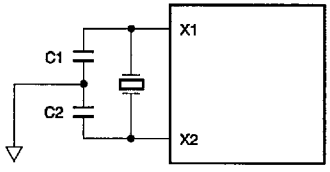
(2) The oscillation stabilization time is the time required for the oscillator to stabilize after voltage is applied or the STOP mode is released.

(3) Values shown are for the recommended resonators. Values for resonators not shown in this data sheet should be obtained from the manufacturer's spec sheets.

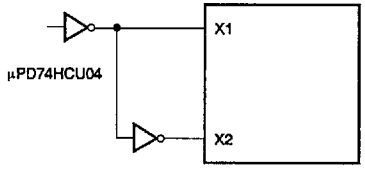
(4) When the oscillator frequency is 4.19 MHz < f_{XX} < 5.0 MHz, PCC = 0011 should not be selected as the instruction execution time. If PCC = 0011 is selected, one machine cycle is less than 0.95 μs and the rated minimum value of 0.95 μs is not observed.

Figure 1. System Clock Configurations

A. Ceramic/Crystal Resonator



B. External Clock



Note: When the input is an external clock, the stop mode cannot be set because the X1 pin is connected to System ground (V_{SS}).

83RD-6905A

Recommended Ceramic Resonators

Manufacturer	Part Number	C1 (pF)	C2 (pF)	Remarks
Murata	CSA 2.00MG	30	30	V_{DD} = 2.7 to 5.0 V
	CSA 4.19MG	30	30	V_{DD} = 3.0 to 5.0 V
	CSA 4.19MGU	30	30	V_{DD} = 2.7 to 5.0 V
	CST 4.19T (Note)	—	—	V_{DD} = 3.0 to 5.0 V
Kyocera	KBR-2.0MS	100	100	V_{DD} = 3.0 to 5.0 V
	KBR-4.0MS	33	33	
	KBR-4.19MS	33	33	
	KBR-4.9152M	33	33	

Note: C1 and C2 are contained in the oscillator.

Recommended Crystal Resonator

Manufacturer	Frequency (MHz)	Part No. (Note)	C1 (pF)	C2 (pF)	Remarks
Kinseki	4.19	HC-49/U	22	22	V_{DD} = 2.7 to 5.0 V

Note: Equivalent series resistance of crystal must be less than 80 Ω.

Comparator Characteristics

V_{DD} = 4.5 to 5.0 V; T_A = −40 to +60°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Comparison accuracy	V_{ACOMP}			±100	mV	
Threshold voltage	V_{TH}	0		V_{DD}	V	
PTH input voltage	V_{IPTH}	0		V_{DD}	V	
Comparator consumption current	I_{COMP}		1		mA	Set PTHM7 to 1

DC Characteristics

T_A = −40 to +60°C; V_{DD} = 2.7 to 5.0 V; refer to figure 2

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except ports 0, 1, 12-14, TI0, TI1, $\overline{RESET}$, X1, X2
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	Ports 0, 1, TI0, TI1 and $\overline{RESET}$
	V_{IH3}	0.7 V_{DD}		V_{DD}	V	Ports 12-14; built-in pullup resistor
		0.7 V_{DD}		10	V	Ports 12-14; open drain
	V_{IH4}	V_{DD} − 0.5		V_{DD}	V	X1, X2
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	Except ports 0, 1, TI0, TI1, $\overline{RESET}$, X1, X2
	V_{IL2}	0		0.2 V_{DD}	V	Ports 0, 1, TI0, TI1 and $\overline{RESET}$
	V_{IL3}	0		0.4	V	X1, X2
High-level output voltage	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 4.5 to 5.0 V; I_{OH} = −1 mA
		V_{DD} − 0.5			V	V_{DD} = 2.7 to 5.0 V; I_{OH} = −100 μA
Low-level output voltage	V_{OL}		0.35	2.0	V	Ports 0, 2-9; V_{DD} = 4.5 to 5.0 V; I_{OL} = 15 mA
			0.35	2.0	V	Ports 12-14; V_{DD} = 4.5 to 5.0 V; I_{OL} = 10 mA
				0.4	V	V_{DD} = 4.5 to 5.0 V; I_{OL} = 1.6 mA
				0.5	V	I_{OL} = 400 μA
High-level input leakage current	I_{LIH1}			3	μA	All except X1, X2, and ports 12-14; V_{IN} = V_{DD}
	I_{LIH2}			20	μA	X1, X2; V_{IN} = V_{DD}
	I_{LIH3}			20	μA	Ports 12-14 (with open drain); V_{IN} = 10 V
Low-level input leakage current	I_{LIL1}			−3	μA	All except X1, X2; V_{IN} = 0 V
	I_{LIL2}			−20	μA	X1, X2; V_{IN} = 0 V
High-level output leakage current	I_{LOH1}			3	μA	Other than ports 12-14; V_{OUT} = V_{DD}
	I_{LOH2}			20	μA	Ports 12-14 (open drain); V_{OUT} = 10 V
Low-level output leakage current	I_{LOL}			−3	μA	V_{OUT} = 0 V
Internal pullup resistor	R_L	15	40	70	kΩ	Ports 12-14; V_{DD} = 4.5 to 5.0 V
		10		80	kΩ	Ports 12-14
Supply current (Note 1)	I_{DD1}		3	9	mA	V_{DD} = 4.5 to 5.0 V (Notes 2, 3)
			0.55	1.5	mA	V_{DD} = 3 V ± 10% (Notes 3, 4)
	I_{DD2}		600	1800	μA	HALT mode; V_{DD} = 4.5 to 5.0 V
			200	600	μA	HALT mode; V_{DD} = 3 V ± 10% (Note 3)
	I_{DD3}		0.1	10	μA	STOP mode; V_{DD} = 3 V ± 10%

Notes:

(1) Does not include pullup resistor current and comparator current.

(2) When operated in the high-speed mode with the processor clock control register (PCC) set to 0011.

(3) f_{XX} = 4.19 MHz; C1 = C2 = 22 pF.

(4) When operated in the low-speed mode with the PCC set to 0000.

Figure 2. DC Characteristics

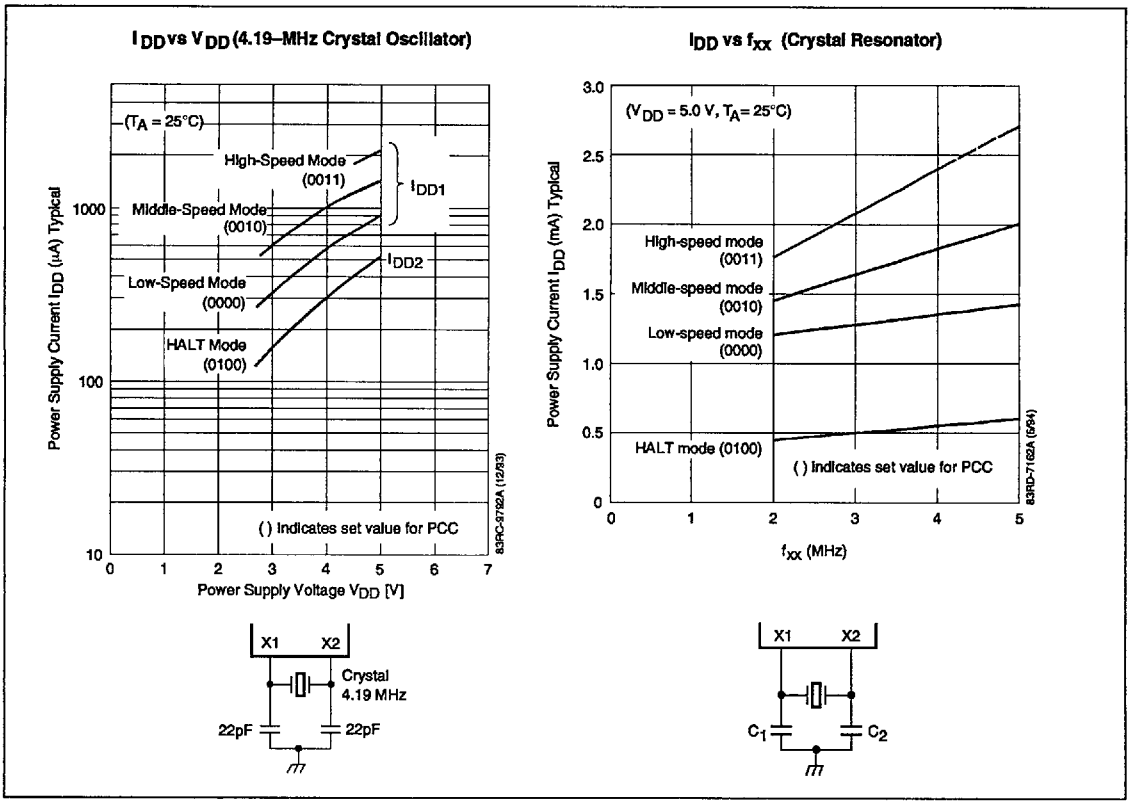


Figure 2. DC Characteristics (cont)

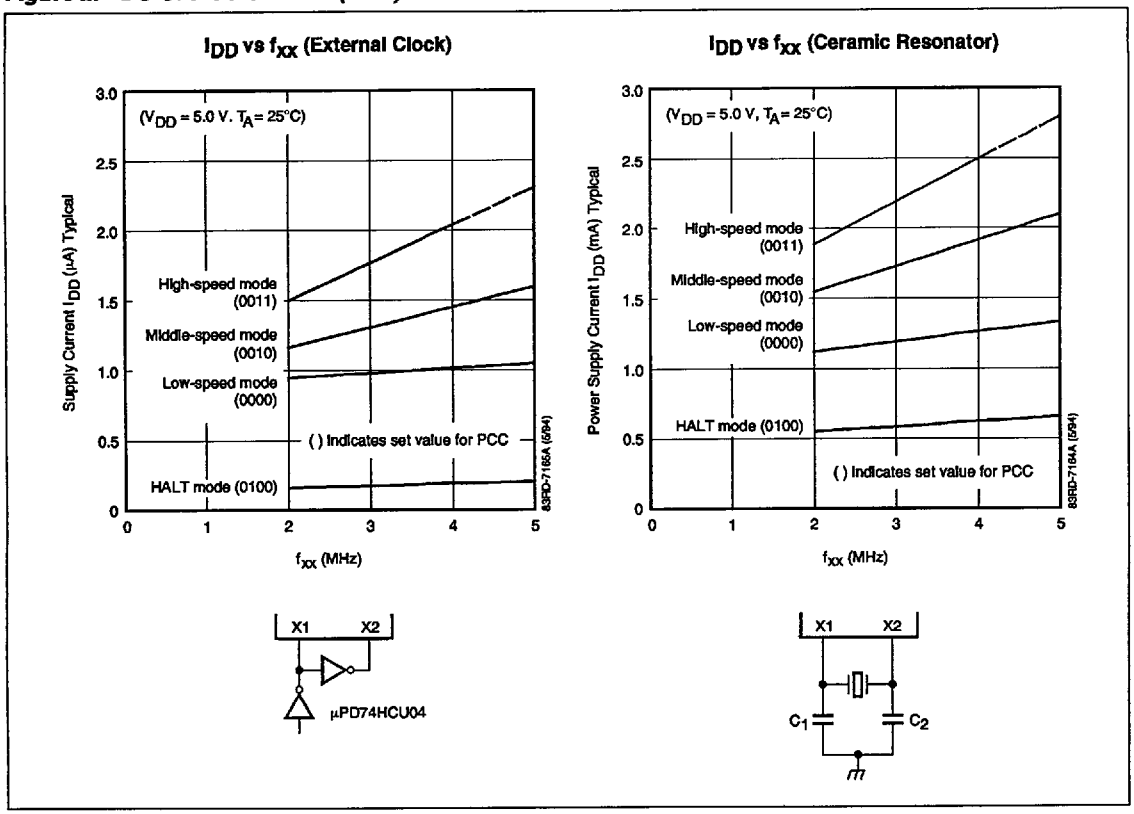
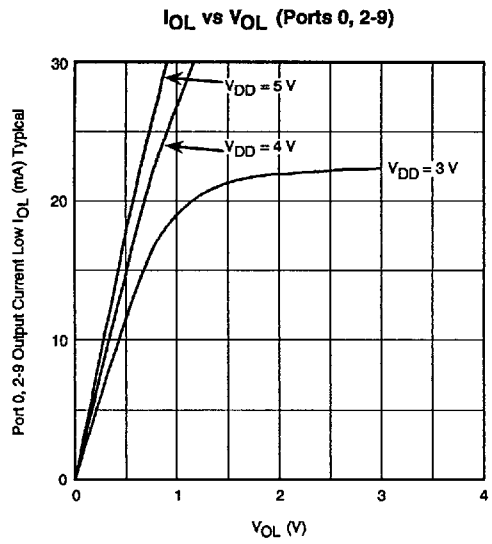
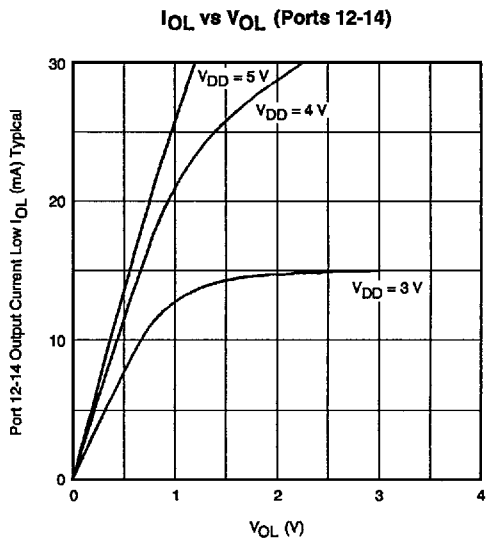
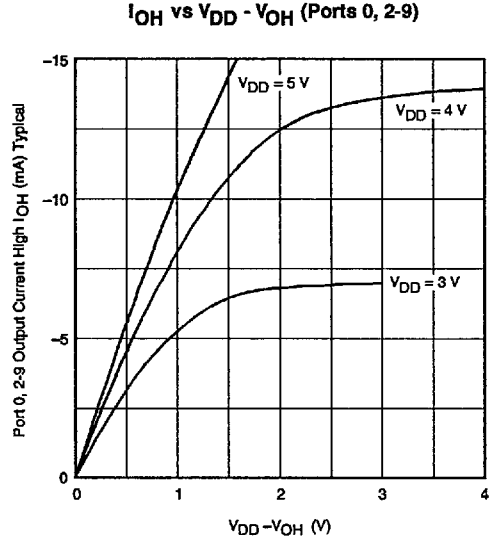


Figure 2. DC Characteristics (cont)







83YL-9788B (12/93)

AC Characteristics

T_A = −40 to +60°C; V_{DD} = 2.7 to 5.0 V; refer to figures 3 through 10

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Cycle time *	t_{CY}	0.95		32	μs	V_{DD} = 4.5 to 5.0 V
		1.91		32	μs	V_{DD} = 2.7 to 5.0 V
TI0, TI1 input frequency	f_{TI}	0		1	MHz	V_{DD} = 4.5 to 5.0 V
		0		275	kHz	V_{DD} = 2.7 to 5.0 V
TI0, TI1 input high- and low-level width	t_{TIH}, t_{TIL}	0.48			μs	V_{DD} = 4.5 to 5.0 V
		1.8			μs	V_{DD} = 2.7 to 5.0 V
$\overline{SCK}$ cycle time	t_{KCY}	0.8			μs	Input; V_{DD} = 4.5 to 5.0 V
		0.95			μs	Output; V_{DD} = 4.5 to 5.0 V
		3.2			μs	Input; V_{DD} = 2.7 to 5.0 V
		3.8			μs	Output; V_{DD} = 2.7 to 5.0 V
$\overline{SCK}$ high and low level width	t_{KH}, t_{KL}	0.4			μs	Input; V_{DD} = 4.5 to 5.0 V
		$0.5\ t_{KCY} - 50$			ns	Output; V_{DD} = 4.5 to 5.0 V
		1.6			μs	Input; V_{DD} = 2.7 to 5.0 V
		$0.5\ t_{KCY} - 150$			ns	Output; V_{DD} = 2.7 to 5.0 V
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	100			ns	
SI hold time from $\overline{SCK}$ ↑	t_{KSI}	400			ns	
$\overline{SCK}$ ↓ to SO output delay time	t_{KSO}			300	ns	V_{DD} = 4.5 to 5.0 V
				1000	ns	V_{DD} = 2.7 to 5.0 V
INT0-INT4 high- and low-level width	t_{INTH}, t_{INTL}	5			μs	
$\overline{RESET}$ low-level width	t_{RSL}	5			μs	

* Cycle time (minimum instruction execution time) is determined by the frequency of the oscillator connected to the microcontroller and the processor clock control (PCC) register. See figure 3.

Figure 3. Main System Clock Operation; t_{CY} vs V_{DD}

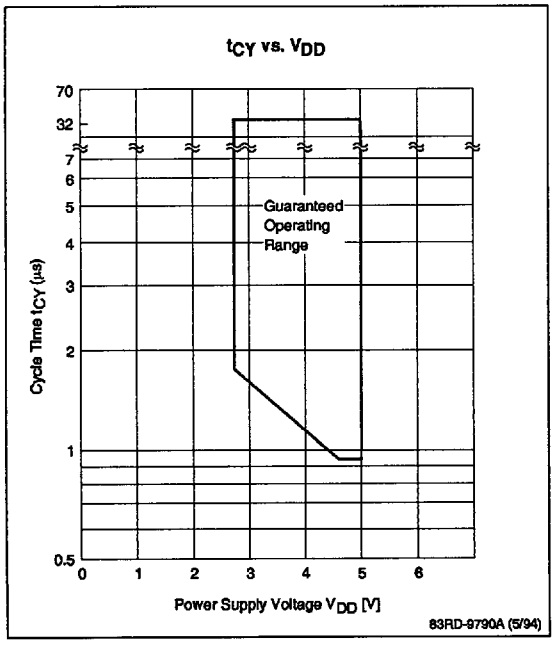


Figure 4. AC Timing Measurement Points (except Ports 0, 1, TI0, TI1, X1, X2, and $\overline{RESET}$)

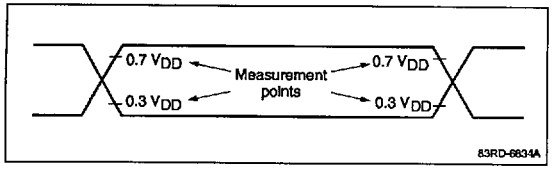


Figure 5. Clock Timing Measurement Points

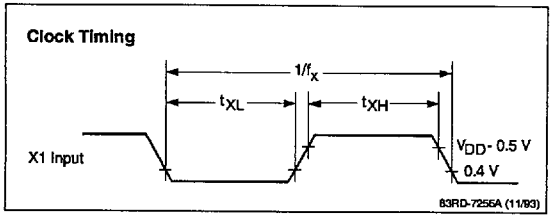


Figure 6. TI Timing

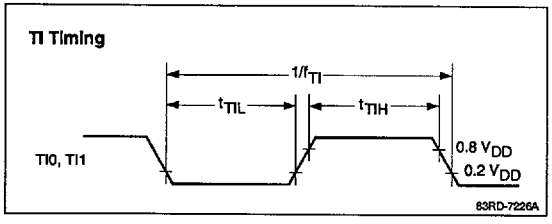


Figure 7. Serial Transfer Timing

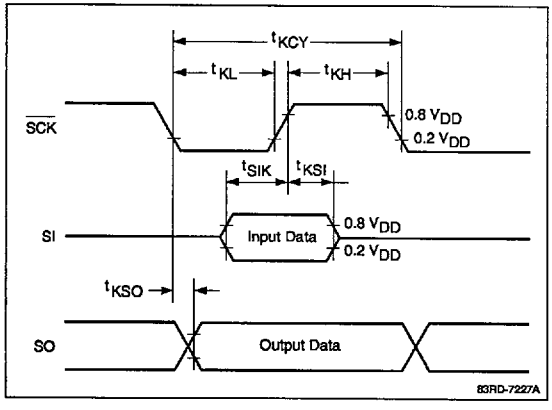


Figure 8. Interrupt Input Timing

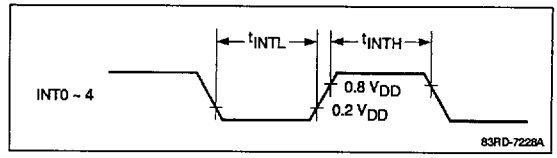


Figure 9. $\overline{RESET}$ Input Timing

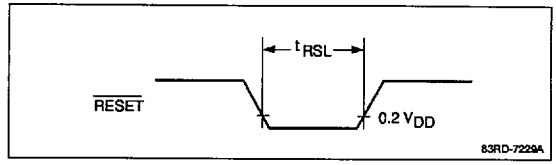
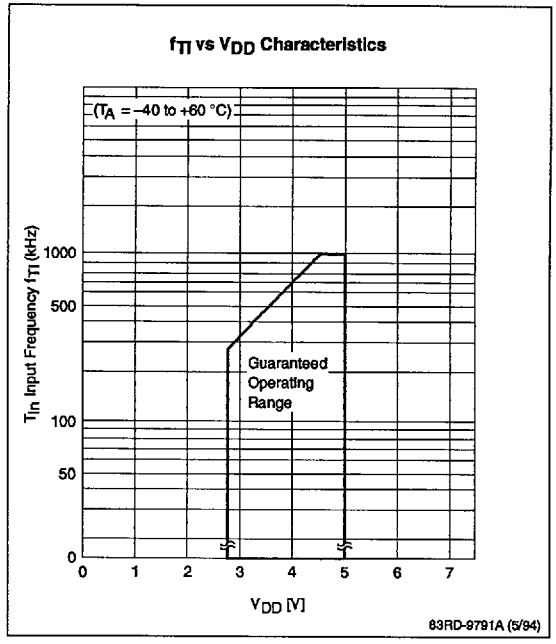


Figure 10. Main System Clock Operation; f_{TI} vs V_{DD}



Data Memory STOP Mode; Low Voltage Data Retention Characteristics

T_A = −40 to +60°C; refer to figure 11

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.0		5.0	V	
Data retention current (Note 1)	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2.0 V
Release signal set time	t_{SREL}	0			μs	
Oscillation stabilization time (Note 2)	t_{WAIT}		$2^{17}/f_{XX}$		s	Release by $\overline{\text{RESET}}$ input
			(Note 3)		ms	Release by interrupt request

Notes:

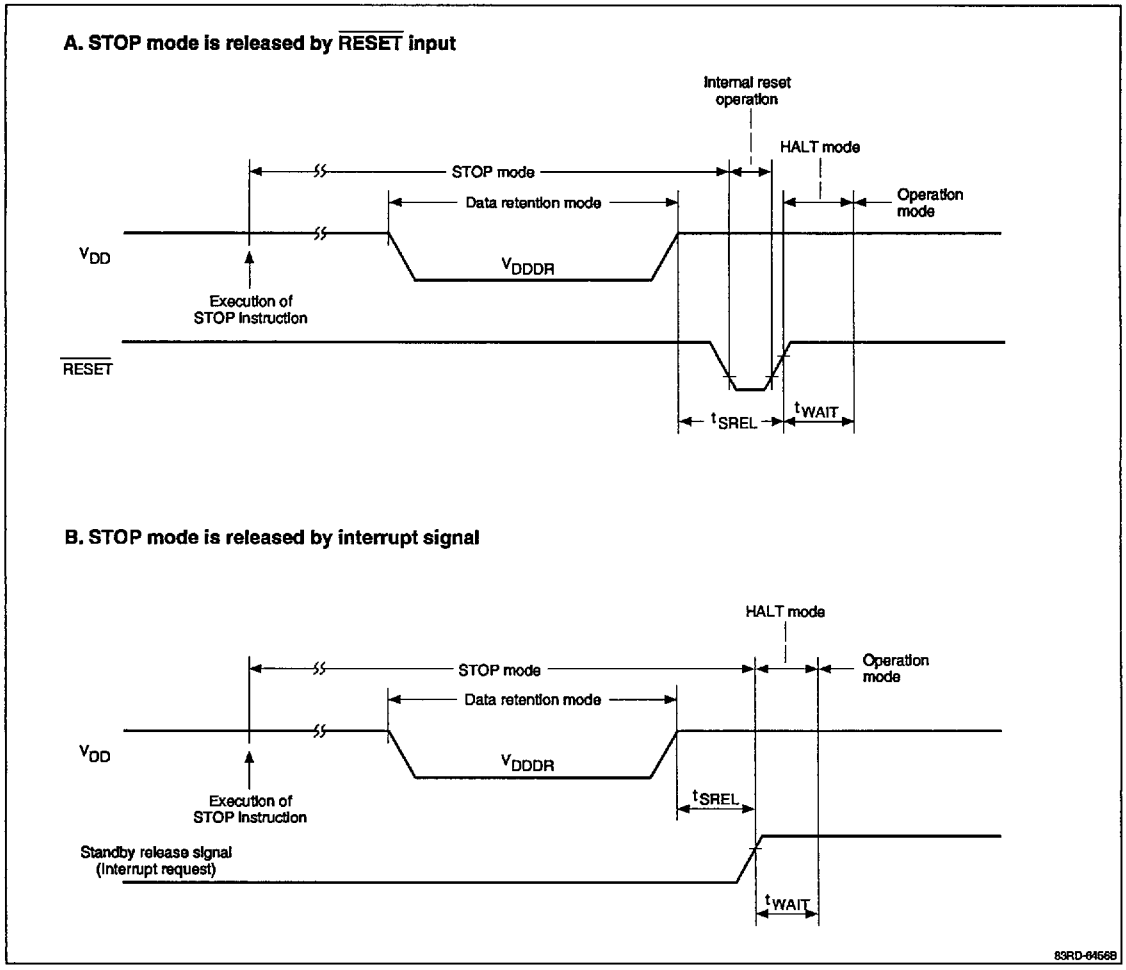
(1) Excludes current in the pullup resistors and comparator.

(2) Consult the manufacturer's resonator or crystal spec sheet for this value.

(3) Oscillation stabilization WAIT time is the time during which the CPU is stopped and the crystal is stabilizing. This time is required to prevent unstable operation while the oscillation is started. The interval timer can be used to delay the CPU from executing instructions using the the basic interval timer mode register (BTM) according to the following table:

BTM3	BTM2	BTM1	BTM0	WAIT time (f_{XX} = 4.19 MHz)
—	0	0	0	$2^{20}/f_{XX}$ (Approx 250 ms)
—	0	1	1	$2^{17}/f_{XX}$ (Approx 31.3 ms)
—	1	0	1	$2^{15}/f_{XX}$ (Approx 7.82 ms)
—	1	1	1	$2^{13}/f_{XX}$ (Approx 1.95 ms)

Figure 11. Data Retention Timing



SOLDERING

Packaging and Soldering Information

Part Number	Package	Package Drawing No.	Recommended Soldering Code
μPD751xxFGF	64-pin plastic QFP	P64GF-100-3B8, 3BE-1	IR30-00-1, VP15-00-1, WS60-00-1

Soldering Conditions

Method (Note 1)	Code (Note 2)	Soldering Conditions	Exposure Limit (Note 3)
Infrared reflow	IR30-00-1	Package peak temp: 230°C Time: 30 sec max (210°C min)	No limit
Vapor phase	VP15-00-1	Package peak temp: 215°C Time: 40 sec max (200°C min)	No limit
Wave soldering	WS60-00-1	Solder bath temp: 260°C max Time: 10 sec max Preheating temp: 120°C max (package surface temp)	No limit
Pin partial heating (QFP)		Temperature: 300°C max Time: 3 sec max (per device side)	No limit

Notes:

(1) Do not use different soldering methods together. However, on all devices the pin partial heating soldering method can be used alone or in combination with other soldering methods.

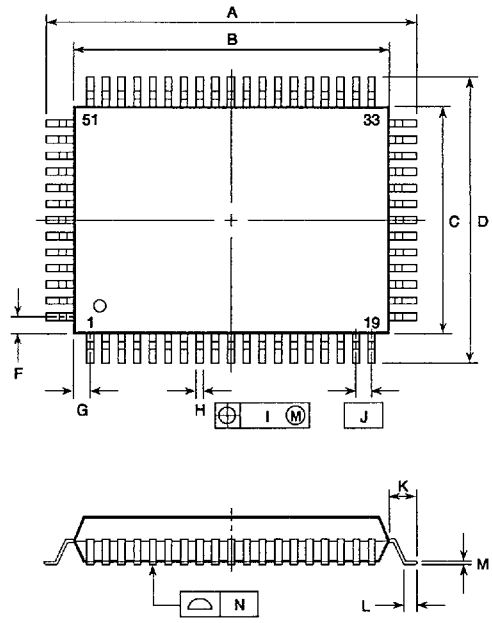
(2) The maximum number of soldering operations is one or two as indicated by the last digit of the soldering code: –1 or –2.

(3) Exposure limit means number of days after unpacking the dry pack. Storage conditions are 25°C and 65% RH minimum. Thereafter, baking the devices is required before soldering.

PACKAGE DRAWINGS

64-Pin Plastic QFP (2.7 mm thick)

Item	Millimeters	Inches
A	23.6 ± 0.4	.929 ± .016
B	20.0 ± 0.2	.795 $^{+.009}_{-.008}$
C	14.0 ± 0.2	.551 $^{+.009}_{-.008}$
D	17.6 ± 0.4	.693 ± .016
F	1.0	.039
G	1.0	.039
H	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
I	0.20	.008
J	1.0 (TP)	.039 (TP)
K	1.8 ± 0.2	.071 $^{+.008}_{-.009}$
L	0.8 ± 0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.15	.006
P	2.7	.106
Q	0.1 ± 0.1	.004 ± .004
R	0.1 ± 0.1	.004 ± .004
S	3.0 max	.119 max



P64GF-100-3B8, 3BE-1

49NR-599B (6/91)

64-Pin Ceramic QFP for Engineering Samples

Item	Millimeters	Inches
A	14.20	.559
B	12.0	.472
C	18.0	.708
D	20.0	.787
H	0.40	.016
J	1.0	.039
N	0.15	.006
S	2.25	.089

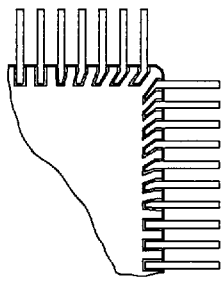
Notes:

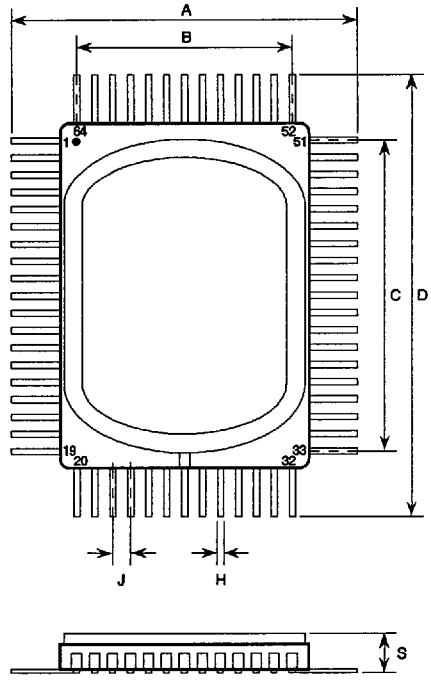
(1) The metal cover is connected to pin 26 (V_{SS}).

(2) The leads on the bottom surface are formed obliquely.

(3) The length of the leads is not defined since the cutting of the lead tips is not controlled during the manufacturing process.

Enlarged detail of bottom





83YL-9269B (6/94)