

40-CHANNEL SEGMENT/COMMON DRIVER FOR DOT MATRIX LCD

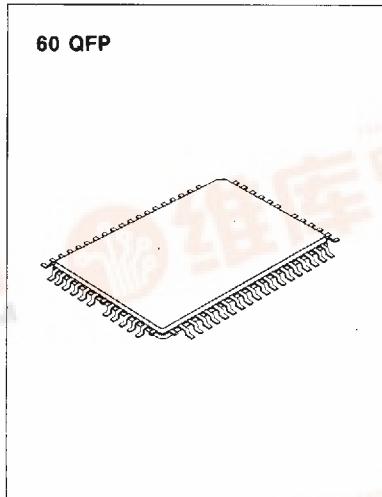
The KS0065B is a LCD driver LSI which is fabricated by low power CMOS technology. Basically this LSI consists of 20 x 2bit bidirectional shift register, 20 x 2bit data latch ad 20 x 2 bit driver. (refer to Fig 1) This LSI can be used a common or segment driver.

FUNCTION

- Dot matrix LCD driver with 40 channel output.
 - Selectable function to use common/segment drivers simultaneously.
 - Input/Output signal
 - output; 20 x 2 channel waveform for LCD driving
 - input ; - Serial display data and control pulse from the controller LSI.
 - Bias voltage (V_1-V_5)

FEATURES

- Display driving bias; static-1/5
 - Power supply voltage; $+5V \pm 10\%$
 - Supply voltage for display: $0\sim -5V(V_{EE})$
 - interface



2

driver (cascade connection)	controller
Other KS0065B, KS0063	KS0066

- CMOS Process
 - 60QFP and bare chip available

BLOCK DIAGRAM

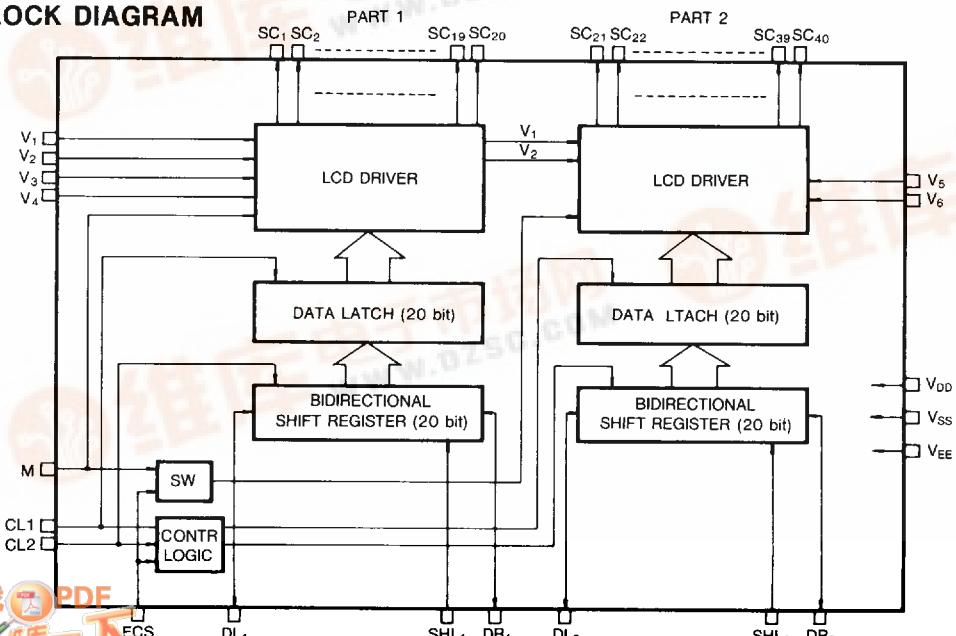


Fig. 1. KS0065B functional block diagram.

PIN CONFIGURATION

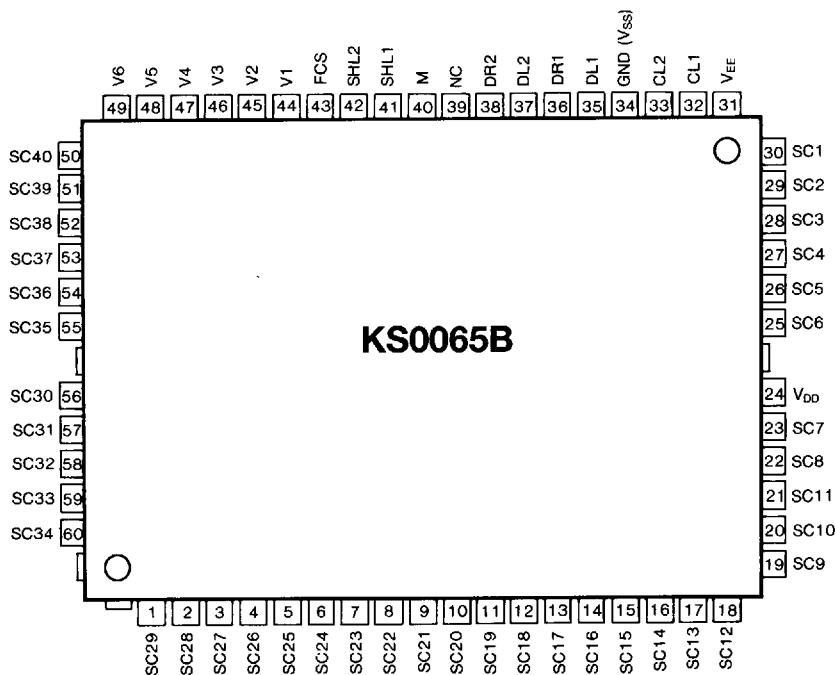


Fig. 2. 60 QFP Top View

PIN(No.)	INPUT/OUTPUT	NAME	DESCRIPTION	INTERFACE															
V _{DD} (24)		Power Supply	For logical circuit (+5V±10%)	Power Supply															
GND(34)			0V (GND)																
V _{EE} (31)			For LCD driver circuit (-5V)																
V ₁ V ₂ (44, 45)	Input	Bias Vtg	Bias voltage level for LCD drive (select level)	power															
SC ₁ ~SC ₂₀	Output	LCD driver	LCD driver output	LCD															
V ₃ V ₄ (46, 47)	Input	Bias Vtg	Bias voltage level for LCD drive (nonselect level)	power															
SHL1 (41)	Input	Data interface	Selection of the shift direction of Part 1 shift register	V _{DD} or V _{SS}															
DL1, DR1 (35, 36)	Input Output		<table border="1"> <tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr> <tr><td>V_{DD}</td><td>out</td><td>in</td></tr> <tr><td>V_{SS}</td><td>in</td><td>out</td></tr> </table>		SHL1	DL1	DR1	V _{DD}	out	in	V _{SS}	in	out						
SHL1	DL1	DR1																	
V _{DD}	out	in																	
V _{SS}	in	out																	
SC ₂₁ ~SC ₄₀	Output	LCD driver	LCD driver output	LCD															
V ₅ V ₆ (48, 49)	Input	Part 2	Bias Vtg	power															
SHL2 (42)	Input		Selection of the shift direction of Part 2 shift register																
DL2, DR2 (37, 38)	Input Output	Data Interface	Data input/output of Part 1 shift register	Controller or KS0065B															
M (40)	Input		Data input/output of Part 2 shift register																
CL1, CL2 (32, 33)	Input	Alternated signal for LCD driver output	<table border="1"> <tr><th>PART</th><th>FCS</th><th>CL1</th><th>CL2</th><th>M polarity</th></tr> <tr><td>1</td><td>V_{SS} V_{DD}</td><td>latch clock (\overline{U})</td><td>shift clock (\overline{U})</td><td>M</td></tr> <tr><td>2</td><td>V_{SS} V_{DD}</td><td>shift clock (U)</td><td>latch clock (U)</td><td>\overline{M}</td></tr> </table>	PART	FCS	CL1	CL2	M polarity	1	V _{SS} V _{DD}	latch clock (\overline{U})	shift clock (\overline{U})	M	2	V _{SS} V _{DD}	shift clock (U)	latch clock (U)	\overline{M}	Controller or KS0065B Controller
PART	FCS	CL1	CL2	M polarity															
1	V _{SS} V _{DD}	latch clock (\overline{U})	shift clock (\overline{U})	M															
2	V _{SS} V _{DD}	shift clock (U)	latch clock (U)	\overline{M}															
FCS(43)	Input	Shift/latch clock of display data and polarity of M signal are changed by FCS signal. By setting FCS to V _{DD} level, user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously.																	
NC (39)			No connection pin	N.C															

MAXIMUM ABSOLUTE LIMIT ($T_a=25^\circ\text{C}$)

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	$-0.3 \sim +7.0$	V
Driver supply voltage	V_{LCD}	$V_{DD}-13.5 \sim V_{DD}+0.3$	V
Input voltage 1	V_{IN1}	$-0.3 \sim V_{DD}+0.3$	V
Input voltage 2 (V_1-V_6)	V_{IN2}	$V_{DD}+0.3 \sim V_{EE}-0.3$	V
Operating temperature	T_{opr}	$-20 \sim +75$	$^\circ\text{C}$
Storage temperature	T_{stg}	$-55 \sim +125$	$^\circ\text{C}$

* Voltage greater than above may damage to the circuit

* V_{EE} : connect a protection resistor ($220\Omega \pm 5\%$)**ELECTRICAL CHARACTERISTICS****DC characteristics** ($V_{DD}=+5V \pm 10\%$, $V_{EE}=-5V \pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ\text{C}$)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin	
Supply current *	I_{DD}	$f_{CL2}=400\text{KHz}$	—	1	mA	—	
	I_{EE}	$f_{CL1}=1\text{kHz}$	—	10	μA		
Input voltage	V_{IH}	—	0.7 V_{DD}	V_{DD}	V	CL1, CL2, DL1, DL2 DR1, DR2, SHL1, SHL2, M, FCS	
	V_{IL}		0	0.3 V_{DD}			
Input leakage current	I_{IL}	$V_{IN}=0\text{-}V_{DD}$	-5	5	μA	DL1, DL2, DR1, DR2	
Output Voltage	V_{OH}	$I_{OH}=-0.4\text{mA}$	$V_{DD}-0.4$	—	V		
	V_{OL}	$I_{OL}=+0.4\text{mA}$	—	0.4	V(V_1-V_6)-SC(SC1-SC40)		
Voltage descending	V_{d1}	$I_{ON}=0.1\text{mA}$ for one of SC1-SC40	—	1.1			
	V_{d2}	$I_{ON}=0.05\text{mA}$ for each SC1-SC40	—	1.5			
Leakage current	I_{v1}	$V_{IN}=V_{DD}\sim V_{EE}$ (Output SC1-SC40: floating)	-10	10	μA	V_1-V_6	

AC CHARACTERISTICS ($V_{DD}=+5V \pm 10\%$, $V_{EE}=-5V \pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ\text{C}$)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data shift frequency	f_{CL}	—	—	400	KHz	CL2
Clock high level width	t_{CWH}	—	800	—	ns	CL1, CL2
Clock low level width	t_{CWL}	—	800	—		CL2
Clock set-up time	t_{SL}	from CL2 to CL1	500	—		CL1, CL2
	t_{LS}	from CL1 to CL2	500	—		
Clock rise/fall time	t_{CTR}	—	—	200		DL1, DL2, DR1, DR2, FLM
Data set-up time	t_{TSU}	—	300	—		
Data hold time	t_{DH}	—	300	—		
Data delay time	t_{PD}	$CL=15\text{pF}$	—	500		DL1, DL2, DR1, DR2

* Input/output current is excluded; When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at "H" or "L".

TIMING CHARACTERISTICS

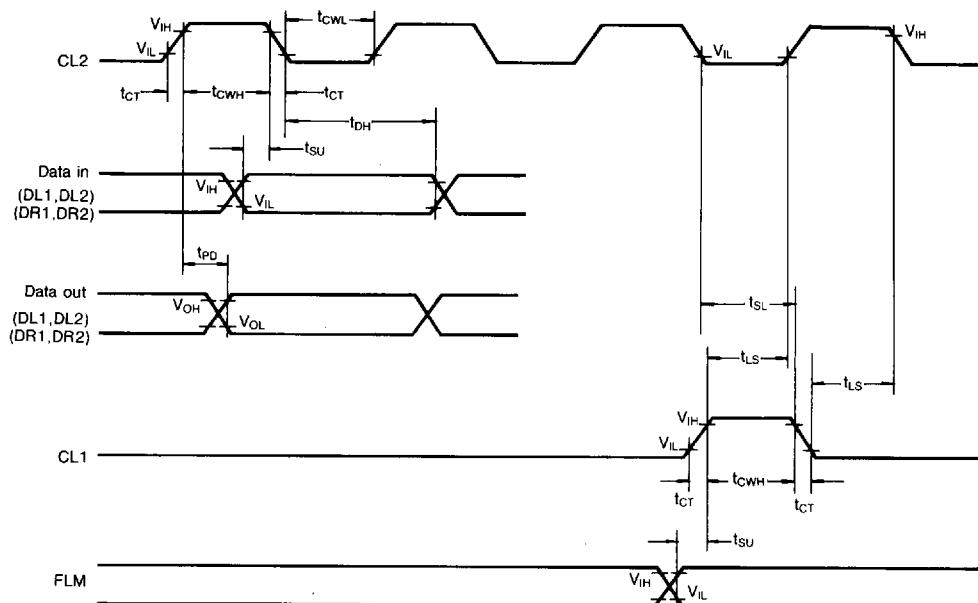


Fig. 3. AC characteristics

FUNCTIONAL DESCRIPTION

1) To drive segment type

When the FCS is connected to V_{ss}, KS0065B(SC1-SC40) is operated as segment driver.(refer to fig 4)

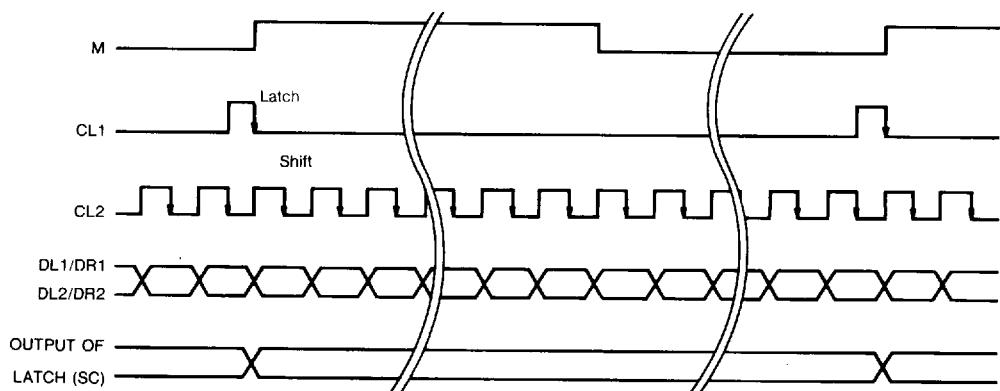


Fig. 4. Segment Data Waveforms

2) To drive common type

When the FCS is connected to VDD, only part2(SC21-SC40) of KS0065B is operated as common driver.(refer to Fig 5).

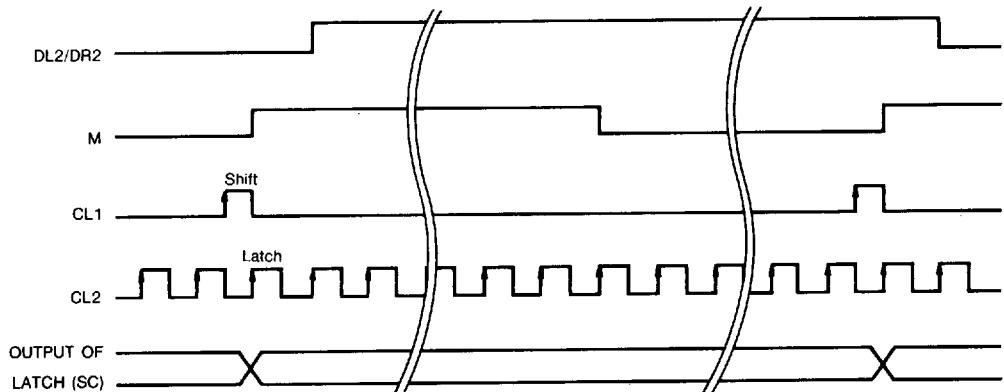


Fig. 5. Common Data Waveforms

LCD OUTPUT WAVEFORMS

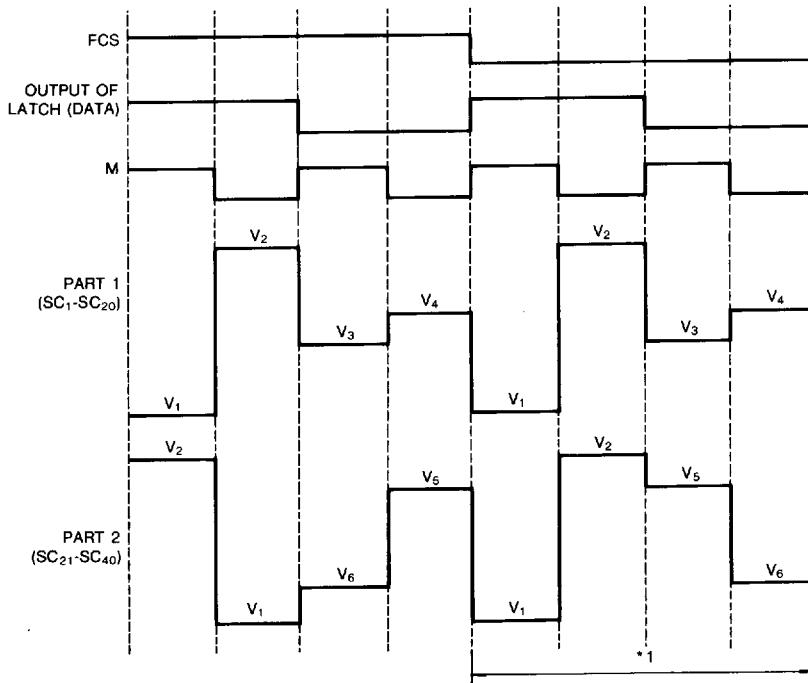
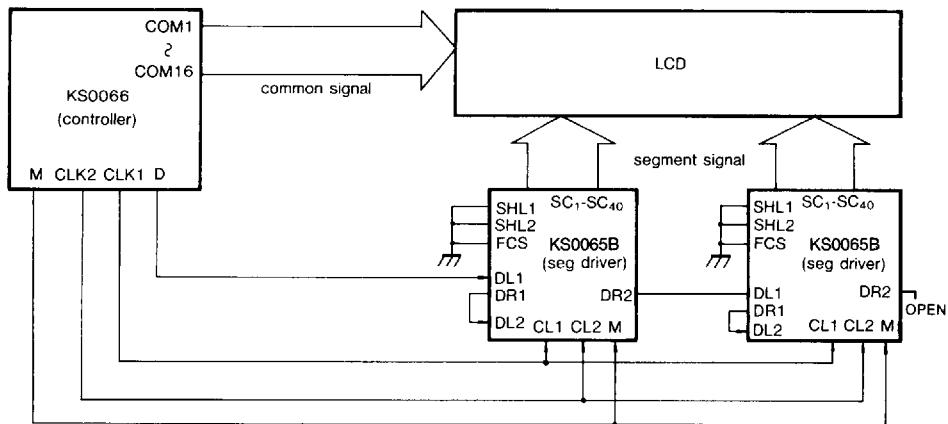


Fig. 6. Output waveform

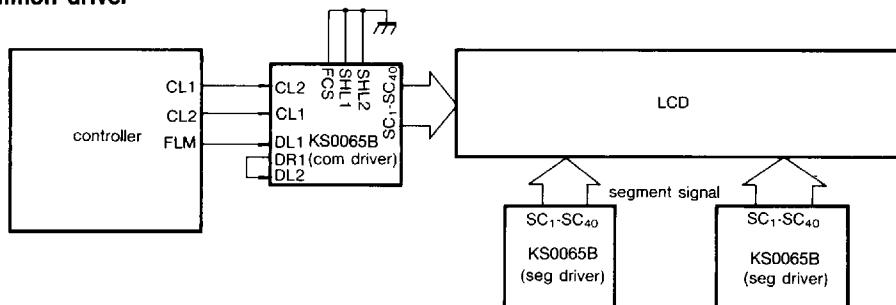
*1: To use for same function of part 1 and part 2, V3 and V5, V4 and V6 of power supply for LCD driver are short circuited respectively.

APPLICATION CIRCUIT

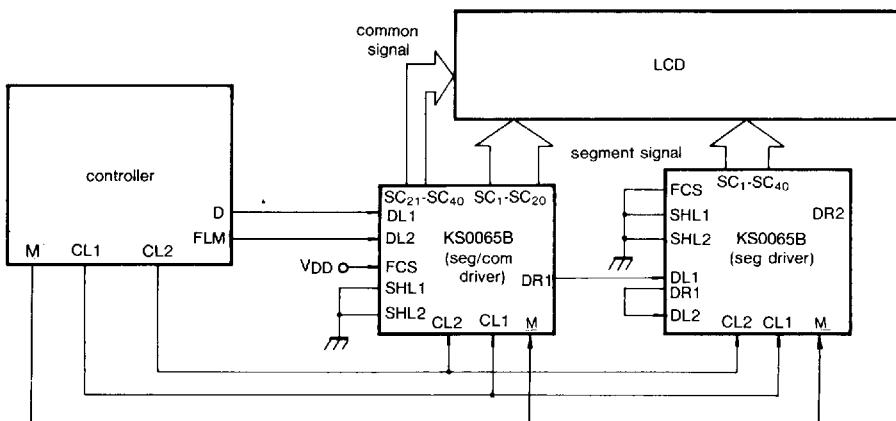
1) Segment driver



2) Common driver



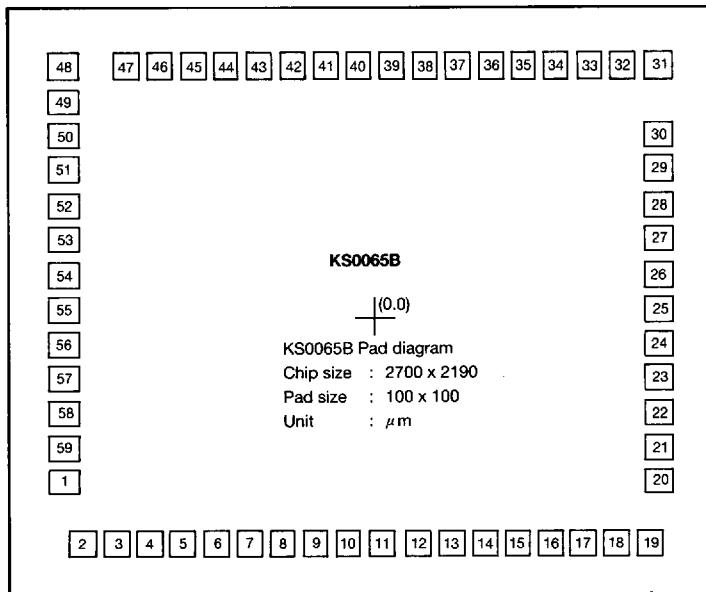
3) Segment/common driver



KS0065B

CMOS DIGITAL INTEGRATED CIRCUIT

PAD DIAGRAM



KS0065B**CMOS DIGITAL INTEGRATED CIRCUIT****PAD LOCATION**

UNIT [um]

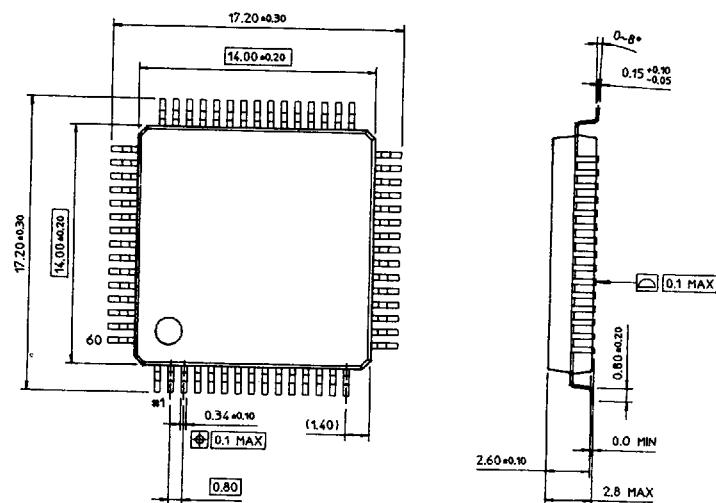
PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE	
		X	Y			X	Y
1	V _{EE}	-1120.2	-642.5	31	SC ₂₈	1117.5	865.2
2	CL ₁	-1062.5	-865.2	32	SC ₂₇	992.5	865.2
3	CL ₂	-937.5	-865.2	33	SC ₂₆	867.5	865.2
4	V _{SS}	-812.5	-865.2	34	SC ₂₅	742.5	865.2
5	DL ₁	-687.5	-865.2	35	SC ₂₄	617.5	865.2
6	DR ₁	-562.5	-865.2	36	SC ₂₃	492.5	865.2
7	DL ₂	-437.5	-865.2	37	SC ₂₂	367.5	865.2
8	DR ₂	-312.5	-865.2	38	SC ₂₁	242.5	865.2
9	M	-187.5	-642.5	39	SC ₂₀	117.5	865.2
10	SHL ₁	-62.5	-865.2	40	SC ₁₉	-7.5	865.2
11	SHL ₂	62.5	-865.2	41	SC ₁₈	-132.5	865.2
12	FCS	187.5	-865.2	42	SC ₁₇	-257.5	865.2
13	V ₁	332.5	-865.2	43	SC ₁₆	-382.5	865.2
14	V ₂	457.5	-865.2	44	SC ₁₅	-507.5	865.2
15	V ₃	582.5	-865.2	45	SC ₁₄	-632.5	865.2
16	V ₄	707.5	-865.2	46	SC ₁₃	-757.5	865.2
17	V ₅	832.5	-865.2	47	SC ₁₂	-882.5	865.2
18	V ₆	957.5	-865.2	48	SC ₉	-1120.2	857.5
19	SC ₄₀	1082.5	-865.2	49	SC ₁₀	-1120.2	732.5
20	SC ₃₉	1120.2	-627.5	50	SC ₁₁	-1120.2	607.5
21	SC ₃₈	1120.2	-502.5	51	SC ₈	-1120.2	482.5
22	SC ₃₇	1120.2	-377.5	52	SC ₇	-1120.2	357.5
23	SC ₃₆	1120.2	-252.5	53	V _{DD}	-1120.2	232.5
24	SC ₃₅	1120.2	-127.5	54	SC ₆	-1120.2	107.5
25	SC ₃₀	1120.2	-2.5	55	SC ₅	-1120.2	-17.5
26	SC ₃₁	1120.2	122.5	56	SC ₄	-1120.2	-142.5
27	SC ₃₂	1120.2	247.5	57	SC ₃	-1120.2	-267.5
28	SC ₃₃	1120.2	372.5	58	SC ₂	-1120.2	-392.5
29	SC ₃₄	1120.2	497.5	59	SC ₁	-1120.2	-517.5
30	SC ₂₉	1120.2	622.5				

Note : (0.0) is center in the chip

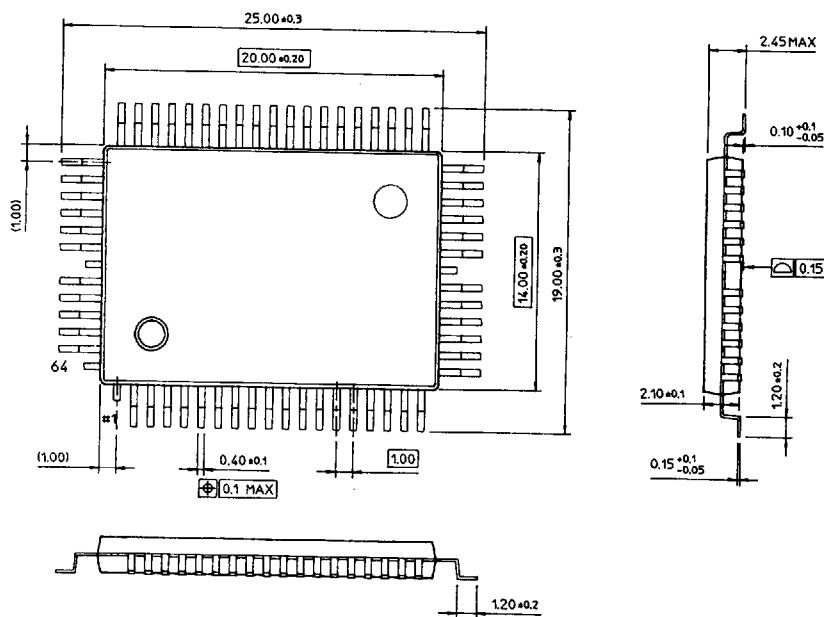
PACKAGE DIMENSIONS

Dimensions in Millimeters

60-QFP-1414A

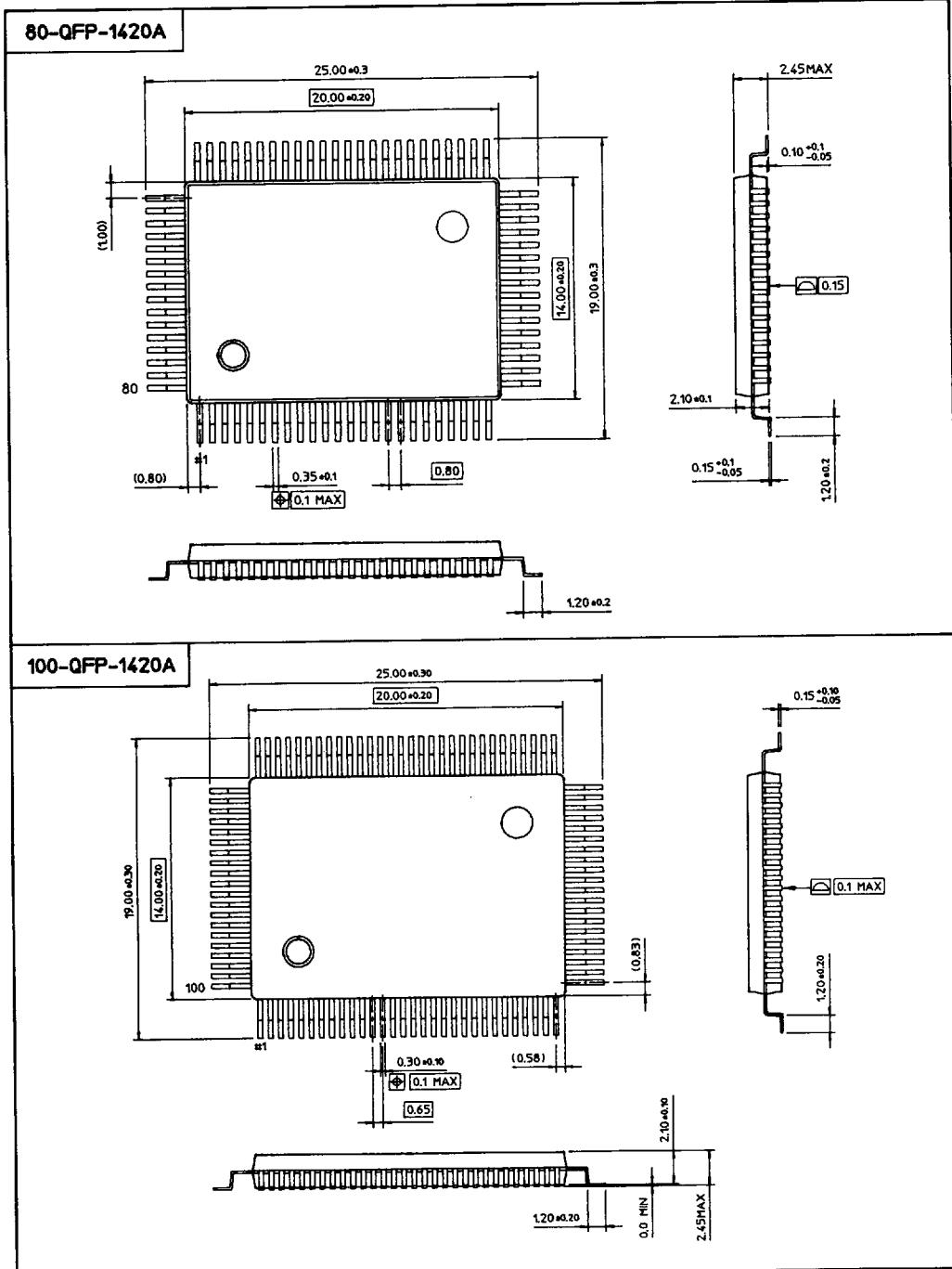


64-QFP-1420D



PACKAGE DIMENSIONS

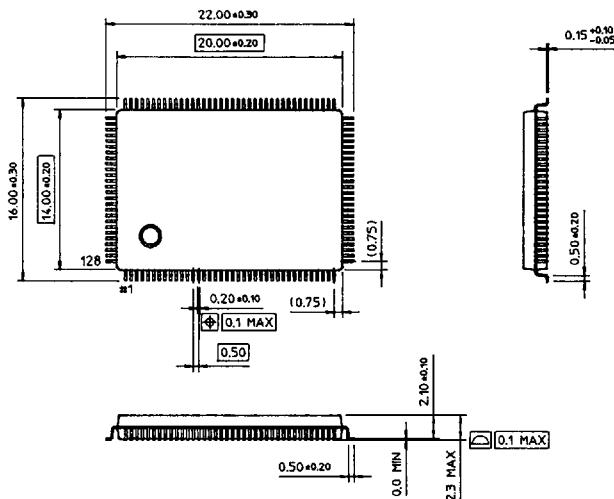
Dimensions in Millimeters



PACKAGE DIMENSIONS

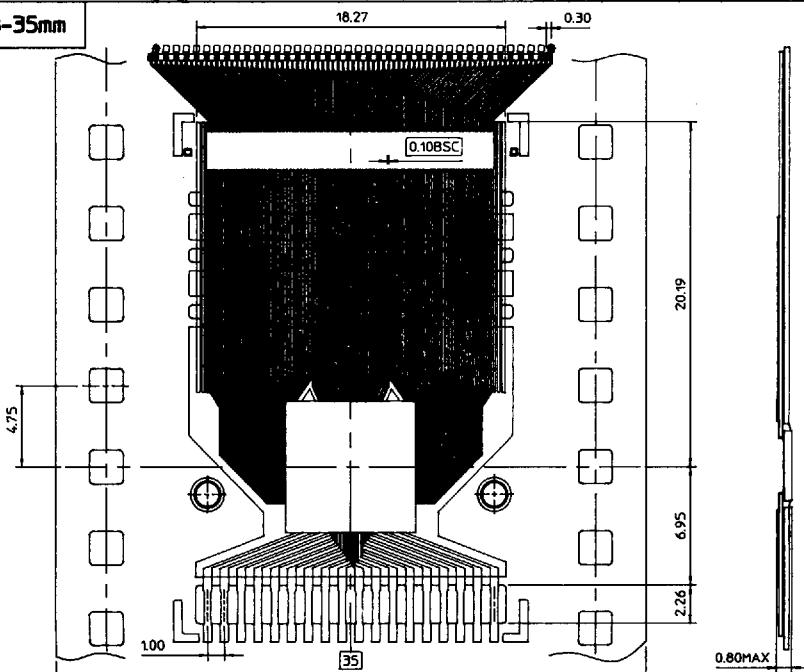
Dimensions in Millimeters

128-QFP-1420



3

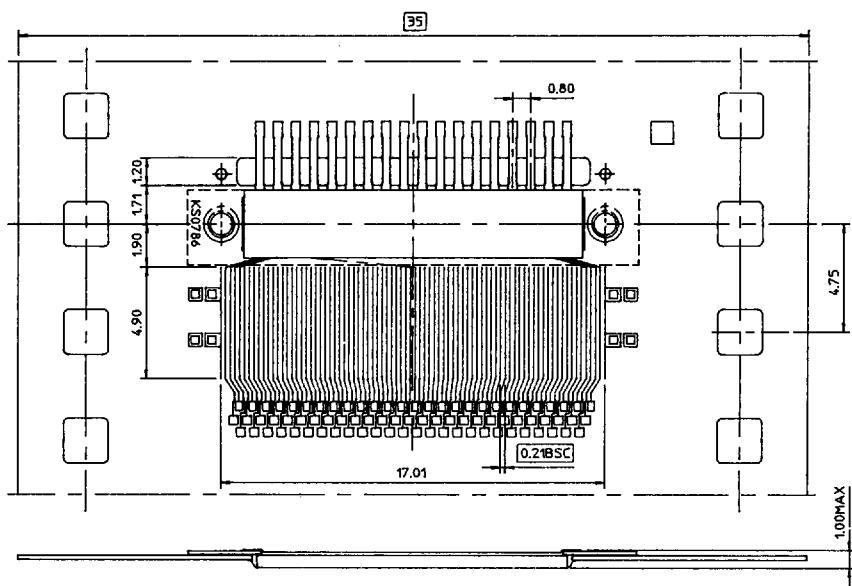
98-TAB-35mm



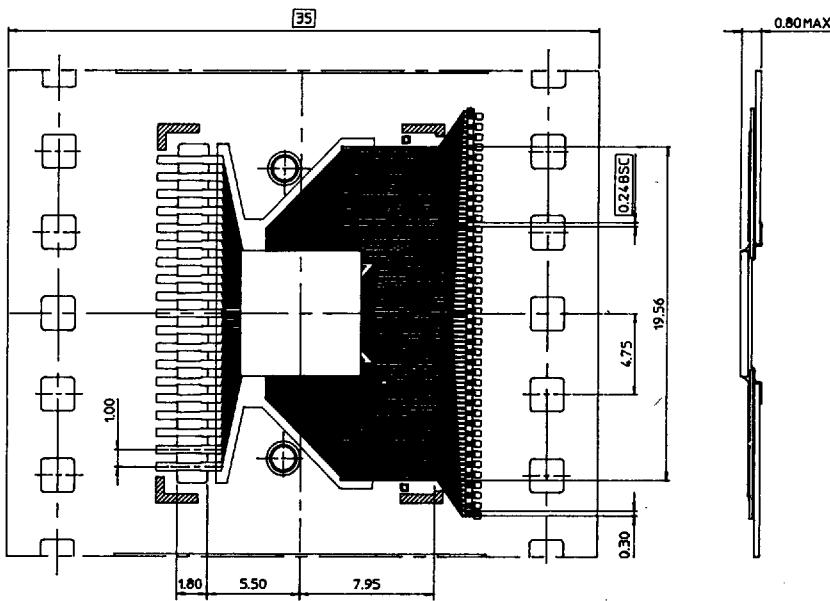
PACKAGE DIMENSIONS

Dimensions in Millimeters

98-STAB-35mm



99-TAB-35mm



PACKAGE DIMENSIONS

Dimensions in Millimeters

