Spartan-IIE 1.8V FPGA Automotive IQ Product Family: Introduction and Ordering

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Product Specification

Introduction

The Spartan™-IIE 1.8V Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in Table 1. System performance is supported beyond 200 MHz.

Spartan-IIE devices deliver more gates, I/Os, and features per dollar than other FPGAs by combining advanced process technology with a streamlined architecture based on the proven Virtex™-E platform. Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Guaranteed to meet full electrical specifications over T_J = –40°C to +125°C
- Second generation ASIC replacement technology
  - Densities as high as 15,552 logic cells with up to 600,000 system gates
  - Streamlined features based on Virtex-E architecture
  - Unlimited in-system reprogrammability
  - Very low cost
- System level features
  - SelectRAM+™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K-bit true dual-port block RAM
    - Fast interfaces to external RAM
  - Low-power segmented routing architecture
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
    - Eliminate clock distribution delay
    - Multiply, divide, or phase shift
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Low cost packages available in all densities
  - Family footprint compatibility in common packages
  - 19 high-performance interface standards
    - LVTTL, LVCMOS, HSTL, SSTL, AGP, CTT, GTL
    - LVDS and LVPECL differential I/O
  - Up to 120 differential I/O pairs that can be input, output, or bidirectional
- Fully supported by powerful Xilinx ISE development system
  - Fully automatic mapping, placement, and routing
  - Integrated with design entry and verification tools
  - Extensive IP library including DSP functions and soft

Table 1: **Spartan-IIE FPGA Family Members**

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O[1]	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	182	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	182	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	182	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	329	120	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	329	120	221,184	288K

Notes:

1. User I/O counts include the four global clock/user input pins. See details in Table 3, page 5

General Overview

The Spartan-IIE family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. The XC2S400E has four columns and the XC2S600E has six columns of block RAM. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-IIE FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes.

Spartan-IIE FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-IIE FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-IIE FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-IIE devices provide system clock rates beyond 200 MHz. Spartan-IIE FPGAs offer the most cost-effective solution while maintaining leading edge performance. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-IIE FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

Spartan-IIE Family Compared to Spartan-II Family

- Higher density and more I/O
- Higher performance
- Unique pinouts in cost-effective packages
- Differential signaling
  - LVDS, Bus LVDS, LVPECL
- V_{CCINT} = 1.8V
  - Lower power
  - 5V tolerance with external resistor
  - 3V tolerance directly
- LVTTL and LVCMOS2 input buffers powered by V_{CCO} instead of V_{CCINT}
- Unique larger bitstream

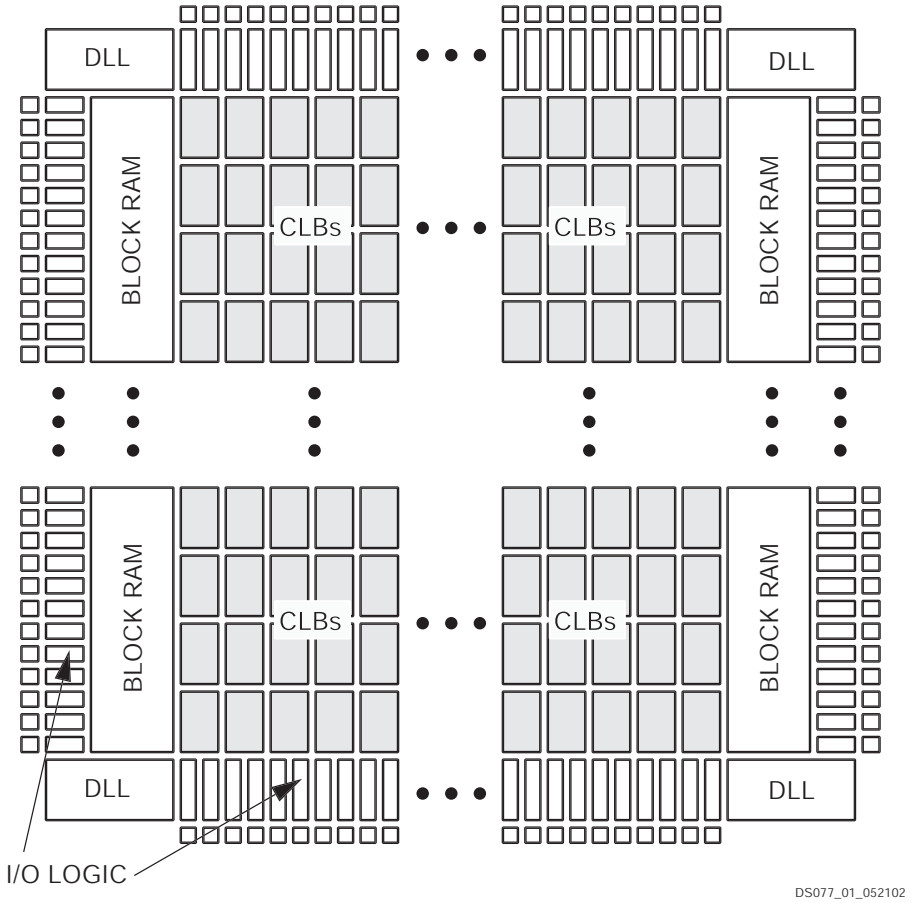


Figure 1: **Basic Spartan-IIE Family FPGA Block Diagram**

DC Specifications

Absolute Maximum Ratings(1)

Symbol	Description	Min	Max	Units
V_{CCINT}	Supply voltage relative to GND	–0.5	2.0	V
V_{CCO}	Supply voltage relative to GND	–0.5	4.0	V
V_{REF}	Input reference voltage	–0.5	4.0	V
V_{IN}	Input voltage relative to GND(2,3)	–0.5	4.05	V
V_{TS}	Voltage applied to 3-state output (3)	–0.5	4.0	V
T_{STG}	Storage temperature (ambient)	–65	+150	°C
T_J	Junction temperature	-	+135	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. V_{IN} should not exceed V_{CCO} by more than 3.6V over extended periods of time (e.g., longer than a day).
3. Maximum DC overshoot must be limited to either V_{CCO} + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to V_{CCO} + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Packaging Information on the Xilinx Web site.

Recommended Operating Conditions

Symbol	Description	Min	Max	Units
T_J	Junction temperature	–40	125	°C
V_{CCINT}	Supply voltage relative to GND(1)	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND(2)	1.2	3.6	V
T_{IN}	Input signal transition time(3)	-	250	ns

Notes:
1. Functional operation is guaranteed down to a minimum V_{CCINT} of 1.62V (Nominal V_{CCINT} –10%). For every 50 mV reduction in V_{CCINT} below 1.71V (nominal V_{CCINT} –5%), all delay parameters increase by 3%.
2. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
3. Input and output measurement threshold is ~50% of V_{CCO}.

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current(1)	XC2S50E	-	200	mA
		XC2S100E	-	350	mA
		XC2S150E	-	450	mA
		XC2S200E	-	550	mA
		XC2S300E	-	650	mA
		XC2S400E	-	750	mA
		XC2S600E	-	850	mA

Notes:
1. With no output current loads, no active pull-up resistors, and all I/O pins 3-stated and floating.

Spartan-IIE Product Availability

Table 2 shows the package and speed grades available for Spartan-IIE family devices. Table 3 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

Table 2: **Spartan-IIE Package and Speed Grade Availability**

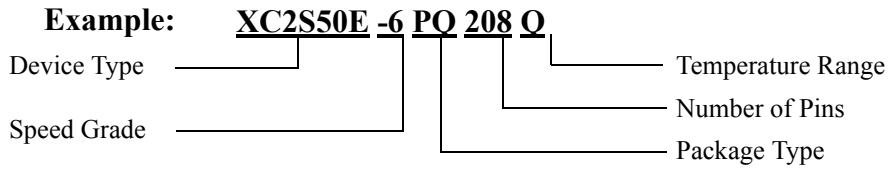
Device	Pins	144	208	256	456
	Type	Plastic TQFP	Plastic PQFP	Fine Pitch BGA	Fine Pitch BGA
	Code	TQ144	PQ208	FT256	FG456
XC2S50E	-6	Q	Q	Q	-
XC2S100E	-6	Q	Q	Q	-
XC2S150E	-6	-	Q	Q	-
XC2S200E	-6	-	Q	Q	-
XC2S300E	-6	-	Q	-	Q
XC2S400E	-6	-	-	-	Q
XC2S600E	-6	-	-	-	Q

Notes:
1. Q = Automotive IQ, T_J = –40°C to +125°C

Table 3: **Spartan-IIE User I/O Chart**

Device	Maximum User I/O	Available User I/O According to Package Type			
		TQ144	PQ208	FT256	FG456
XC2S50E	182	102	146	182	-
XC2S100E	182	102	146	182	-
XC2S150E	182	-	146	182	-
XC2S200E	182	-	146	182	-
XC2S300E	329	-	146	-	329
XC2S400E	329	-	-	-	329
XC2S600E	329	-	-	-	329

Ordering Information



Device Ordering Options

Device
XC2S50E
XC2S100E
XC2S150E
XC2S200E
XC2S300E
XC2S400E
XC2S600E

Speed Grade	
-6	Standard Performance

Package Type / Number of Pins	
TQ144	144-pin Plastic Thin QFP
PQ208	208-pin Plastic QFP
FT256	256-ball Fine Pitch BGA
FG456	456-ball Fine Pitch BGA

Temperature Range (T_J)	
Q = Automotive IQ	–40°C to +125°C

Revision History

Version No.	Date	Description
1.0	07/17/02	Initial Xilinx release.
1.1	11/18/02	Added XC2S400-E and XC2S600-E devices. Added FG676 to package list.
1.2	11/26/02	Updated Max User I/O and Differential I/O Pairs in Table 1 and Max User I/O in Table 3. Updated notes for Recommended Operating Conditions.
1.3	06/04/03	Changed five-member family to seven-member family in first paragraph.
1.4	06/16/03	Updated features list. Added **DC Characteristics Over Operating Conditions** table. Deleted “FG676” from Table 2, Table 3, and the **Device Ordering Options** section.
1.5	07/16/03	Updated features list, Table 1, **DC Characteristics Over Operating Conditions** table, and Table 3.
1.6	09/24/03	Updated title to read "Product Specification" (removed "Advance")