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intel®

PRELIMINARY

8XC196MC INDUSTRIAL MOTOR CONTROL MICROCONTROLLER

87C196MC 16 Kbytes of On-Chip OTPROM*
87C196MC, ROM 16 Kbytes of On-Chip Factory-Programmed OTPROM
80C196MC ROMless

- High-Performance CHMOS 16-Bit CPU
- 16 Kbytes of On-Chip OTPROM/ Factory-Programmed OTPROM
- 488 bytes of On-Chip Register RAM
- Register to Register Architecture
- Up to 53 I/O Lines
- Peripheral Transaction Server (PTS) with 11 Prioritized Sources
- Event Processor Array (EPA)
  - — 4 High Speed Capture/Compare Modules
  - — 4 High Speed Compare Modules
- Extended Temperature Standard
- Two 16-Bit Timers with Quadrature Decoder Input
- 3-Phase Complementary Waveform Generator
- 13 Channel 8/10-Bit A/D with Sample/ Hold with Zero Offset Adjustment H/W
- 14 Prioritized Interrupt Sources
- Flexible 8-/16-Bit External Bus
- 1.75 μs 16 x 16 Multiply
- 3 μs 32/16 Divide
- Idle and Power Down Modes

4

The 8XC196MC is a 16-bit microcontroller designed primarily to control 3 phase AC induction and DC brushless motors. The 8XC196MC is based on Intel's MCS® 96 16-bit microcontroller architecture and is manufactured with Intel's CHMOS process.

The 8XC196MC has a three phase waveform generator specifically designed for use in "Inverter" motor control applications. This peripheral allows for pulse width modulation, three phase sine wave generation with minimal CPU intervention. It generates 3 complementary non-overlapping PWM pulses with resolutions of 0.125 μs (edge trigger) or 0.250 μs (centered).

The 8XC196MC has 16 Kbytes on-chip OTPROM/ROM and 488 bytes of on-chip RAM. It is available in three packages; PLCC (84-L), SDIP (64-L) and EIAJ/QFP (80-L).

Note that the 64-L SDIP package does not include P1.4, P2.7, P5.1 and the CLKOUT pins.

Operational characteristics are guaranteed over the temperature range of −40°C to +85°C.

The 87C196MC contains 16 Kbytes on-chip OTPROM. The 83C196MC contains 16 Kbytes on-chip ROM. All references to the 80C196MC also refers to the 83C196MC and 87C196MC unless noted.

*OTPROM (One Time Programmable Read Only Memory) is the same as EPROM but it comes in an unwindowed package and cannot be erased. It is user programmable.

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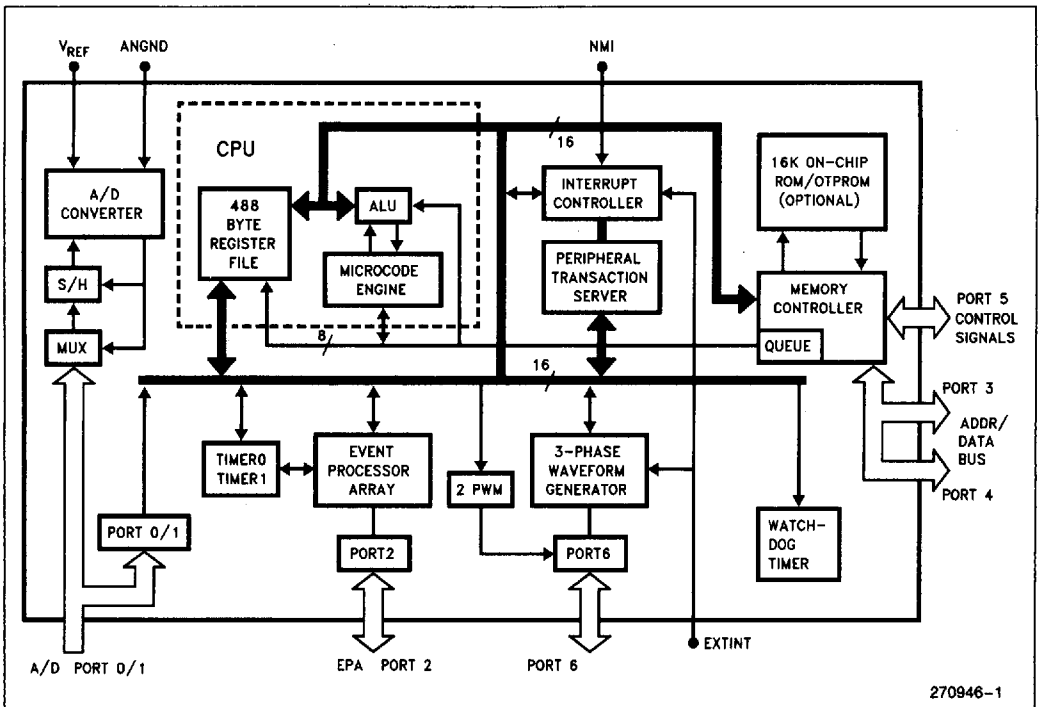
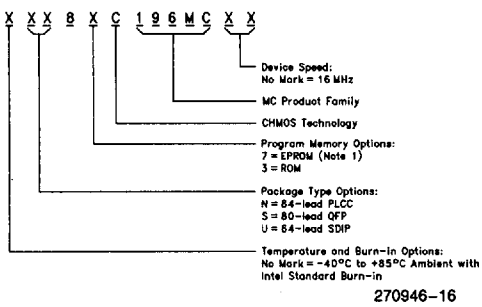


NOTE:
Connections between the standard I/O ports and the bus are not shown.

Figure 1. 87C196MC Block Diagram

PROCESS INFORMATION

This device is manufactured on PX29.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.



EXAMPLE: N87C196MC is 84-Lead PLCC OTPROM, 16 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 3. The 8XC196MC Family Nomenclature

Thermal Characteristics

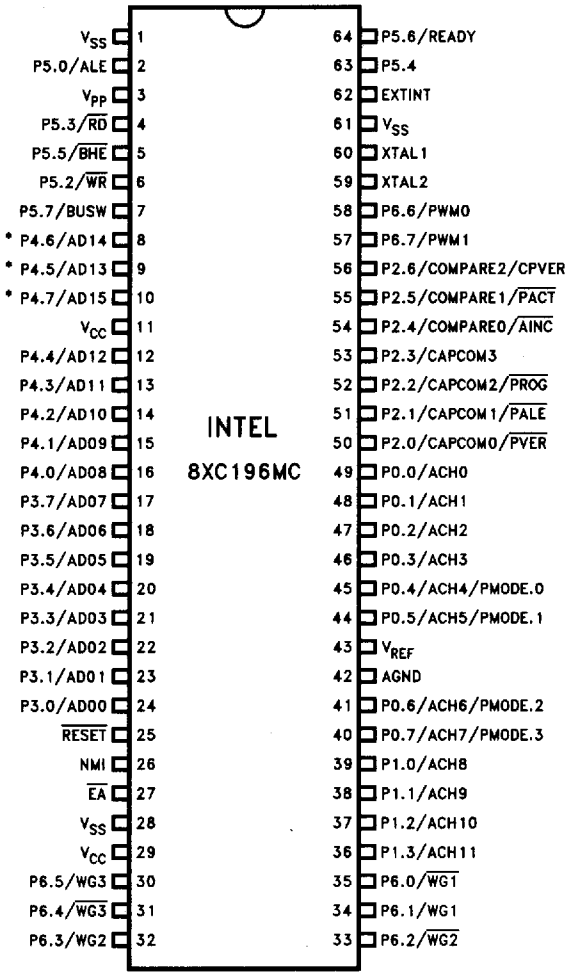
Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	56°C/W	12°C/W
SDIP	TBD	TBD

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

8XC196MC Memory Map

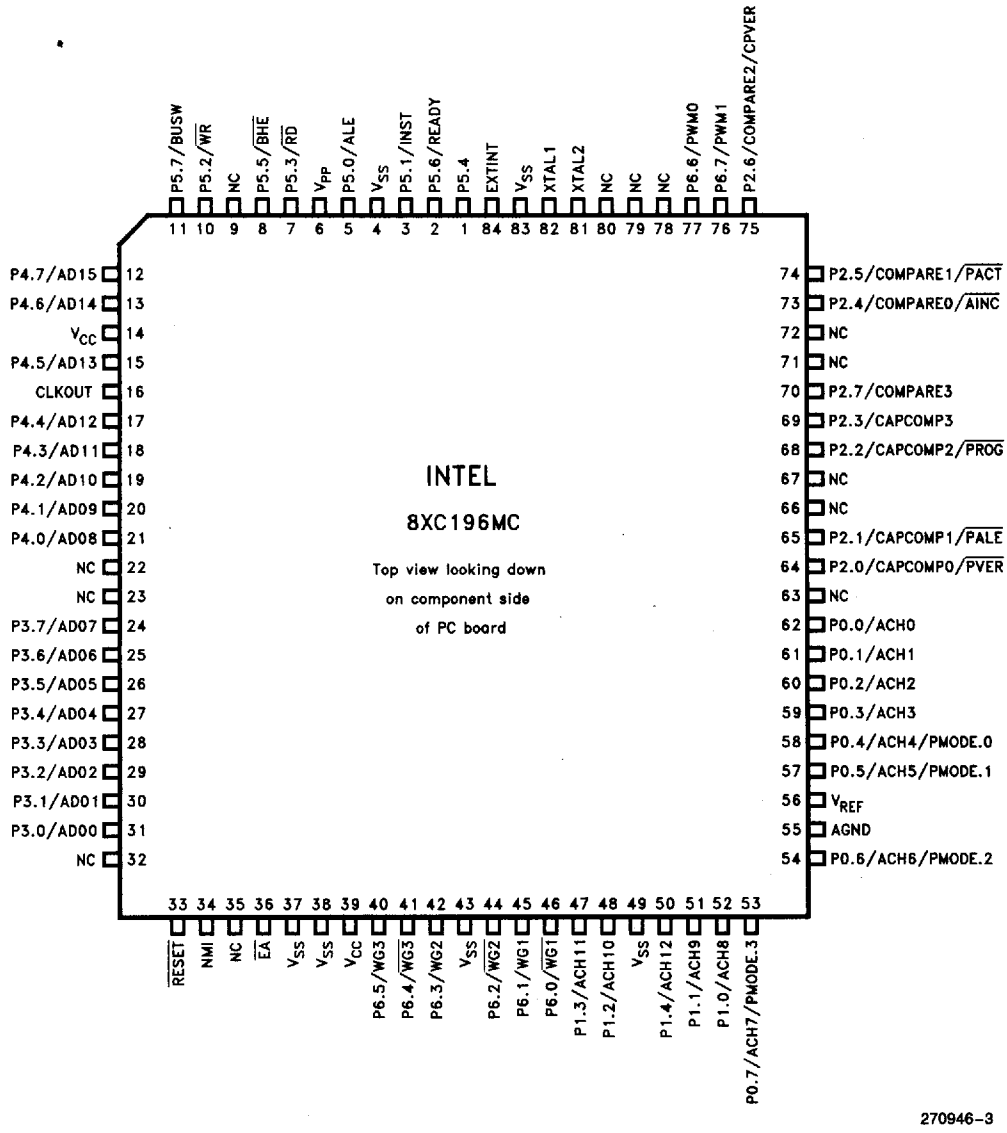
Description	Address
External Memory or I/O	0FFFFH 06000H
Internal ROM/EPROM or External Memory (Determined by $\overline{EA}$)	5FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 205EH
PTS Vectors	205DH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/EPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201CH
Reserved. Must Contain 20H (Note 5)	201BH
CCB1	201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB0	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
SFR's	1FFFH 1F00H
External Memory	1EFFH 0200H
488 Bytes Register RAM (Note 1)	01FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 03FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KC for SFR descriptions.
5. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.



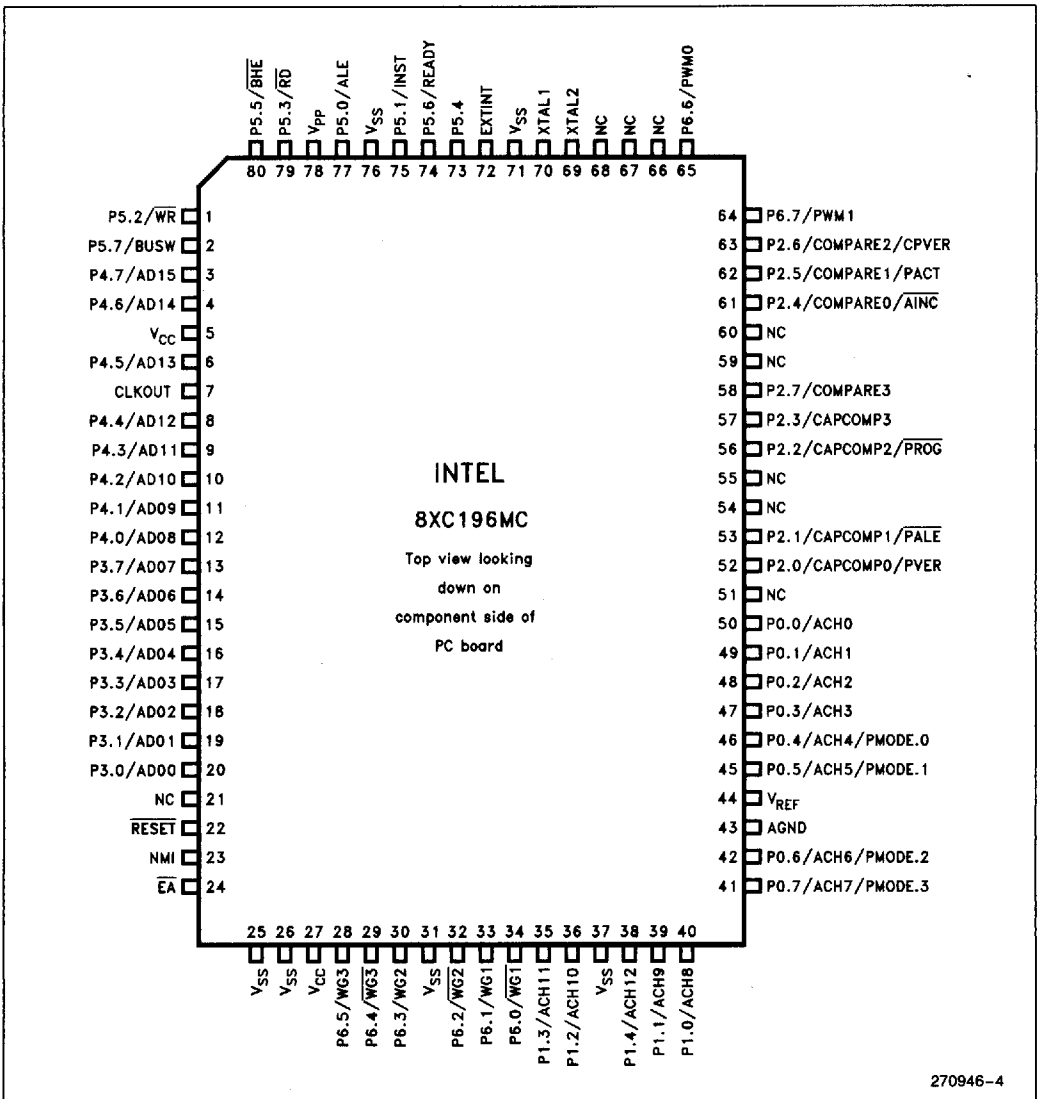
NOTE:
*The pin sequence is correct.
The 64-Lead SDIP package does not include the following pins: P1.4/ACH12, P2.7/COMPARE3, P5.1/INST, CLKOUT.

Figure 2. 64-Lead Shrink DIP (SDIP) Package



NOTE:
NC means No Connect. Do not connect these pins.

Figure 3. 84-Lead PLCC Package



NOTE:
NC means No Connect. Do not connect these pins.

Figure 4. 80-Lead Shrink EIAJQFP (Quad Flat Pack)

PIN DESCRIPTIONS (Alphabetically Ordered)

Symbol	Function
ACH0–ACH12 (P0.0–P0.7, P1.0–P1.4)	Analog inputs to the on-chip A/D converter. ACH0–7 share the input pins with P0.0–7 and ACH8–12 share pins with P1.0–4. If the A/D is not used, the port pins can be used as standard input ports.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
ALE/$\overline{\text{ADV}}$(P5.0)	Address Latch Enable or Address Valid output, as selected by CCR. Both options allow a latch to demultiplex the address/data bus on the signal's falling edge. When the pin is $\overline{\text{ADV}}$, it goes inactive (high) at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is active only during external memory accesses. Can be used as standard I/O when not used as ALE/ADV.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$ (P5.5)	Byte High Enable or Write High output, as selected by the CCR. $\overline{\text{BHE}}$ will go low for external writes to the high byte of the data bus. $\overline{\text{WRH}}$ will go low for external writes where an odd byte is being written. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is activated only during external memory writes.
BUSWIDTH (P5.7)	Input for bus width selection. If CCR bits 1 and 2 = 1, this pin dynamically controls the bus width of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If it is high, a 16-bit cycle occurs. This pin can be used as standard I/O when not used as BUSWIDTH.
CAPCOMP0–CAPCOMP3 (P2.0–P2.3)	The EPA Capture/Compare pins. These pins share P2.0–P2.3. If not used for the EPA, they can be configured as standard I/O pins.
CLKOUT	Output of the internal clock generator. The frequency is ½ of the oscillator frequency. It has a 50% duty cycle.
COMPARE0–COMPARE3 (P2.4–P2.7)	The EPA Compare pins. These pins share P2.4–P2.7. If not used for the EPA, they can be configured as standard I/O pins.
$\overline{\text{EA}}$	External Access enable pin. $\overline{\text{EA}}$ = 0 causes all memory accesses to be external to the chip. $\overline{\text{EA}}$ = 1 causes memory accesses from location 2000H to 5FFFH to be from the on-chip OTPROM/QROM. $\overline{\text{EA}}$ = 12.5V causes execution to begin in the programming mode. $\overline{\text{EA}}$ is latched at reset.
EXTINT	A programmable input on this pin causes a maskable interrupt vector through memory location 203CH. The input may be selected to be a positive/negative edge or a high/low level using WG_PROTECT (1FCEH).
INST (P5.1)	INST is high during the instruction fetch from the external memory and throughout the bus cycle. It is low otherwise. This pin can be configured as standard I/O if not used as INST.
NMI	A positive transition on this pin causes a non-maskable interrupt which vectors to memory location 203EH. If not used, it should be tied to V_{SS}. May be used by Intel Evaluation boards.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port0 pins should not be left floating. These pins also used to select programming modes in the OTPROM devices.
PORT1	5-bit high impedance input-only port. P1.0–P1.4 are also used as A/D converter inputs. In addition, P1.2 and P1.3 can be used as Timer 1 clock input and direction select respectively.
PORT2	8-bit bidirectional I/O port. All of the Port2 pins are shared with the EPA I/O pins (CAPCOMP0–3 and COMPARE0–3).
PORT3 PORT4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which uses strong internal pullups.
PORT5	8-bit bidirectional I/O port. 7 of the pins are shared with bus control signals ($\overline{\text{ALE}}$, INST, $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{BHE}}$, READY, BUSWIDTH). Can be used as standard I/O.

PIN DESCRIPTIONS (Alphabetically Ordered) (Continued)

Symbol	Function
PORT6	8-bit output port. P6.6 and P6.7 output PWM, the others are used as the Wave Form Generator outputs. Can be used as standard output ports.
PWM0, PWM1 (P6.6, P6.7)	Programmable duty cycle, Programmable frequency Pulse Width Modulator pins. The duty cycle has a resolution of 256 steps, and the frequency can vary from 122 Hz to 31 KHz (16 MHz input clock). Pins may be configured as standard output if PWM is not used.
$\overline{RD}$ (P5.3)	Read signal output to external memory. $\overline{RD}$ is low only during external memory reads. Can be used as standard I/O when not used as $\overline{RD}$.
READY (P5.6)	Ready input to lengthen external memory cycles. If READY = 0, the memory controller inserts wait states until the next positive transition of CLKOUT occurs with READY = 1. Can be used as standard I/O when not used as READY.
$\overline{RESET}$	Reset input to and open-drain output from the chip. Held low for at least 16 state times to reset the chip. Input high for normal operation. $\overline{RESET}$ has an Ohmic internal pullup resistor.
T1CLK (P1.2)	Timer 0 Clock input. This pin has two other alternate functions: ACH10 and P1.2.
T1DIR (P1.3)	Timer 0 Direction input. This pin has two other alternate functions: ACH11 and P1.3.
V_{PP}	The programming voltage is applied to this pin. It is also the timing pin for the return from Power Down circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If the Power Down feature is not used, connect the pin to V_{CC}.
WG1–WG3/$\overline{WG1}$–$\overline{WG3}$ (P6.0–P6.5)	3 phase output signals and their complements used in motor control applications. The pins can also be configured as standard output pins.
$\overline{WR}$/$\overline{WRL}$ (P5.2)	Write and Write Low output to external memory. $\overline{WR}$ will go low every external write. $\overline{WRL}$ will go low only for external writes to an even byte. Can be used as standard I/O when not used as $\overline{WR}$/$\overline{WRL}$.
XTAL1	Input of the oscillator inverter and the internal clock generator. This pin should be used when using an external clock source.
XTAL2	Output of the oscillator inverter.
PMODE (P0.4–7)	Determines the EPROM programming mode.
$\overline{PACT}$ (P2.5)	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.
$\overline{PALE}$ (P2.1)	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{PROG}$ (P2.2)	A falling edge in Slave Programming Mode begins programming. A rising edge ends programming.
PVER (P2.0)	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
CPVER (P2.6)	Cumulative Program Verification. Pin is high if all locations since entering a programming mode have programmed correctly.
$\overline{AINC}$ (P2.4)	Auto Increment. Active low input enables the auto increment mode. Auto increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
Under Bias ..... −40°C to +85°C

Storage Temperature ..... −65°C to +150°C

Voltage from $\overline{EA}$ or V_{PP}
to V_{SS} or ANGND ..... +13.00V

Voltage on V_{PP} or $\overline{EQ}$
to V_{SS} or ANGND ..... −0.5V to 13.0V

Voltage on Any Other Pin
to V_{SS} or ANGND ..... −0.5V to +7.0V(1)

Power Dissipation ..... 1.5W(2)

NOTES:
1. This includes V_{PP} and $\overline{EA}$ on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
F_{OSC}	Oscillator Frequency	8	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential. Also V_{SS} and V_{SS1} must be at the same potential.

DC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.3 V_{CC}	V	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage Port 2 and 5, P6.6, P6.7, CLKOUT		0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage on Port 3/4		1.0	V	I_{OL} = 15 mA
V_{OL2}	Output Low Voltage on Port 6.0–6.5		0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7 mA
$V_{th+} - V_{th-}$	Hysteresis Voltage Width on $\overline{RESET}$	0.2		V	Typical

DC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Leakage Current on All Input Only Pins			±10	μA	$0V < V_{IN} < V_{CC}-0.3V$ (in RESET)
I_{LI1}	Input Leakage Current on Port0 and Port1			±3	μA	$0V < V_{IN} < V_{REF}$
I_{IL}	Input Low Current on BD Ports (Note 1)			−70	μA	$V_{IN} = 0.3\ V_{CC}$
I_{IL1}	Input Low Current on P5.4 and P2.6 during Reset			−7	mA	$0.2\ V_{CC}$
I_{OH}	Output High Current on P5.4 and P2.6 during Reset	−2			mA	$0.7\ V_{CC}$
I_{CC}	Active Mode Current in Reset		50	70	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Conversion Reference Current		2	5	mA	
I_{IDL}	Idle Mode Current		15	30	mA	
I_{PD}	Power-Down Mode Current		5	50	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	$\overline{RESET}$ Pin Pullup Resistor	6k		65k	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	$F_{TEST} = 1.0$ MHz

NOTES:

1. BD (Bidirectional ports) include:
   P2.0–P2.7, except P2.6
   P3.0–P3.7
   P4.0–P4.7
   P5.0–P5.3
   P5.5–P5.7
2. During normal (non-transient) conditions, the following total current limits apply:

P6.0–P6.5	I_{OL}: 40 mA	I_{OH}: 28 mA
P3	I_{OL}: 90 mA	I_{OH}: 42 mA
P4	I_{OL}: 90 mA	I_{OH}: 42 mA
P5, CLKOUT	I_{OL}: 35 mA	I_{OH}: 35 mA
P2, P6.6, P6.7	I_{OL}: 63 mA	I_{OH}: 63 mA

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H — High
L — Low
V — Valid
X — No Longer Valid
Z — Floating

Signals:

A — Address
B — $\overline{BHE}$
C — CLKOUT
D — DATA
G — Buswidth
H — $\overline{HOLD}$
HA — $\overline{HLDA}$
L — ALE/$\overline{ADV}$
BR — $\overline{BREQ}$
R — $\overline{RD}$
W — $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X — XTAL1
Y — READY
Q — Data Out

AC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz.

The system must meet the following specifications to work with the 87C196MC:

Symbol	Parameter	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1	8	16	MHz	3
T_{OSC}	$1/F_{XTAL}$	62.5	125	ns	
T_{AVYV}	Address Valid to READY Setup		$2\,T_{OSC} - 75$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns	4
T_{YLYH}	Not READY Time	No Upper Limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	1
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2\,T_{OSC} - 40$	ns	1
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2\,T_{OSC} - 75$	ns	
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns	4
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3\,T_{OSC} - 55$	ns	2
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 22$	ns	2
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.
3. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
4. These timings are included for compatibility with older −90 and BH products. They should not be used for newer high-speed designs.

AC ELECTRICAL CHARACTERISTICS (Continued)

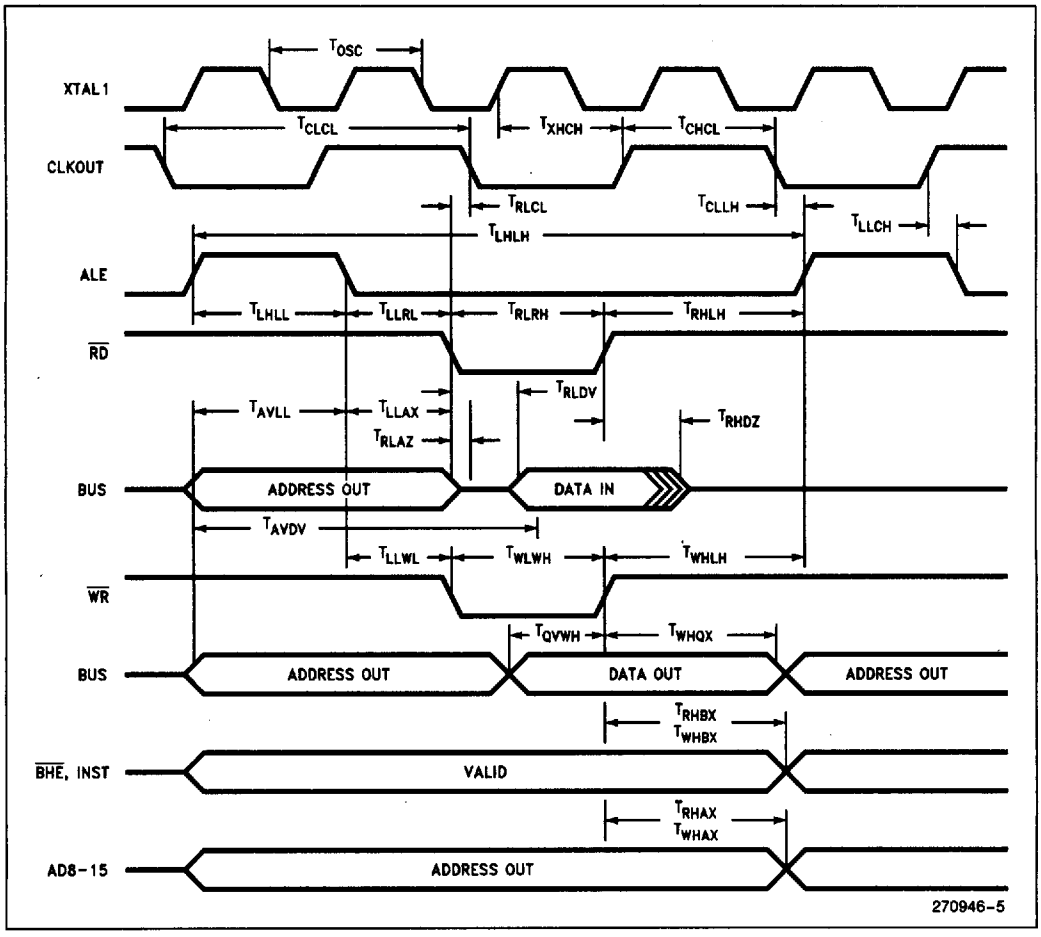
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz.

The 87C196MC will meet the following timing specifications:

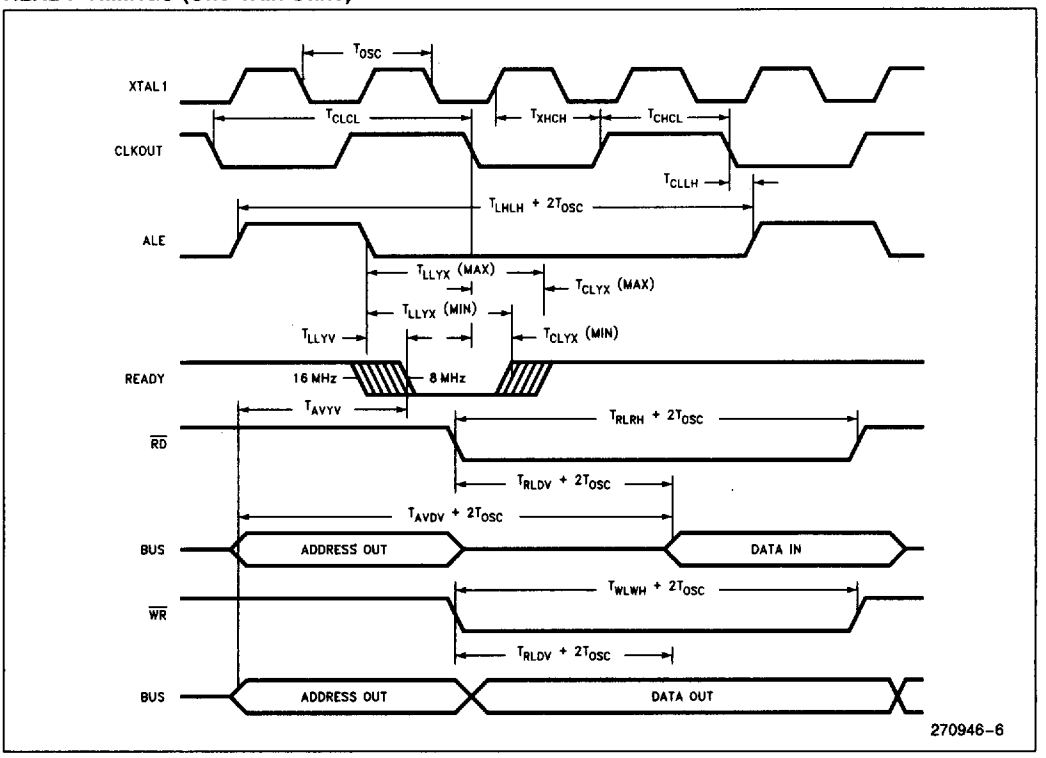
Symbol	Parameter	Min	Max	Units	Notes
T_{XHCH}	XTAL1 to CLKOUT High or Low	30	110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 15	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	3
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 15		ns	
T_{LLAX}	Address Hold after ALE Falling	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling	T_{OSC} − 30		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5	T_{OSC} + 25	ns	3
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	1
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 30		ns	3
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 25		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 15	ns	1
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ Rising	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising	T_{OSC} − 30		ns	2
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ Rising	T_{OSC} − 10		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising	T_{OSC} − 30		ns	2

NOTES:
1. Assuming back to back cycles.
2. 8-bit bus only.
3. If wait states are used, add 2 T_{OSC}*N, where N = number of wait states.

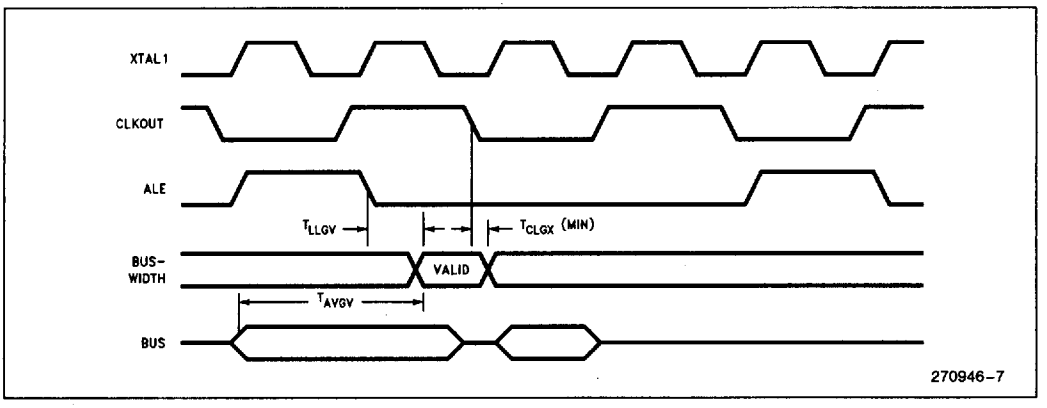
SYSTEM BUS TIMINGS



READY TIMINGS (One Wait State)



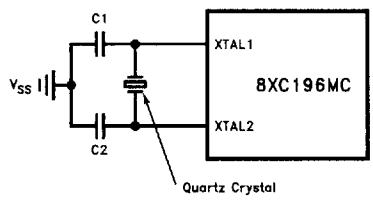
BUSWIDTH TIMINGS



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16.0	MHz
T_{XLXL}	Oscillator Period	62.5	125	ns
T_{XHXX}	High Time	22		ns
T_{XLXX}	Low Time	22		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

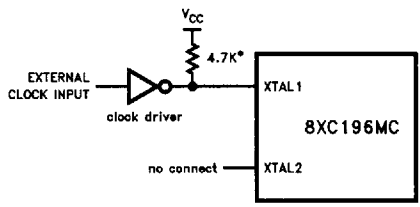
EXTERNAL CRYSTAL CONNECTIONS



270946-14

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

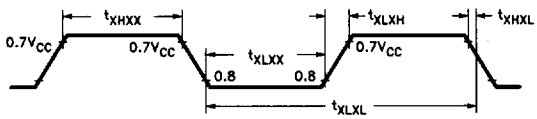
EXTERNAL CLOCK CONNECTIONS



270946-15

* Required if TTL driver used.
Not needed if CMOS driver is used.

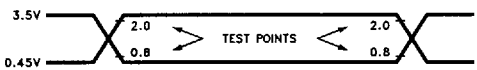
EXTERNAL CLOCK DRIVE WAVEFORMS



270946-8

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

AC TESTING INPUT, OUTPUT WAVEFORMS



270946-9

AC Testing inputs are driven at 3.5V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS

270946-10

For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs I_{OL}/I_{OH} = ≤ ±15 mA.

A TO D CHARACTERISTICS

The sample and conversion time of the A/D converter in the 8-bit or 10-bit modes is programmed by loading a byte into the AD_TIME Special Function Register. This allows optimizing the A/D operation for specific applications. The AD_TIME register is functional for all possible values, but the accuracy of the A/D converter is only guaranteed for the times specificed in the operating conditions table.

The value loaded into AD_TIME bits 5, 6, 7 determines the sample time, T_{SAM}, and is calculated using the following formula:

$$SAM = \frac{(T_{SAM} \times F_{OSC}) - 2}{8}$$

T_{SAM} = Sample time, μs
F_{OSC} = Processor frequency, MHz
SAM = Value loaded into AD_TIME bits 5, 6, 7

SAM must be in the range 1 through 7.

The value loaded into AD_TIME bits 0–5 determines the conversion time, T_{CONV}, and is calculated using the following formula:

$$CONV = \frac{(T_{CONV} \times F_{OSC}) - 3}{2B} - 1$$

T_{CONV} = Conversion time, μs
F_{OSC} = Processor frequency, MHz
B = 8 for 8-bit conversion
B = 10 for 10-bit conversion
CONV = Value loaded into AD_TIME bits 0–5

CONV must be in the range 2 through 31.

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the analog portion of the converter and input port pins. There is also an AD_TEST SFR that allows for conversion on ANGND and V_{REF} as well as adjusting the zero offset. The absolute error listed is WITHOUT doing any adjustments.

A/D CONVERTER SPECIFICATION

The specifications given assume adherence to the operating conditions section of this data sheet. Testing is performed with V_{REF} = 5.12V and 16.0 MHz operating frequency. After a conversion is started, the device is placed in the IDLE mode until the conversion is complete.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	10.0	20.0	μs(2)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTES:
ANGND and V_{SS} should nominally be at the same potential.
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Min	Max	Units*
Resolution		1024 10	1024 10	Levels Bits
Absolute Error		0	±4	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±4	LSBs
Differential Non-Linearity		> −1	+2	LSBs
Channel-to-Channel Matching	±0.1	0	±1.0	LSBs
Repeatability	±0.25	0		LSBs
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	2K	Ω(4)
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5, 6)
Sampling Capacitor	3			pF
DC Input Leakage	±1	0	±3.0	μA

NOTES:
*An "LSB", as used here has a value of approximately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	7.0	20.0	μs(2)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTES:
ANGND and V_{SS} should nominally be at the same potential.
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over the Above Operating Conditions)

Parameter	Typical(1)	Min	Max	Units*
Resolution		256 8	256 8	Level Bits
Absolute Error		0	±1	LSBs
Full Scale Error	±0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity		0	±1	LSBs
Differential Non-Linearity		>−1	+1	LSBs
Channel-to-Channel Matching		0	±1.0	LSBs
Repeatability	±0.25			LSBs
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	2K	Ω(4)
Voltage on Analog Input Pin		V_{SS} − 0.5	V_{REF} + 0.5	V(5, 6)
Sampling Capacitor	3			pF
DC Input Leakage	±1	0	±3.0	μA

NOTES:
*An "LSB" as used here, has a value of approximately 20 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.

EPROM SPECIFICATIONS

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}	Supply Voltage during Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage during Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
T_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(1)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	PROG High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

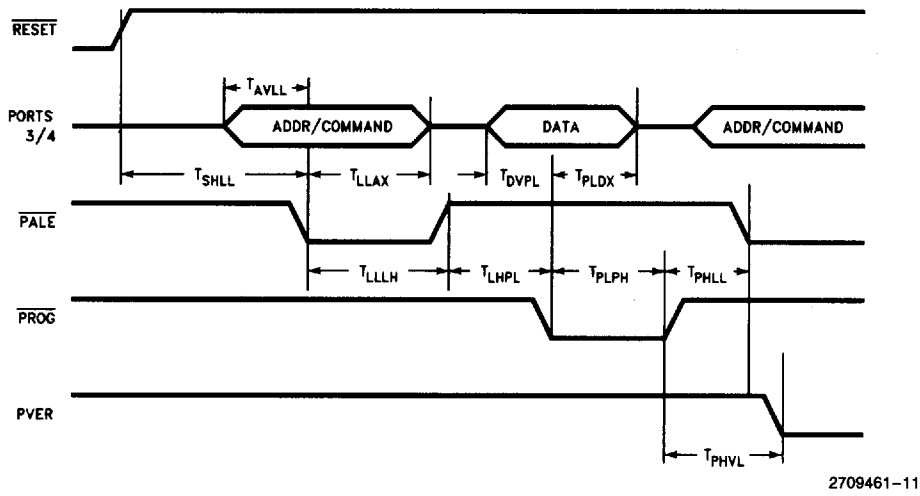
NOTE:
1. This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm.

DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

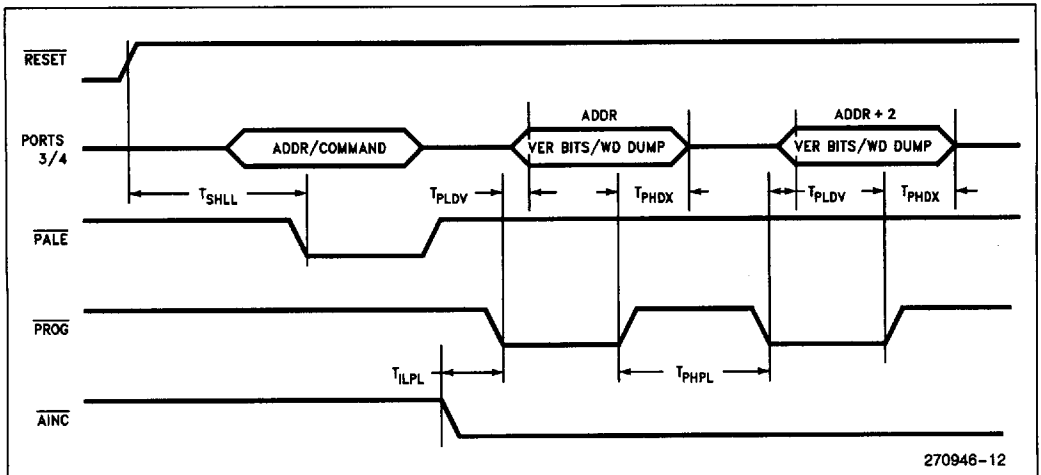
NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



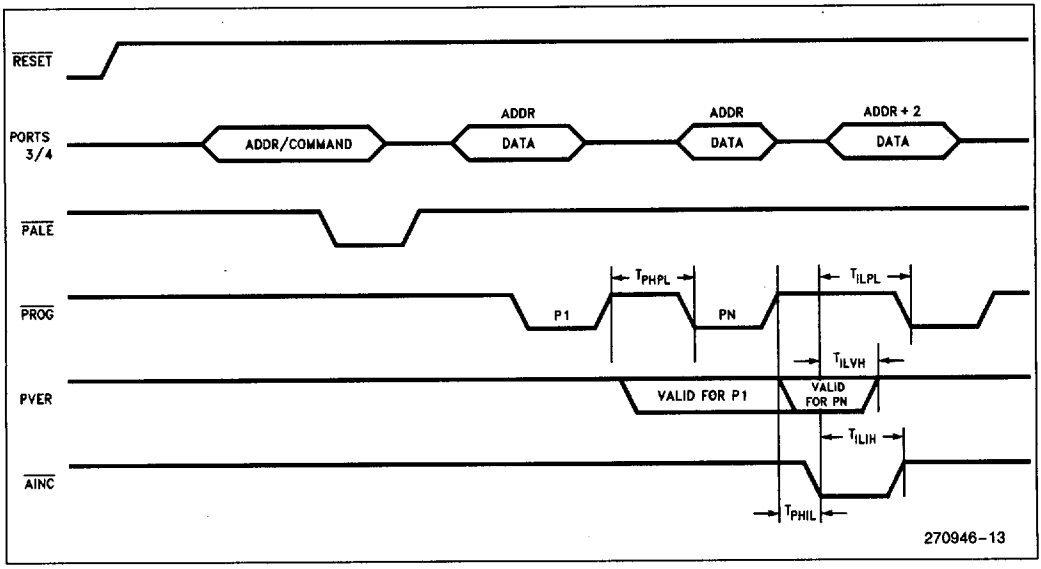
NOTE:
P3.0 must be high ("1")

SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



NOTE:
P3.0 must be low ("0")

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



87C196MC DESIGN CONSIDERATIONS

When an indirect shift during divide occurs the upper 3 bits of the shift count are not masked completely. If the shift count register has the value 32*n where n = 1, 3, 5 or 7, the operand will be shifted 32 times. This should have resulted in no shift taking place.

DATA SHEET REVISION HISTORY

This data sheet (270946-004) is valid for devices with a "B" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following important differences exist between this data sheet (270946-002) and the previous version (270946-003):

1. The data sheet was reorganized to standard format.
2. Added 83C196MC device.
3. Added package thermal characteristics.
4. Added note on missing pins on SDIP package.
5. Removed SFR maps (now in user's manual).
6. Added note on T_{LLYV} and T_{LLGV} specifications.
7. Changed 10-bit mode T_{CONV} (MIN) to 10.0 μs from 15.0 μs.
8. Changed 10-bit mode T_{CONV} (MAX) to 20.0 μs from 18.0 μs.
9. Changed VREF (MIN) in 8- and 10-bit mode to 4.0V from 4.5V.

The following important differences exist between data sheet 270946-003 and the previous version (270946-002):

1. The data sheet title was changed to better reflect the purpose of the 87C196MC as an AC Inverter/DC Brushless Motor Control Microcontroller.
2. The standard temperature range for this part now covers −40°C to +85°C.
3. EXTINT function description now includes WG_PROTECT (1FCEH) as the name and address of the register used to select positive/negative or high/low detection for EXTINT.
4. The memory range 01F00H–01FBFH was added to the SFR map as RESERVED.
5. I_{IL} changed from −60 μA to −70 μA.
6. I_{REF} changed from 5 mA to 2 mA maximum and the typical specification was removed.
7. The READY description of the READY TIMINGS (One Wait State) graphic was modified to denote the shifting of the leading edge of READY versus frequency. At 16 MHz the falling edge of READY occurs before the falling edge of ALE.
8. AC Testing Input, Output Waveform was changed to reflect inputs driven at 3.5V for a Logic "1" and .45V for a Logic "0" and timing measurements made at 2.0V for a Logic "1" and 0.8V for a Logic "0".
9. Float Waveform was changed from I_{OL}/I_{OH} = ±15 mA to $I_{OL}/I_{OH} \leq \pm 15$ mA
10. AD_TIME register for 10-bit conversions was changed from 0C7H to 0D8H. The number of sample time states was changed from 24 to 25 states, the conversion time states was changed from 80 to 240 states, and the total conversion time for AD_TIME = D8H replaced the total conversion time for AD_TIME = C7H.
11. The number of sample time states for an 8-bit conversion was changed from 20 states to 21 states.
12. There is a single entry in the ERRATA section of this version of the data sheet concerning the results of an indirect shift during divide.

The following important differences exist between this data sheet (270946-002) and the previous version (270946-001):

1. T_A Ambient Temperature Under Bias Min changed from −20°C to −40°C.
2. I_{REF} A/D Conversion Reference Current Max changed from 5 mA to 2 mA.
3. Testing levels changed from TTL values to CMOS values.
4. A/D Input Series Resistance Max changed from 1.2 KΩ to 2 KΩ.