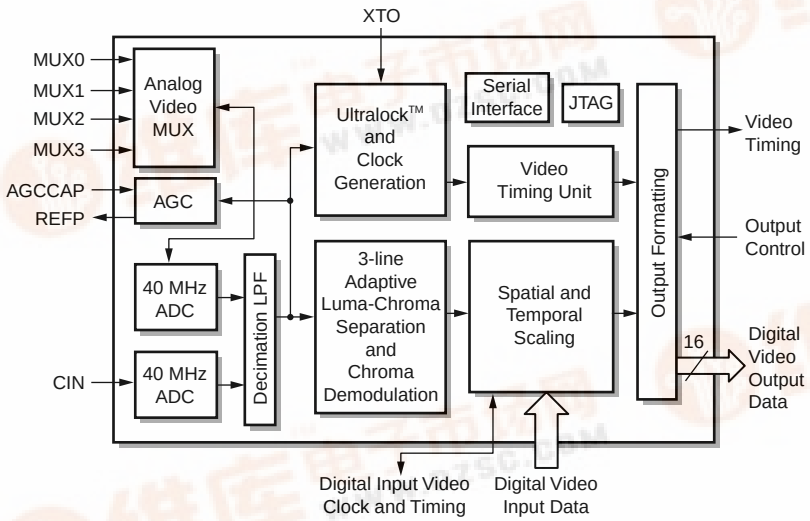
CONEXANT™

Bt835 VideoStream™ III Decoder

Video Capture Processor and Scaler for TV/VCR Analog Input

The Bt835 VideoStream III Decoder is a high quality single-chip, composite NTSC/PAL/SECAM video and S-Video decoder. Low operating power consumption and power-down capability make it an ideal low-cost solution for PC video capture applications on both desktop and portable system platforms. The Bt835 supports square pixel and CCIR601 resolutions for NTSC, PAL, and SECAM video. The Bt835 has a sophisticated 3-line adaptive comb filter to maintain full vertical video resolution and eliminate traditional comb filter artifacts. The Bt835's flexible pixel ports support digital video input as well as VIP and ByteStream interfaces to popular graphics controllers.

Functional Block Diagram



Distinguishing Features

- Single-chip composite/S-Video NTSC/PAL/SECAM to YCrCb digitizer
- On-chip Ultralock™
- Square pixel and CCIR601 resolution for:
  - NTSC (M), NTSC (4.43)
  - NTSC (M) without 7.5 IRE pedestal
  - PAL (B, D, G, H, I, M, N, N combination), PAL (60)
  - SECAM
- NTSC 3-line adaptive comb filter
- Arbitrary horizontal and 5-tap vertical filtered scaling
- Hardware closed-caption decoder
- Vertical Blanking Interval (VBI) data pass-through
- Single crystal for any video format
- Arbitrary temporal decimation for a reduced frame-rate video sequence
- Programmable hue, brightness, saturation, and contrast
- Digital video input port
- 2x oversampling to simplify external analog filtering
- 2-line serial programming interface
- 8- or 16-bit pixel interface
- YCrCb (4:2:2) output format
- Software selectable four-input analog MUX
- Eight fully programmable GPIO bits
- Auto NTSC/PAL format detect
- Automatic Gain Control (AGC)
- Typical power consumption 500 mW (3.3 V)
- IEEE 1149.1 Joint Test Action Group (JTAG) interface
- 100-pin PQFP package
- VIP, ByteStream interfaces

Related Products

- Bt829B, Bt868/869

Applications

- Multimedia
- Image processing
- Desktop video
- Video phone
- Interactive video

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt835KRF	100-pin PQFP	0 °C to +70 °C

Revision History

Revision	Level	Date	Description
A	Advance	October 1998	Created
B			Upgrade to Conexant format.
C		April 2001	Engineering changes and corrections

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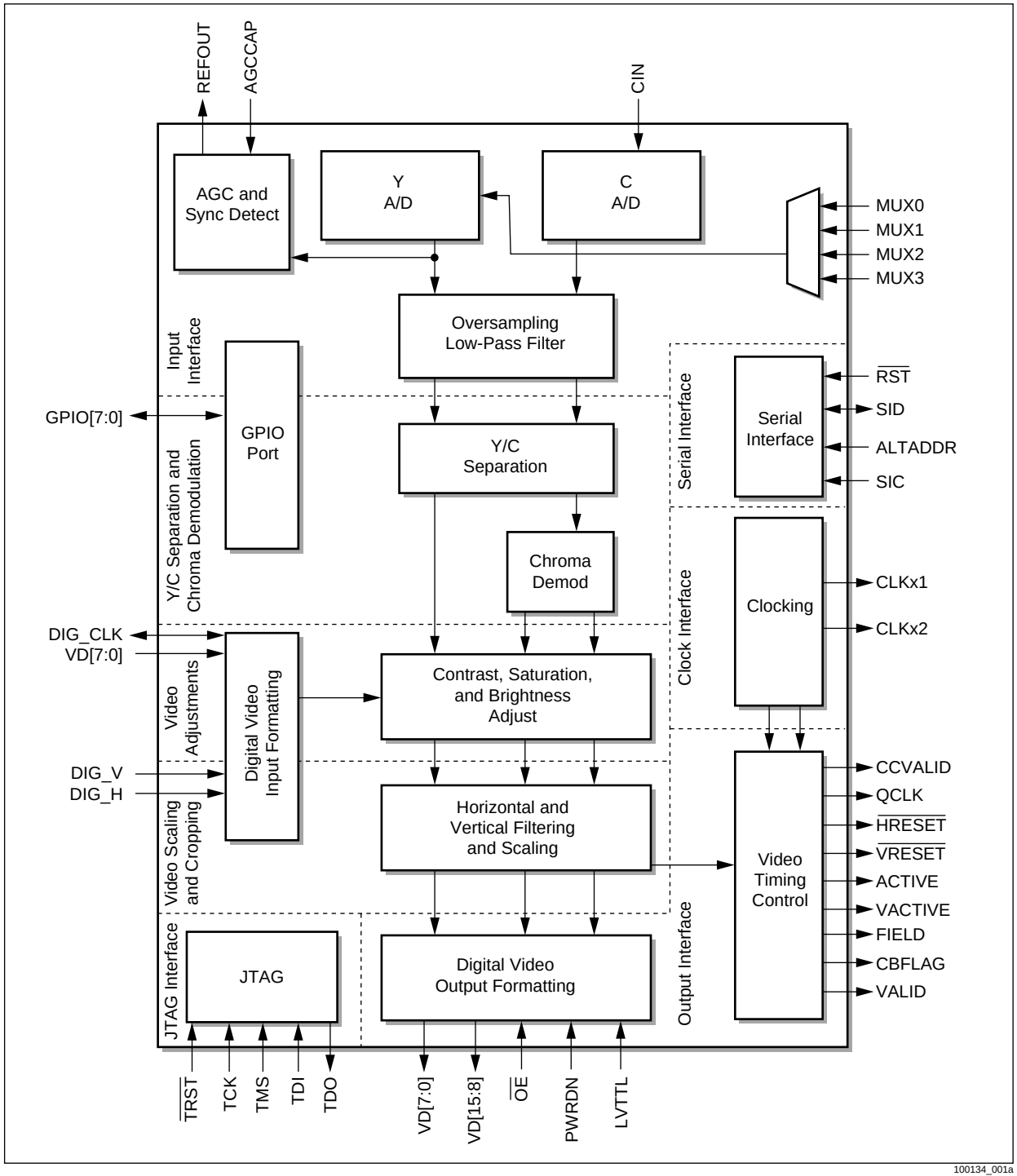
1.0 Functional Description

1.1 Functional Overview

Conexant's VideoStream™ III decoder is a high quality, single-chip solution for processing all analog NTSC/PAL/SECAM video standards into 4:2:2 YCrCb video. The Bt835 offers the highest price/performance of any video decoder, with its unique 3-line adaptive comb filter, digital video input port, flexible digital video output port, single crystal operation, and low power consumption.

Figure 1-1 illustrates a detailed block diagram of the decoder.

Figure 1-1. Bt835 Detailed Block Diagram



1.1.1 Bt835 Video Capture Processor for TV/VCR Analog Input

The Bt835 Video Capture Processor is a fully integrated single-chip decoding and scaling solution for analog NTSC/PAL/SECAM input signals from TV tuners, VCRs, cameras, and other sources of composite or Y/C video. It is the third generation front-end input solution for low-cost PC video/graphics systems. The Bt835 delivers complete integration and high-performance video synchronization, Y/C separation, and filtered scaling. It has all the mixed signal and DSP circuitry required to convert an analog composite waveform into a scaled digital video stream supporting a variety of video formats, resolutions, and frame rates.

The Bt835 builds on the previous Bt829B VideoStream II decoder by adding the features detailed in Table 1-1.

Table 1-1. VideoStream III Features Options

Feature Options	Bt829B	Bt835
Composite Video Decoding	X	X
S-Video Decoding	X	X
SECAM Video	X	X
Hardware Closed-Caption Decoding	X	X
Filtered Vertical Scaling	X	X
3-line Adaptive Comb Filter		X
Single Crystal Operation for all Video Formats		X
Digital Video Input Port		X
PAL 60, NTSC 4.43 Decoding		X
8-bit GPIO		X
VIP Interface		X

1.1.2 Bt835 Architecture and Partitioning

The Bt835 provides the most cost-effective, high-quality video input solution for low-cost multimedia subsystems that integrate graphics display and video capabilities. The feature set of the Bt835 supports a video/graphics system partitioning, that optimizes the total cost of a system configured with and without video capture capabilities. This enables system vendors to easily offer products with graphics display and video support using a single base-system design.

As graphics chip vendors move from PCI video/graphics processors to 3D AGP graphics processors, the ability to efficiently use silicon and package pins to support 2D/3D graphics acceleration, video playback acceleration, and video capture becomes critical. This problem becomes more acute as the race toward higher performance graphics requires more and more package pins to be consumed for wide 128-bit memory interfaces and glueless local bus interfaces.

The Bt835 minimizes the cost of video capture function integration in two ways. First, recognizing that YCrCb to RGB color space conversion is a standard feature of multimedia controllers for acceleration of digital video playback, the Bt835 avoids redundant functionality and allows the downstream controller to perform this task. Second, the Bt835 can minimize the number of interface pins required by a downstream multimedia controller to keep package costs to a minimum. This is accomplished by using industry standards interfaces such as the VESA Video Interface Port (VIP) or the Conexant ByteSteam™ interface.

Controller systems designed to take advantage of these features allow video capture capability to be added to the base system in a modular fashion using only a single Integrated Circuit (IC).

1.1.3 Comb Filter

Many video decoders employ a luminance notch filter, a chrominance bandpass filter, and a chrominance comb filter. The luminance signal is derived by filtering out the color information (chrominance) from a composite video signal with a notch filter. This works because the NTSC color information is in a frequency band centered at about 3.58 MHz that extends about +/- 1.3 MHz (i.e., from 2.3 to 4.9 MHz). The Y filter rejects frequencies in that range. Although this effectively filters most of the chrominance signal out of the luminance signal, it also removes the higher frequency luminance signal components. This loss of bandwidth reduces the horizontal resolution of the luminance signal, and fine details in the picture are lost. The chrominance signal is derived by bandpass filtering the composite video signal to extract the frequency band centered at 3.58 MHz that contains the color information. A chrominance comb filter removes any residual luminance (Y) signal that overlaps the chrominance (C) signal in this frequency range.

Other video decoders employ a line comb filter. These line comb filters operate by delaying the previous composite video horizontal scan line and comparing it to the current horizontal scan line. Adding the two lines together cancels the C signal and provides the Y signal. Subtracting the current line from the delayed line provides the C signal. This process creates two filters which have a frequency response that look like teeth in a comb. This type of filter is usually known as a 1-H comb filter, since it uses a 1-horizontal scan line delay to process the signals. More complex filters can be built using 2-horizontal scan line delays and are called 2-H comb filters. While these filters show improvement with a multiburst test pattern compared to a notch filter, and demonstrate a horizontal flat frequency response, the multiburst pattern does not show that 50% of the vertical resolution is lost due to the averaging of two lines. These filters still suffer the “hanging dot” problem noticeable on test patterns such as the SMPTE color bar test pattern.

In order to overcome this hanging dot problem and the loss of vertical resolution, Conexant designed a sophisticated 3-line, adaptive comb filter to separate the Y/C components in a composite video signal. The new Bt835 video decoder uses this circuit. As stated above, simple 1-H comb filters can not eliminate "hanging dots" on a vertical color transition. Comb filtering two successive scan lines with different color values at the same horizontal positions along the lines cause the problem. The line comb filter cannot separate the Y/C signals correctly in this situation. The color signal crosses over into the luminance signal, creating the cross-luminance artifact. In a 3-line adaptive Y/C separation filter, adaptive logic continuously evaluates the video image and then selects the most efficient processing algorithm available in the filter. This is sometimes called a 2-D filter, because both the horizontal scan lines and vertical transitions are processed. This eliminates the hanging dot problem by detecting vertical transitions in the image. The logic examines three successive horizontal scan lines simultaneously. If a vertical transition occurs between the first and third lines, the notch filtered luminance and bandpass filtered chrominance are used directly, without comb filtering. Hence, two lines with different colors will not be input to the comb filter at a transition boundary. Therefore, the Y/C signals will be fully separated and the hanging dots eliminated. The Bt835 accomplishes this adaptive task on a pixel by pixel basis by using powerful DSP techniques. This also ensures that the Y/C separated image does not suffer from any loss of vertical resolution.

1.1.4 UltraLock

The Bt835 employs a proprietary technique known as UltraLock to lock the incoming analog video signal. It always generates the required number of pixels per line from an analog source where line length can vary by as much as a few microseconds. UltraLock's digital locking circuitry enables VideoStream™ decoders to quickly and accurately lock on to video signals, regardless of their source. Because the technique is completely digital, UltraLock can recognize unstable signals caused by VCR head switches or any other deviation, and adapt the locking mechanism to accommodate the source. UltraLock uses nonlinear techniques which are difficult, if not impossible, to implement for genlock systems. Unlike linear techniques, it automatically adapts the locking mechanism.

1.1.5 Scaling and Cropping

The Bt835 independently reduces the video image size in both horizontal and vertical directions. Using arbitrarily selected scaling ratios, the X and Y dimensions can be scaled down to one-sixteenth of the full resolution. Horizontal scaling is implemented with a six-tap interpolation filter, while a maximum of five-tap interpolation is used for vertical scaling with a line store.

The video image can be arbitrarily cropped by programming the ACTIVE flag to reduce the number of active scan lines and active horizontal pixels per line.

The Bt835 also supports a temporal decimation feature that reduces video bandwidth by allowing frames or fields to be dropped from a video sequence at regular, but arbitrarily selected, intervals.

1.1.6 Input Interfaces

Analog Video Input

Analog video signals are input to the Bt835 via a four-input multiplexer that can select between four composite source inputs, or between three composite input sources and a single S-Video input source. When an S-Video source is input to the Bt835, the luma component is fed through the input analog multiplexer, and the chroma component feeds directly into the C input pin. An AGC circuit enables the Bt835 to compensate for reduced amplitude in the analog signal input.

The clock signal interface consists of two pins for crystal connection and two clock output pins. These crystal pins connect to any standard 14.318 MHz, low-jitter (50 ppm or better) crystal for NTSC /PAL/SECAM operation. The on-board PLL circuit generates output clocks for interface to the graphics controller or frame buffer. CLKx2 is output at full frequency (8*Fsc), whereas CLKx1 operates at half the synthesized crystal frequency (4*Fsc). Either crystals or CMOS oscillators may be used for the clock source.

Digital Video Input

The Bt835 accepts digital video data as 8-bit, 26-30 MHz 4:2:2 YCrCb samples on the VD[7:0] pins. The digital video clock (DIG_CLK) can be configured either as an input or output for slave or master mode timing. The DIG_H and DIG_V pins provide timing and synchronization control. These pins are not required if the video source has CCIR656 timing with embedded SAV and EAV timing codes. When accepting digital video, the Bt835 controls contrast, saturation, and brightness. There is no provision for hue adjustment.

1.1.7 Output Interface

The Bt835 supports a Synchronous Pixel Interface (SPI) mode.

The SPI supports a YCrCb 4:2:2 data stream over an 8- or 16-bit wide path. When the pixel output port is configured to operate 8 bits wide, 8 bits of chrominance data are output on the first clock cycle, followed by 8 bits of luminance data on the next clock cycle for each pixel. Two clocks are required to output one pixel in this mode, and so a 2x clock is used to output the data.

The Bt835 outputs all horizontal and vertical blanking pixels, in addition to the active pixels synchronous with CLKX1 (16-bit mode) or CLKX2 (8-bit mode). It is possible to insert control codes into the pixel stream using chrominance and luminance values that are outside the allowable chroma and luma ranges. These control codes can be used to flag video events such as ACTIVE, HRESET, and VRESET. Decoding these video events downstream enables the video controller to eliminate pins required for the corresponding video control signals.

The Bt835 supports the VESA VIP interface and Conexant ByteStream interface for embedding control codes into the digital video pixel stream.

1.1.8 VBI Data Passthrough

The Bt835 provides VBI data passthrough capability. The VBI region ancillary data is captured by the video decoder and made available to the system for subsequent software processing. The Bt835 may operate in a VBI line output mode, in which the VBI data is only made available during select lines. This mode of operation enables capture of VBI lines containing ancillary data, as well as processing normal YCrCb video image data. In addition, the Bt835 supports a VBI frame output mode, in which every line in the video signal is treated as if it were a vertical interval line, and no image data is output. This mode of operation is used in still-frame capture/processing applications.

In VIP mode, the Bt835 passes VBI data raw samples. During selected VBI lines, the VIP task bit T is set. Protection bits P[3:0] are not used and are forced to 0. Ancillary data is not supported. The VIPEN bit controls this mode.

1.1.9 Closed Caption Decoding

The Bt835 provides a Closed Captioning (CC) and Extended Data Services (EDS) decoder. Data presented to the video decoder on the CC and EDS lines is decoded and made available to the system through the CC_DATA and CCSTATUS registers.

1.1.10 Two Wire Serial Bus Interface

The Bt835 registers are accessed via a two-wire serial bus interface. The Bt835 operates as a slave device. Serial clock and data lines SIC and SID transfer data from the bus master at a maximum rate of 100 kbps. Chip select and reset signals are available to select one of two possible Bt835 devices in the same system, and to set the registers to their default values.

1.1.11 3.3 V/5 V Operation

The Bt835 interfaces to either 5 V or 3.3 V signal level graphics/system controllers. When in 5 V mode, all power pins should be tied to +5 V levels. LVTTL must also be tied to +5 V.

When in 3.3 V mode, the digital inputs/outputs are not 5 V tolerant, they can only interface to 3.3 V signal levels (this includes the serial interface pins). When in 3.3 V mode, all VDD, VPP, and VDDO pins must be tied to 3.3 V, all VAA pins must be tied to +5 V (for ADC biasing). LVTTL must be tied to ground.

1.2 Pin Descriptions

Figure 1-2 illustrates the Bt835 pinout. Table 1-2 provides pin numbers, names, input and output functions, and descriptions.

Figure 1-2. Bt835 Pinout

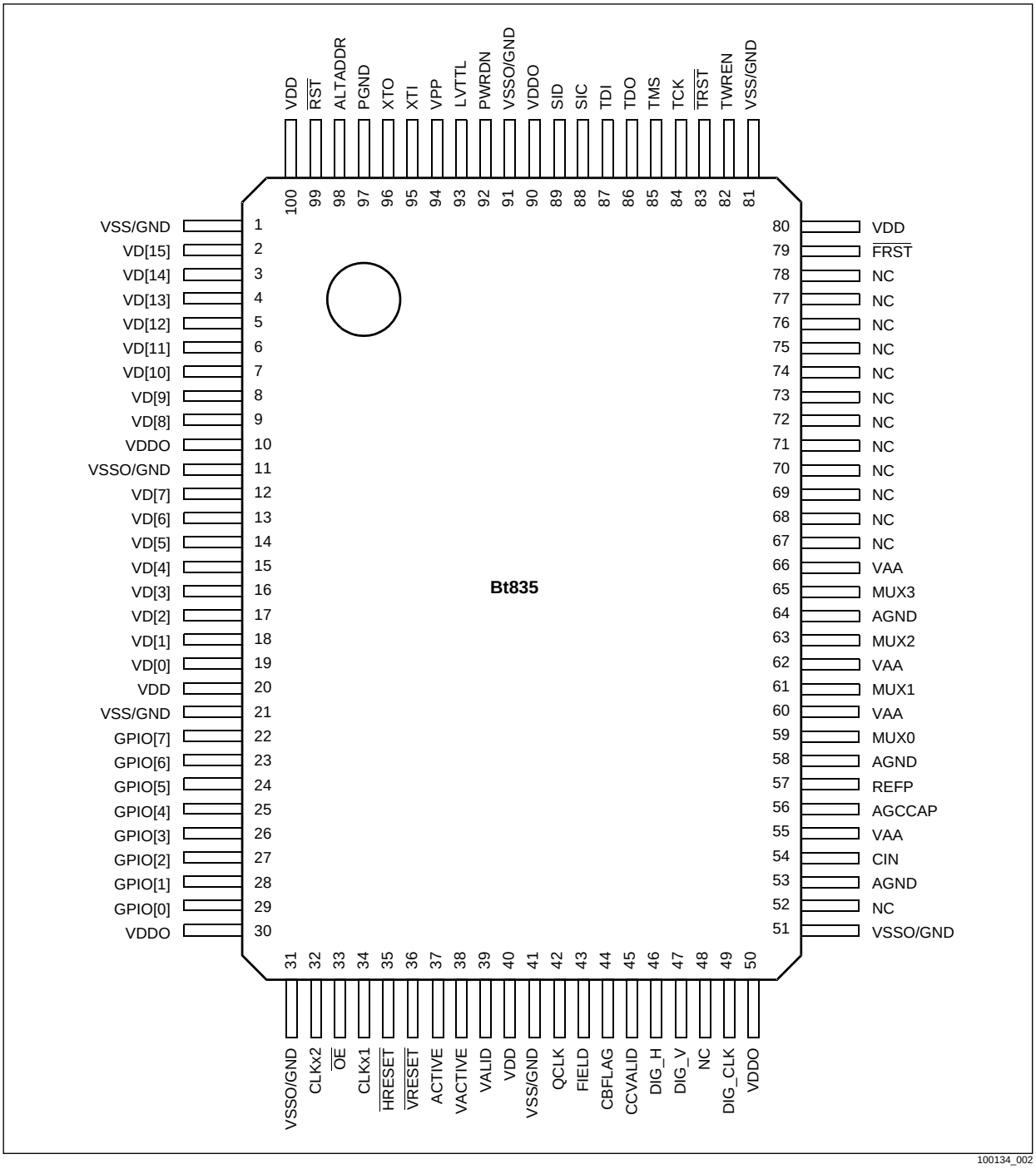


Table 1-2. Bt835 Pin Descriptions *(1 of 2)*

Pin #	I/O	Pin Name	Description
2–9	O	VD[15:8]	In 16-bit output mode, these pins represent the luma portion of the decoded video signal. In 8-bit output mode, these pins are the 4:2:2 multiplexed data stream. In test mode, these pins may be configured to be the test bus output.
12–19	I/O	VD[7:0]	In 16-bit mode, these pins represent the multiplexed Cr/Cb portion of the decoded video signal. In 8-bit mode, these pins are three-stated. When in 8-bit mode, these pins may be used to input digital video. In test mode, these pins are used as the test bus input.
22–29	I/O	GPIO[7:0]	These pins control, or sample, external devices. These pins power up three-stated.
32	O	CLKx2	ADC sample clock output.
33	I	$\overline{OE}$	Active low output enable. When pulled high, this pin will three-state the pins defined by the OES[1:0] register bits. This pin works in conjunction with the NOUTEN register bit. When either NOE or NOUTEN is high, the selected pins are three-stated.
34	O	CLKx1	ADC sample clock, divided by two.
35	O	$\overline{HRESET}$	Active low. Horizontal reset output.
36	O	$\overline{VRESET}$	Active low. Vertical reset output.
37	O	ACTIVE	Composite active video region. Indicates non-blanked region of decoded video. May be configured to represent the horizontal active region of each line.
38	O	VACTIVE	Vertical active output. Indicates the non-blanked vertical region of the decoded video.
39	O	VALID	Valid pixel output. This signal, in conjunction with ACTIVE, indicates which pixels are used in the construction of the decoded video field/frame. May be internally and logically ANDED with the ACTIVE pin.
42	O	QCLK	Gated output clock. In 16-bit mode, this pin is created by inverting and gating the CLKX1 clock. In 8-bit mode, the CLKx2 clock is used.
43	O	FIELD	Even Field indicator.
44	O	CBFLAG	Cb pixel indicator.
45	O	CCVALID	Open drain output. Indicates that the CC FIFO has CC data to be read. If used, must be externally pulled up.
46	I	DIG_H	Digital video horizontal reset input. Can be tied high/low if not used.
47	I	DIG_V	Digital video vertical reset input. Can be tied high/low if not used.
49	I/O	DIG_CLK	Digital video clock. May be configured as either input or output. Bidirectional. Do not tie if not used.
79	I	$\overline{FRST}$	Active LOW FIFO reset. Used for testing purposes only. JTAG. Tie high for normal use.
82	I	TWREN	FIFO test-write input. JTAG pin. Tie low for normal use.
83	I	$\overline{TRST}$	Active low. JTAG reset. Tie low for normal use.
84	I	TCK	JTAG clock. Tie low for normal use.
85	I	TMS	JTAG test mode select. Tie high for normal use.
86	O	TDO	JTAG test data out. Do not connect this pin for normal use.

Table 1-2. Bt835 Pin Descriptions *(2 of 2)*

Pin #	I/O	Pin Name	Description
87	I	TDI	JTAG test data in. Tie high for normal use.
88	I	SIC	Serial interface clock.
89	I/O	SID	Serial interface data. Open drain I/O. Must be externally pulled up, typically with a 10 kΩ resistor.
92	I	PWRDN	Powers down the decoder when high.
93	I	LVTTL	When connected to ground, configures the Bt835 to operate at 3.3 V. When connected to VDD, configures the Bt835 to operate at 5 V.
95	I	XTI	Crystal in.
96	I	XTO	Crystal out.
98	I	ALTADDR	Used to select alternate serial interface address. High = 0x8A; low = 0x88.
99	I	$\overline{\text{RST}}$	When low, resets the Bt835. Internal pullup.
20, 40, 80, 100	P	VDD	Core power. Can be connected to 3.3 V or 5 V.
1, 21, 41, 81	G	VSS	Core ground. Must be connected to ground.
10, 30, 50, 90	P	VDDO	Pad ring power.
11, 31, 51, 91	G	VSSO/GND	Pad ring ground.
94	P	VPP	PLL power.
97	G	PGND	PLL ground.
55, 60, 62, 66	P	VAA	Analog power. Must always be connected to 5 V.
53, 58, 64	G	AGND	Analog ground. Must always be connected to ground.
54	I	CIN	The analog chroma input to the C-ADC.
57	I	REFP	The top of the ADC reference must be connected to a 0.1 µF input capacitor to ground.
56	I	AGCCAP	The AGC time-constant control. Must be connected to a 0.1 µF capacitor to ground.
59, 61, 63, 65	I	MUX[3:0]	Analog composite video inputs to the on-chip input multiplexer. They are used to select between four composite sources or three composite and one S-Video source. Unused pins should be connected to GND.

1.3 UltraLock

1.3.1 The Challenge

The line length (the interval between the midpoints of the falling edges of succeeding horizontal sync pulses) of analog video sources is not constant. For a stable source such as a studio grade video source or test signal generators, this variation is very small (±2 ns). For an unstable source such as a VCR, laser disk player, or TV tuner, line length variation can be a few microseconds.

Despite these variations, digital display systems require a fixed number of pixels per line. The Bt835 employs the UltraLock technique to lock to the horizontal sync and the subcarrier of the incoming analog video signal, and generate the required number of pixels per line.

1.3.2 Operation Principles of UltraLock

UltraLock is based on sampling, using a fixed-frequency stable clock. Because the video line length varies, the number of samples generated using a fixed-frequency sample clock also varies from line to line. If the number of generated samples per line is always greater than the number of samples per line required by the particular video format, the number of acquired samples can be reduced to fit the required number of pixels per line.

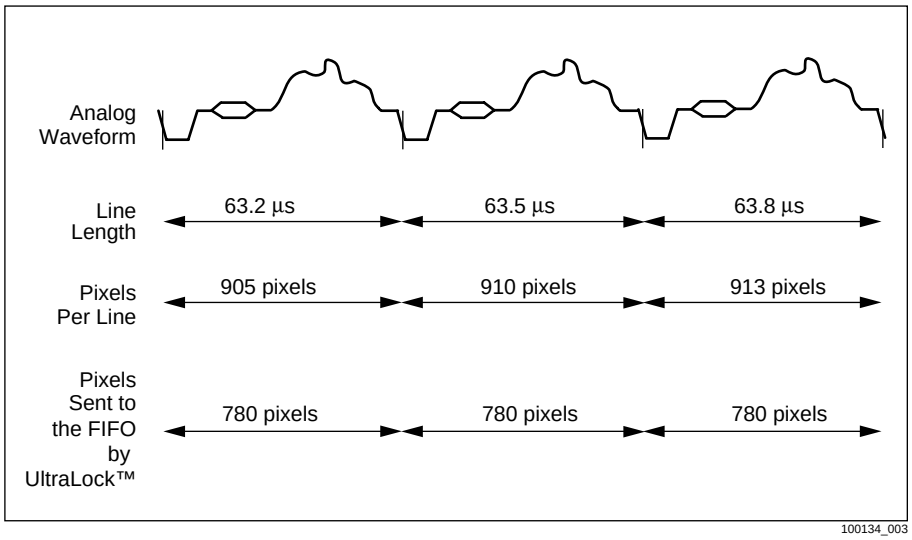
The Bt835 PLL generates a 8*Fsc (28.64 MHz for NTSC and 35.47 MHz for PAL) clock from a crystal or oscillator input signal source. The 8*Fsc clock signal, or CLKx2, is divided down to CLKx1 internally (14.32 MHz for NTSC and 17.73 MHz for PAL). Both CLKx2 and CLKx1 are provided to the system. UltraLock operates at CLKx1, although the input waveform is sampled at CLKx2, then low-pass filtered, and decimated to a CLKx1 sample rate.

A 4*Fsc (CLKx1) sample rate produces 910 pixels for NTSC and 1,135 pixels for PAL/SECAM within a nominal line time interval (63.5 ms for NTSC and 64 ms for PAL/SECAM). Square pixel NTSC and PAL/SECAM formats should produce only 780 and 944 pixels per video line, respectively. This is because the square pixel clock rates are slower than a 4*Fsc clock rate; i.e., 12.27 MHz for NTSC, and 14.75 MHz for PAL.

UltraLock accommodates line length variations from nominal time line intervals in the incoming video by always acquiring more samples (at an effective 4*Fsc rate) than the particular video format requires. UltraLock interpolates to the required number of pixels so that it maintains the stability of the original image, despite variation in the line length of the incoming analog waveform.

Figure 1-3 illustrates three successive lines of video being decoded for square pixel NTSC output. The first line is shorter than the nominal NTSC line time interval of 63.5 ms. On this first line, a line time of 63.2 ms sampled at 4*Fsc (14.32 MHz) generates only 905 pixels. The second line matches the nominal line time of 63.5 ms and provides the expected 910 pixels. Finally, the third line is too long at 63.8 µs, within which 913 pixels are generated. In all three cases, UltraLock outputs only 780 pixels.

Figure 1-3. UltraLock Behavior for NTSC Square Pixel Output



UltraLock can be used to extract any programmable number of pixels from the original video stream, as long as the sum of the nominal pixel line length, 910 for NTSC and 1,135 for PAL/SECAM, and the worst case line length variation in the active region is greater than or equal to the required number of output pixels per line, i.e.,

$$P_{Nom} + P_{Var} \geq P_{Desired}$$

where: P_{Nom} = Nominal number of pixels per line at 4*Fsc sample rate (910 for NTSC, 1,135 for PAL/SECAM)

P_{Var} = Variation of pixel count from nominal at 4*Fsc (can be a positive or negative number)

$P_{Desired}$ = Desired number of output pixels per line

NOTE: For stable inputs, UltraLock guarantees the time between the falling edges of HRESET to within only one pixel. UltraLock guarantees the number of active pixels in a line, as long as the above relationship holds.

1.4 Composite Video Input Formats

The Bt835 supports all composite video input formats. Table 1-3 shows the different video formats and shows some of the countries in which each format is used.

Table 1-3. Video Input Formats Supported by the Bt835

Format	Lines	Fields	F_{SC}	Country
NTSC-M	525	60	3.58 MHz	U.S., many others
NTSC-Japan(1)	525	60	3.58 MHz	Japan
PAL-B	625	50	4.43 MHz	Many
PAL-D	625	50	4.43 MHz	China
PAL-G	625	50	4.43 MHz	Many
PAL-H	625	50	4.43 MHz	Belgium
PAL-I	625	50	4.43 MHz	Great Britain, others
PAL-M	525	60	3.58 MHz	Brazil
PAL-N	625	50	4.43 MHz	Paraguay, Uruguay
PAL-N combination	625	50	3.58 MHz	Argentina
SECAM	625	50	4.406 MHz 4.250 MHz	Eastern Europe, France, Middle East
PAL–60(2)	525	60	4.43 MHz	China
NTSC(4.43)	525	60	4.43 MHz	Transcoding Application

NOTE(S):
(1) NTSC-Japan has 0 IRE setup.
(2) Typically used in Chinese Video CD players.

The video decoder must be appropriately programmed for each of the composite video input formats. Table 1-4 lists the register values that need to be programmed for each input format.

Table 1-4. Register Values for Video Input Formats

Register	Bit	NTSC-M	NTSC-Japan	PAL-B, D, G, H, I	PAL-M	PAL-N	PAL-N Combination	PAL-60	SECAM	NTSC 4.43
INPUT (0x01)	FMT[3:0]	0001	0010	0100	0101	0110	0111	1000	1001	0011
Cropping: HDELAY, VDELAY, VACTIVE, CROP	7:0 in all 5 registers	Set to desired cropping values in registers	Set to NTSC-M square pixel values	Set to desired cropping values in registers	Set to NTSC-M square pixel values	Set to PAL-B, D, G, H, I square pixel values	Set to PAL-B, D, G, H, square pixels values	Set to PAL-B, D, G, H, I square pixel values	Set to PAL-B, D, G, H, I square pixel values	Set to NTSC-M square pixel values
HSCALE (0x0A, 0x0B)	15:0	0x02AA	0x02AA	0x033C	0x02AA	0x033C	0x00F8	0x02AA	0x033C	0x02AA
ADELAY (0x1A)	7:0	0x68	0x68	0x7F	0x68	0x7F	0x7F	0x68	0x7F	0x68
BDELAY (0x1B)	7:0	0x5D	0x5D	0x72	0x5D	0x72	0x72	0x5D	0xA0	0x5D

1.5 Y/C Separation and Chroma Demodulation

Y/C separation and chroma decoding are handled as illustrated in Figures 1-4 and 1-5. A 3-line adaptive comb filter separates luminance and chrominance for NTSC video. A notch/band-pass filter is used for PAL/SECAM video. Figure 1-6 illustrates the filter responses. The optional chroma comb filter, when using the notch filter, is implemented in the vertical scaling block. Refer to Section 1.6 on Video Scaling, Cropping, and Temporal Decimation.

Figure 1-4. Y/C Separation and Chroma Demodulation for Composite NTSC Video

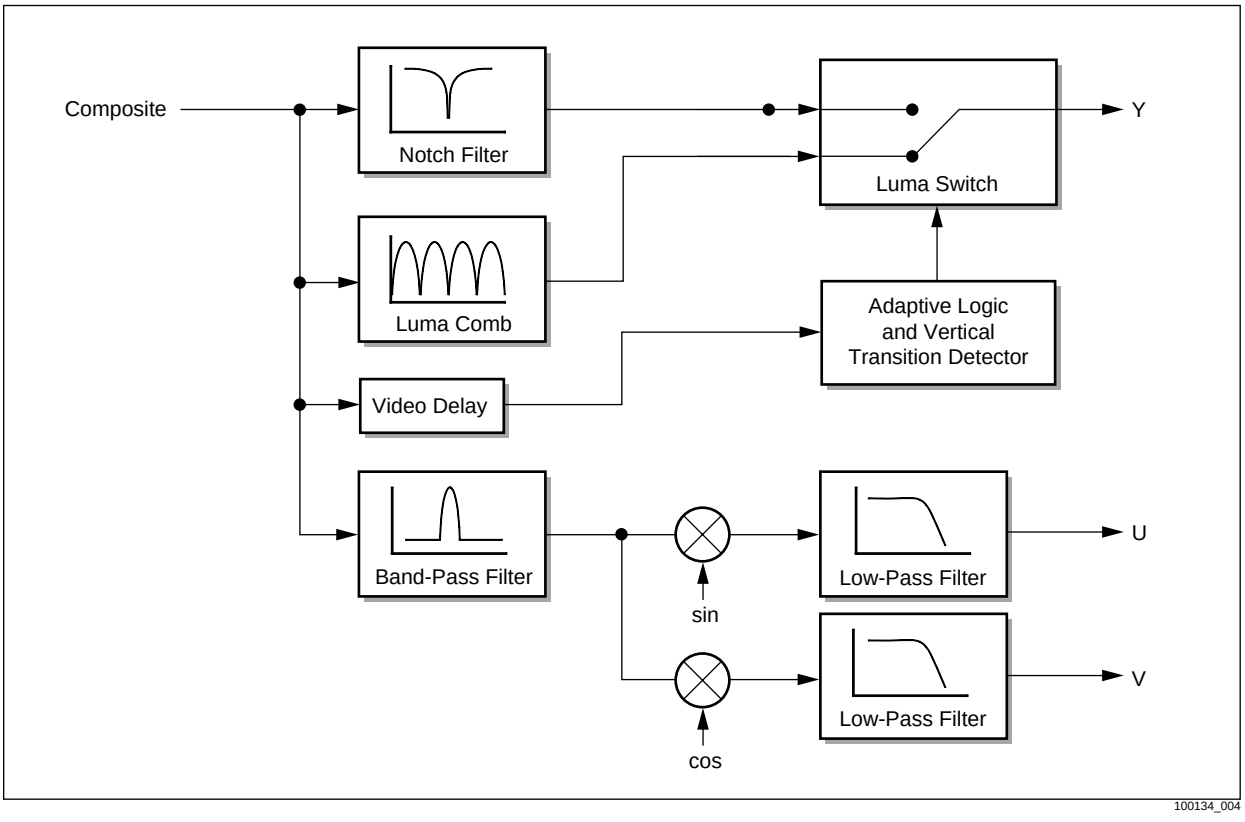


Figure 1-5. Y/C Separation and Chroma Demodulation for Composite PAL Video

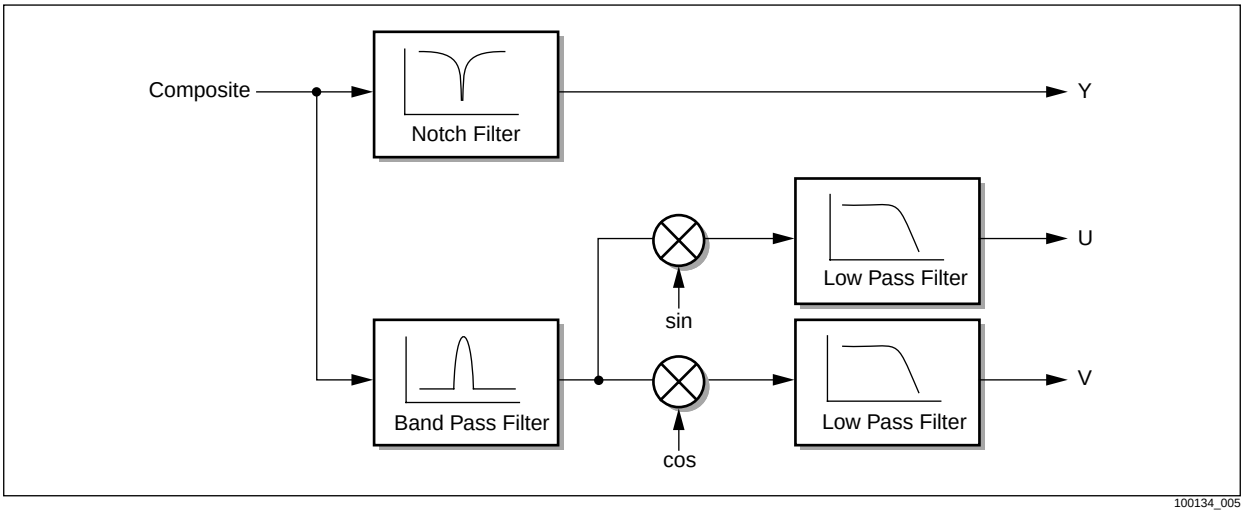


Figure 1-6. NTSC and PAL/SECAM Y/C Separation Filter Responses

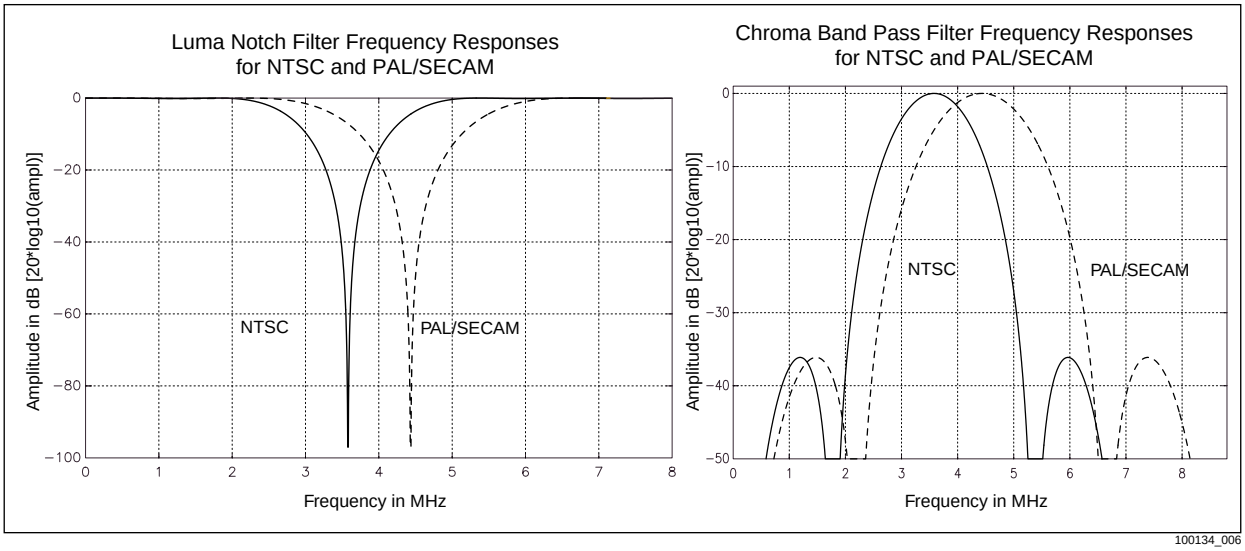


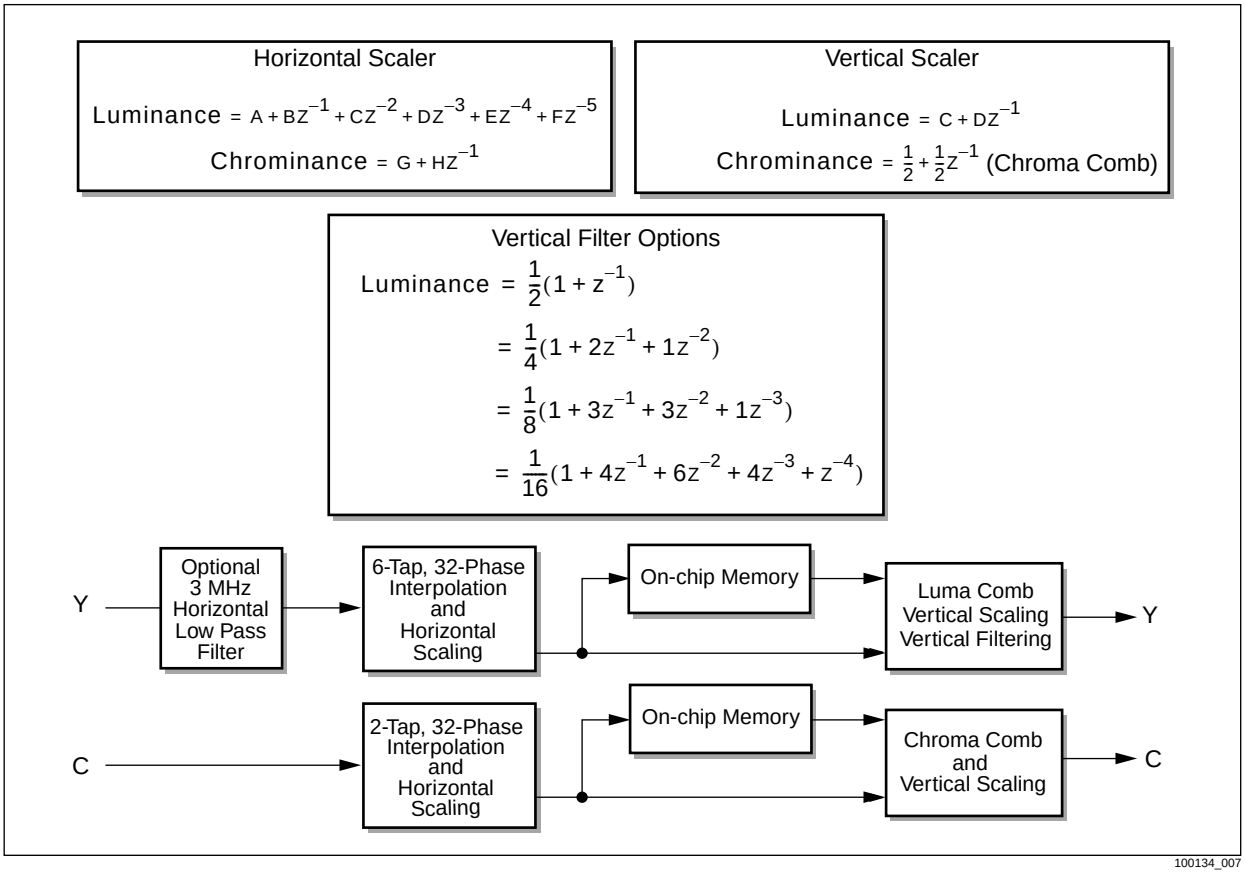
Figure 1-7 illustrates the filtering and scaling operations.

In addition to the Y/C separation and chroma demodulation illustrated in Figure 1-5, the Bt835 also supports chrominance comb filtering as an optional filtering stage after chroma demodulation. The chroma demodulation generates baseband I and Q (NTSC) or U and V (PAL/SECAM) color difference signals.

For S-Video operation, the digitized luma data bypasses the Y/C separation block completely, and the digitized chrominance passes directly to the chroma demodulator.

For monochrome operation, the Y/C separation block is also bypassed, and the saturation registers (SAT_U and SAT_V) are set to zero.

Figure 1-7. Filtering and Scaling



1.6 Video Scaling, Cropping, and Temporal Decimation

The Bt835 provides three mechanisms to reduce the amount of video pixel data in its output stream: down-scaling, cropping, and temporal decimation. All three can be controlled independently.

1.6.1 Horizontal and Vertical Scaling

The Bt835 provides independent and arbitrary horizontal and vertical down-scaling. The maximum scaling ratio is 16:1 in both X and Y dimensions. The maximum vertical scaling ratio is reduced from 16:1 when using frames to 8:1. The following sections describe the different methods used for scaling luminance and chrominance.

1.6.2 Luminance Scaling

The first stage in horizontal luminance scaling is an optional pre-filter that provides the capability to reduce anti-aliasing artifacts. It is generally desirable to limit the bandwidth of the luminance spectrum prior to performing horizontal scaling. This is because the scaling of high-frequency components may create image artifacts in the resized image. The optional low-pass filters illustrated in Figure 1-8 reduce the horizontal high-frequency spectrum in the luminance signal. Figures 1-9 and 1-10 illustrate the combined results of the optional low-pass filters, and the luma notch and 2x oversampling filter.

Figure 1-8. Optional Horizontal Luma Low-Pass Filter Responses

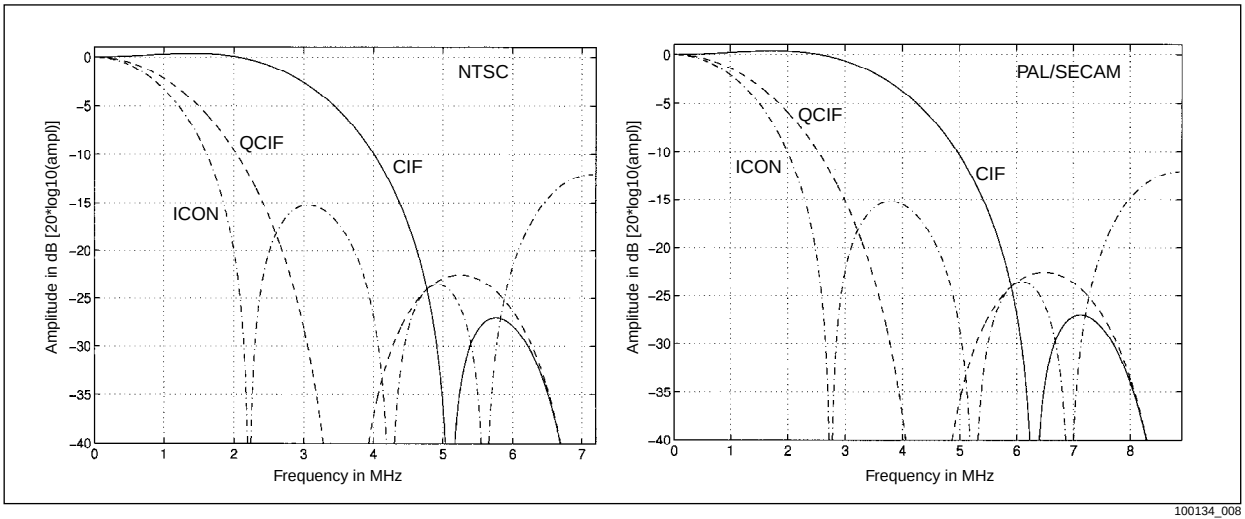


Figure 1-9. Combined Luma Notch, 2x Oversampling and Optional Low-Pass Filter Response (NTSC)

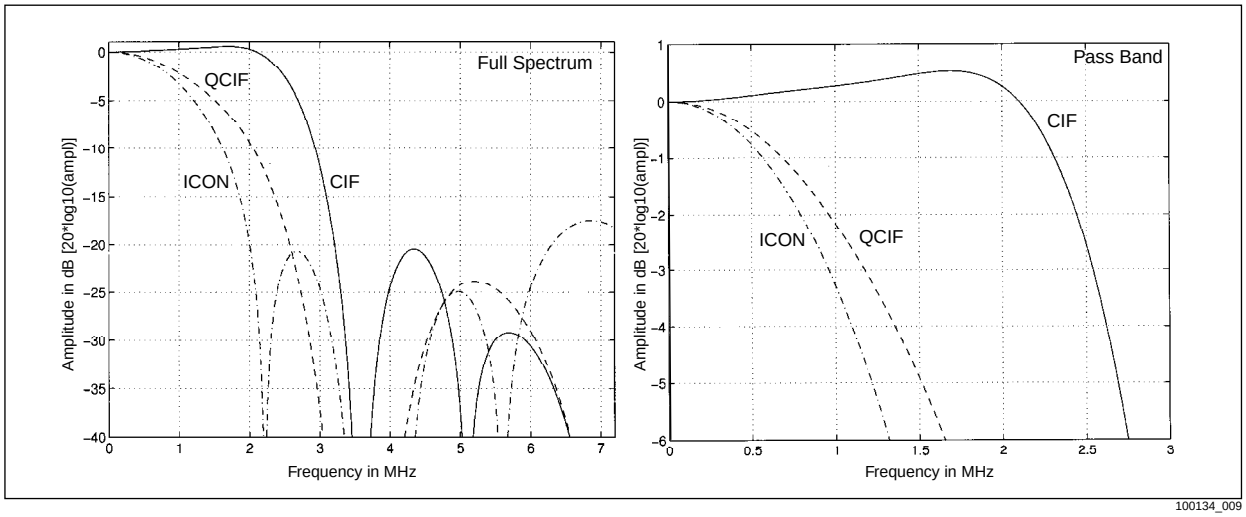
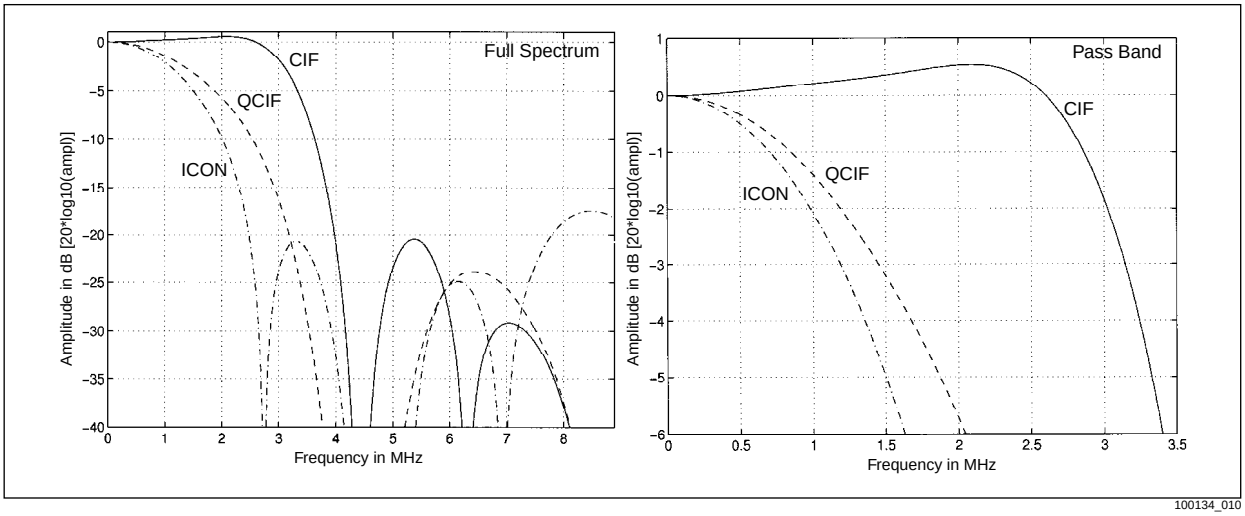


Figure 1-10. Combined Luma Notch, 2x Oversampling and Optional Low-Pass Filter Response (PAL/SECAM)



The Bt835 implements horizontal scaling through poly-phase interpolation. The Bt835 uses 32 different phases to accurately interpolate the value of a pixel. This provides an effective pixel jitter of less than 6 ns.

In simple pixel- and line-dropping algorithms, non-integer scaling ratios introduce a step function in the video signal that effectively introduces high-frequency spectral components. Poly-phase interpolation accurately interpolates to the correct pixel and line position, providing more accurate information. This results in more aesthetically pleasing video, as well as higher compression ratios in bandwidth-limited applications.

For vertical scaling, the Bt835 uses a line store to implement four different filtering options. Figure 1-11 illustrates the filter characteristics. The Bt835 provides up to 5-tap filtering to ensure removal of aliasing artifacts. Figure 1-12 illustrates the combined responses of the luma notch and 2x oversampling filters.

Figure 1-11. Frequency Responses for the Four Optional Vertical Luma Low-Pass Filters

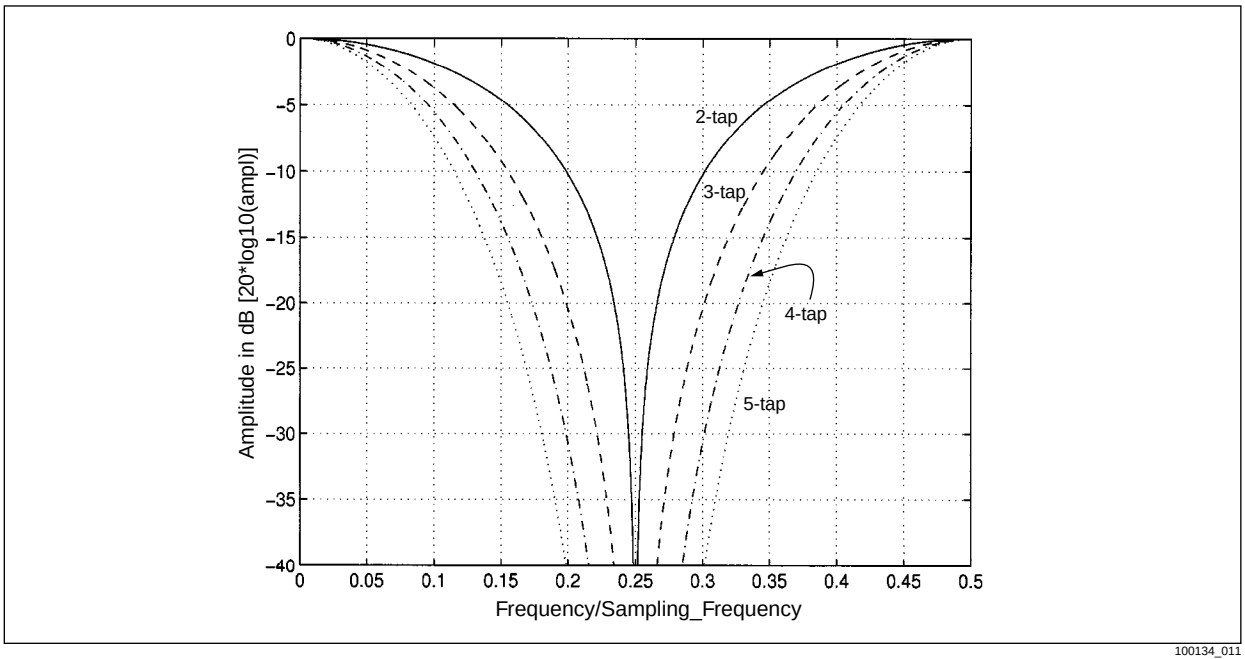
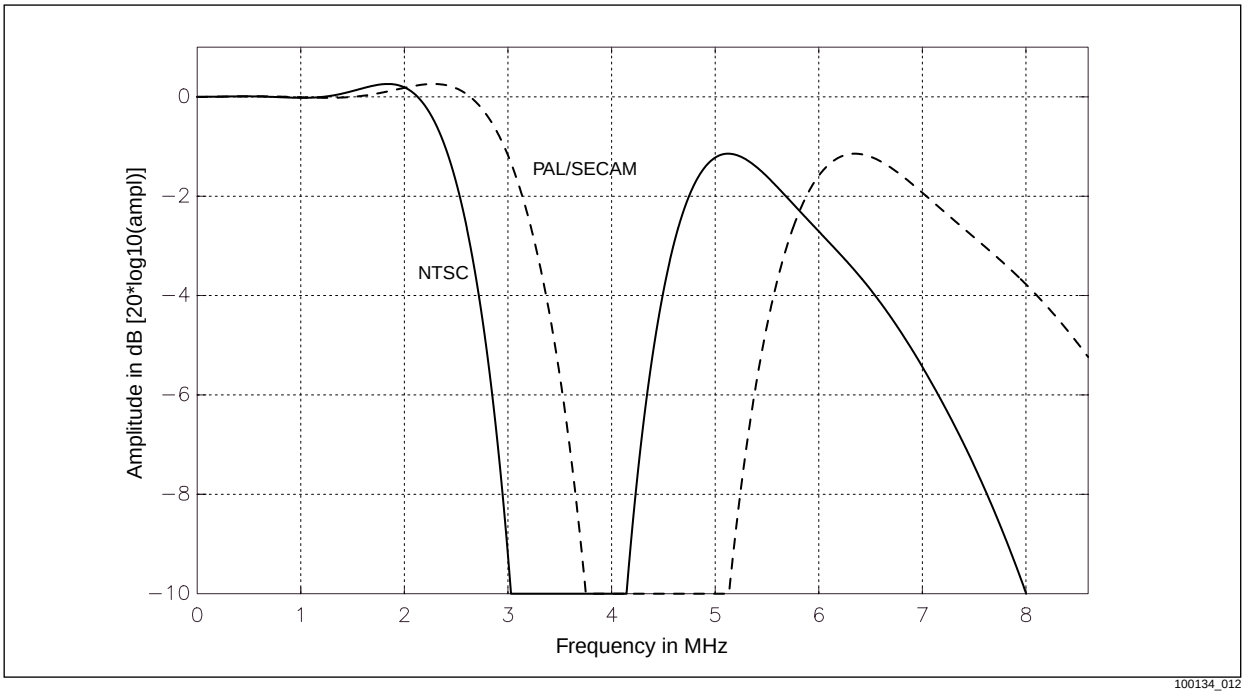


Figure 1-12. Combined Luma Notch and 2x Oversampling Filter Response



1.6.3 Peaking

The Bt835 enables four different peaking levels by programming the PSEL[1:0] bits in the CONTROL_0 register. Figures 1-13 and 1-14 illustrate the filter responses.

Figure 1-13. NTSC Peaking Filters

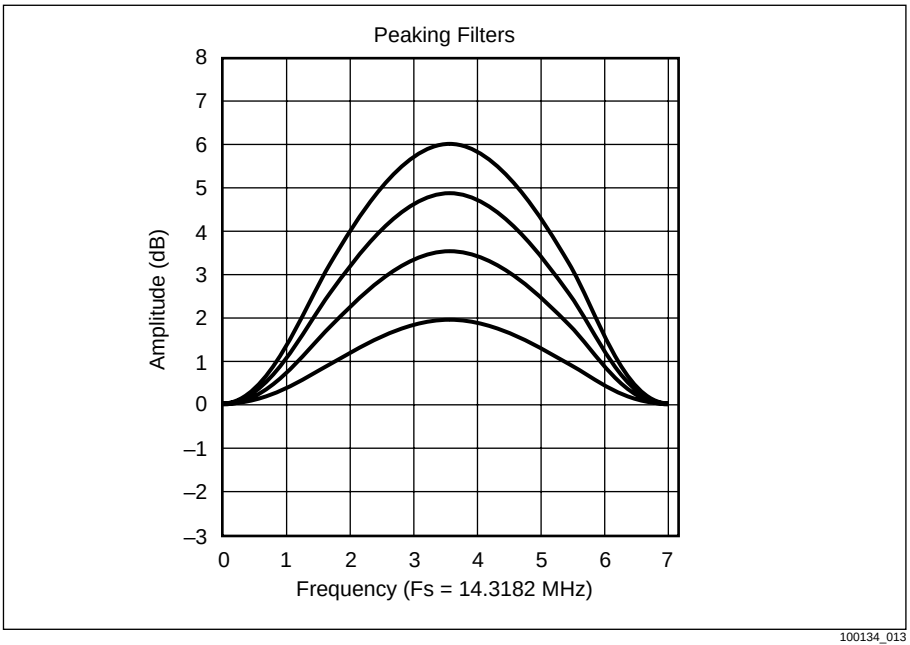
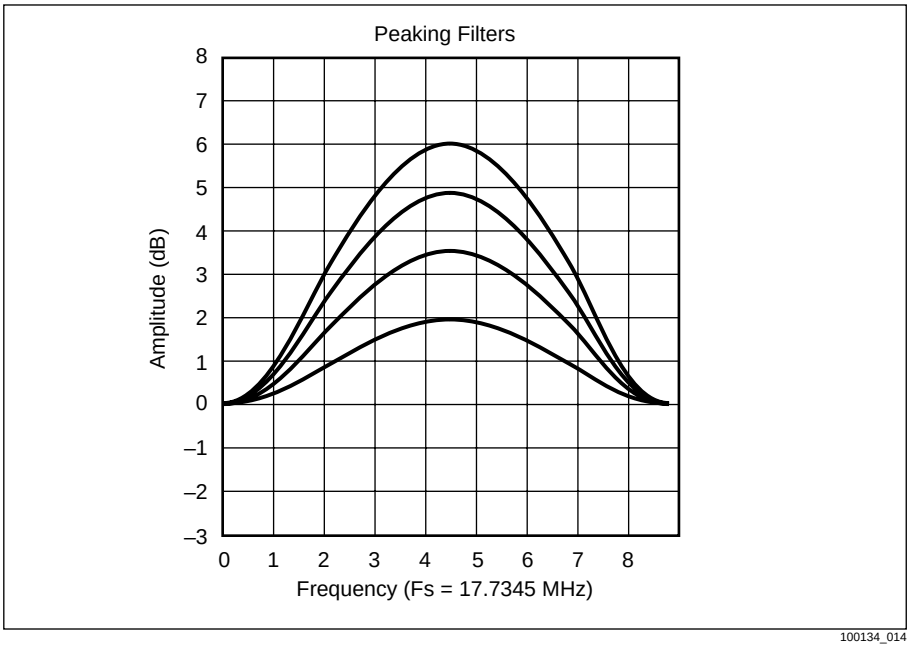


Figure 1-14. PAL/SECAM Peaking Filters



The number of taps in the vertical filter is set by the VSCALE_CTL register. The user may select 2, 3, 4, or 5 taps. The number of taps must be chosen in conjunction with the horizontal scale factor. As the scaling ratio increases, the number of taps available for vertical scaling increases. In addition to low-pass filtering, vertical interpolation is also employed to minimize artifacts when scaling to non-integer scaling ratios (refer to Table 1-5).

Table 1-5. Filter Tap Selection

Resolution	VFILT Tap to Use
Full to 1/2	2
1/2 to 1/4	3(1)
1/4 to 1/8	4(1)
1/8 to 0	5(1)

NOTE(S):
(1) For resolution below 1/2 of full resolution the value added by using the comb filter is lost due to the small image and must be turned off to provide additional buffer space for the larger filter taps.

1.6.4 Chrominance Scaling

A 2-tap, 32-phase interpolation filter is used for horizontal scaling of chrominance. Vertical scaling of chrominance is implemented through chrominance comb filtering using a line store, followed by simple decimation or line dropping.

1.6.5 Scaling Registers

Horizontal Scaling Ratio Register (HSCALE)

HSCALE is programmed with the horizontal scaling ratio. When outputting unscaled video (in NTSC), the Bt835 produces 910 pixels per line. This corresponds to the pixel rate at fCLKx1 (4*Fsc). This register is the control for scaling the video to the desired size. For example, square pixel NTSC requires 780 samples per line, while CCIR601 requires 858 samples per line. HSCALE_HI and HSCALE_LO are two 8-bit registers that, when concatenated, form the 16-bit HSCALE register.

The method below uses pixel ratios to determine the scaling ratio. This is commonly used when re-encoding, such as with set top box applications. The following formula is used to determine the scaling ratio to be entered into the 16-bit register:

$$\text{NTSC:} \quad \text{HSCALE} = [\,(910/P_{desired}) - 1] * 4096$$
$$\text{PAL/SECAM:} \quad \text{HSCALE} = [\,(1135/P_{desired}) - 1] * 4096$$

where: $P_{desired}$ = Desired number of pixels per line of video, including active, sync, and blanking.

For example, to scale PAL/SECAM input to square pixel QCIF, the total number of horizontal pixels is 236:

$$\begin{aligned} HSCALE &= [\,(\,1135/236\,) - 1\,] * 4096 \\ &= 15602 \\ &= 0x3CF2 \end{aligned}$$

An alternative method for determining the HSCALE value, which is useful when attempting to fit the active image to a given window size, uses the ratio of the scaled active region to the unscaled active region, as shown below:

$$\begin{aligned} &\text{NTSC:} && HSCALE = [\,(754 / HACTIVE) - 1\,] * 4096 \\ &\text{PAL/SECAM:} && HSCALE = [\,(922 / HACTIVE) - 1\,] * 4096 \end{aligned}$$

where: *HACTIVE* = Desired number of pixels per line of video, not including sync or blanking. Maximum value is 768.

In this equation, the HACTIVE value cannot be cropped; it represents the total active region of the video line. This equation produces roughly the same result as using the full line length ratio shown in the first example. However, due to truncation, the HSCALE values determined using the active pixel ratio will be slightly different than those obtained using the total line length pixel ratio. The values in Table 1-6 were calculated using the full line length ratio.

Table 1-6. Scaling Ratios for Popular Formats Using Frequency Values

Scaling Ratio	Format	Total Resolution (including sync and blanking interval)	Output Resolution (Active Pixels)	HSCALE Register Values	VSCALE Register Values	
					Use Both Fields	Single Field
Full Resolution 1:1	NTSC SQ Pixel	780 x 525	640 x 480	02aa	0000	1E00
	NTSC CCIR601	858 x 525	720 x 480	00F8	0000	1E00
	PAL CCIR601	864 x 625	720 x 576	0504	0000	1E00
	PAL SQ Pixel	944 x 625	768 x 576	033C	0000	1E00
CIF 2:1	NTSC SQ Pixel	390 x 262	320 x 240	1555	1E00	1A00
	NTSC CCIR601	429 x 262	360 x 240	11F0	1E00	1A00
	PAL CCIR601	432 x 312	360 x 288	1A09	1E00	1A00
	PAL SQ Pixel	472 x 312	384 x 288	1677	1E00	1A00
QCIF 4:1	NTSC SQ Pixel	195 x 131	160 x 120	3AAA	1A00	1200
	NTSC CCIR601	214 x 131	180 x 120	3409	1A00	1200
	PAL CCIR601	216 x 156	180 x 144	4412	1A00	1200
	PAL SQ Pixel	236 x 156	192 x 144	3CF2	1A00	1200
ICON 8:1	NTSC SQ Pixel	97 x 65	80 x 60	861A	1200	0200
	NTSC CCIR601	107 x 65	90 x 60	7813	1200	0200
	PAL CCIR601	108 x 78	90 x 72	9825	1200	0200
	PAL SQ Pixel	118 x 78	96 x 72	89E5	1200	0200

NOTE(S):
1. PAL-M–HSCALE and VSCALE register values should be the same for NTSC.
2. SECAM–HSCALE and VSCALE register values should be the same as for PAL.

Vertical Scaling Ratio Register (VSCALE)

VSCALE is programmed with the vertical scaling ratio. It defines the number of vertical lines output by the Bt835. The following formula should be used to determine the value to be entered into this 13-bit register. The loaded value is a two's-complement, negative value.

$$VSCALE = (0x10000 - \{ [(scaling\_ratio) - 1] * 512 \}) \& 0x1FFF$$

For example, to scale PAL/SECAM input to square pixel QCIF, the total number of vertical lines for PAL square pixel is 156 (see Table 1-6).

$$VSCALE = (0x10000 - \{ [(4/1) - 1] * 512 \}) \& 0x1FFF$$
$$= 0x1A00$$

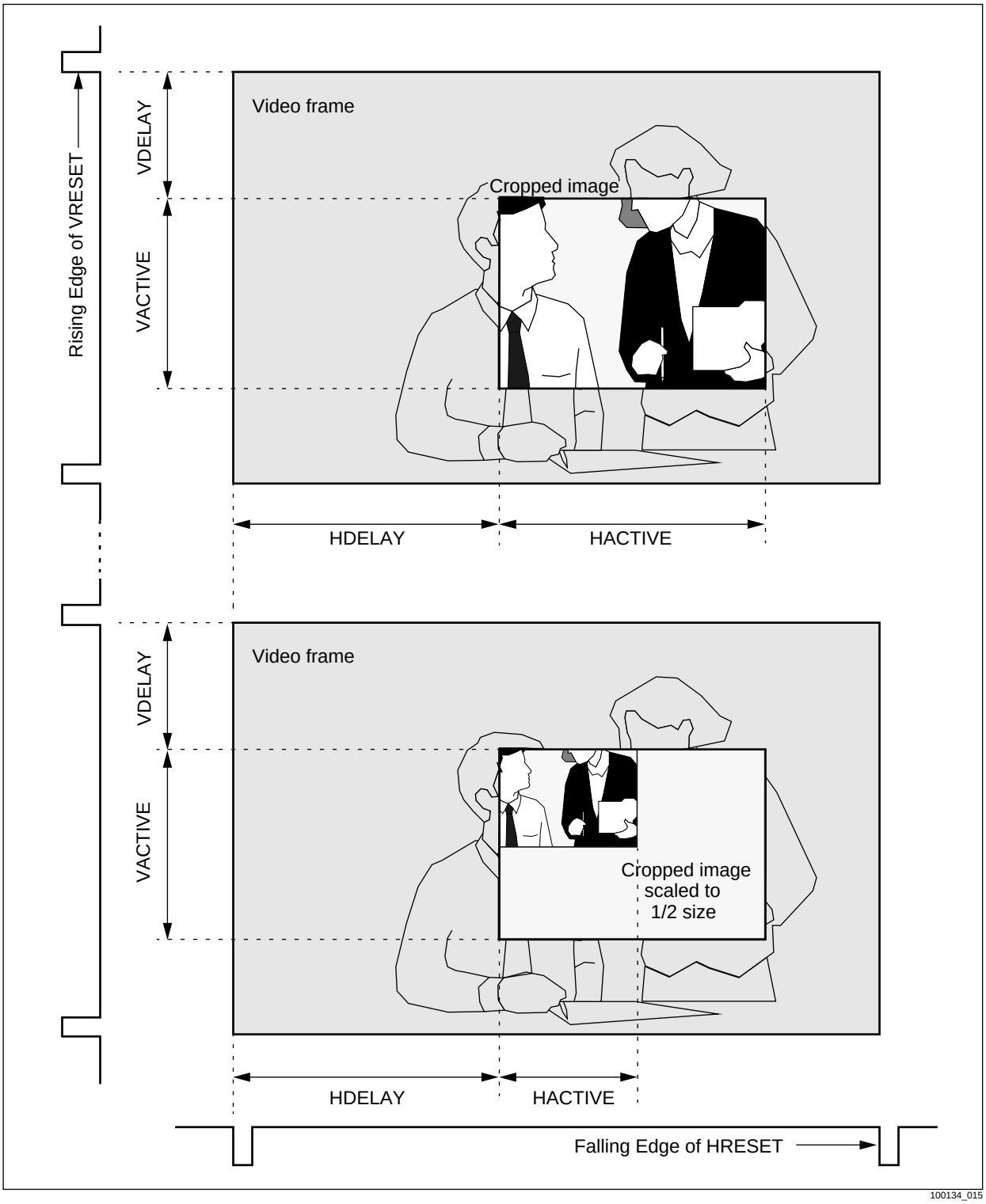
NOTE: Only the 13 least significant bits of the VSCALE value are used. The user must take care not to alter the values of the three most significant bits when writing a vertical scaling value.

When vertical scaling (below CIF resolution), it may be useful to use a single field, as opposed to using both fields. Using a single field ensures that no inter-field motion artifacts occur on the scaled output. When performing single field scaling, the vertical scaling ratio is twice as large as when scaling with both fields. For example, CIF scaling from one field does not require any vertical scaling, but when scaling from both fields, the scaling ratio is 50%. The non-interlaced bit should be reset when scaling from a single field (NVINT = 0 in the VSCALE_CTL register). Table 1-6 lists scaling ratios for various video formats and the register values required.

1.6.6 Image Cropping

Cropping enables the user to output any subsection of the video image. The ACTIVE flag can be programmed to start and stop at any position on the video frame as illustrated in Figure 1-15. The start of the active area in the vertical direction is referenced to VRESET (beginning of a new field). In the horizontal direction, it is referenced to HRESET (beginning of a new line). The dimensions of the active video region are defined by HDELAY, HACTIVE, VDELAY, and VACTIVE. The vertical and horizontal delay values determine the position of the cropped image within a frame, while the horizontal and vertical active values set the pixel dimensions of the cropped image, as illustrated in Figure 1-15.

Figure 1-15. Effect of the Cropping and Active Registers



1.6.7 Cropping Registers

Horizontal Delay Register (HDELAY)

HDELAY is programmed with the delay between the falling edge of HRESET and the rising edge of ACTIVE. The count is programmed with respect to the scaled frequency clock. HDELAY should always be an even number.

Horizontal Active Register (HACTIVE)

HACTIVE is programmed with the actual number of active pixels per line of video. This is equivalent to the number of scaled pixels that the Bt835 should output on a line. For example, if this register contained 90, and HSCALE was programmed to down-scale by 4:1, then 90 active pixels would be output. The 90 pixels would be a 4:1 scaled image of the 360 pixels (at CLKx1), starting at count HDELAY. HACTIVE is restricted in the following manner:

$$\text{HACTIVE} + \text{HDELAY} \leq \text{Total Number of Scaled Pixels.}$$

For example, in the NTSC square pixel format, there is a total of 780 pixels, including blanking, sync and active regions. Therefore:

$$\text{HACTIVE} + \text{HDELAY} \leq 780.$$

When scaled by 2:1 for CIF, the total number of active pixels is 390. Therefore:

$$\text{HACTIVE} + \text{HDELAY} \leq 390.$$

The HDELAY register is programmed with the number of scaled pixels between HRESET and the first active pixel. Because the front porch is defined as the distance between the last active pixel and the next horizontal sync, the video line can be considered in three components: HDELAY, HACTIVE, and the front porch. Figure 1-16 illustrates the video signal regions.

Figure 1-16. Regions of the Video Signal

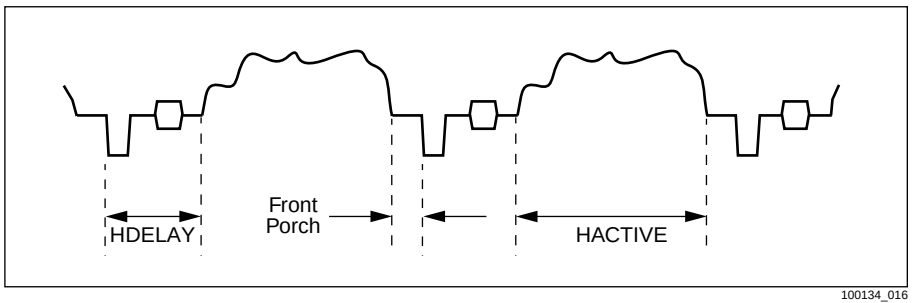


Table 1-7 shows the number of clocks at the 4x sample rate (the CLKx1 rate) when cropping is not implemented.

Table 1-7. Uncropped Clock Totals

	CLKx1 Front Porch	CLKx1 HDELAY	CLKx1 HACTIVE	CLKx1 Total
NTSC	21	135	754	910
PAL/SECAM	27	186	922	1135

The value for HDELAY is calculated using the following formula:

HDELAY = [(CLKx1_HDELAY / CLKx1_HACTIVE) * HACTIVE] & 0x3FE

CLKx1_HDELAY and CLKx1_HACTIVE are constant values, so the equation becomes:

NTSC: HDELAY = [(135 / 754) * HACTIVE] & 0x3FE

PAL/SECAM: HDELAY = [(186 / 922) * HACTIVE] & 0x3FE

In this equation, the HACTIVE value cannot be cropped.

Vertical Delay Register (VDELAY)

VDELAY is programmed with the delay between the rising edge of $\overline{\text{VRESET}}$ and the start of active video lines. It determines how many lines to skip before initiating the ACTIVE signal, and is programmed with the number of lines to skip at the beginning of a frame.

Vertical Active Register (VACTIVE)

VACTIVE is programmed with the number of lines used in the vertical scaling process. The actual number of vertical lines output from the Bt835 is equal to this register, multiplied by the vertical scaling ratio. If VSCALE is set to 0x1A00 (4:1), then the actual number of lines output is VACTIVE/4. If VSCALE is set to 0x0000 (1:1), then VACTIVE contains the actual number of vertical lines output.

NOTE: It is important to note the difference between the implementation of the horizontal registers (HSCALE, HDELAY, and HACTIVE) and the vertical registers (VSCALE, VDELAY, and VACTIVE). Horizontally, HDELAY and HACTIVE are programmed with respect to the scaled pixels defined by HSCALE. Vertically, VDELAY and VACTIVE are programmed with respect to the number of lines before scaling (before VSCALE is applied).

1.6.8 Temporal Decimation

Temporal decimation provides a solution for video synchronization during periods when full frame rate cannot be supported due to bandwidth and system restrictions.

For example, when capturing live video for storage, system limitations such as hard disk transfer rates or system bus bandwidth may limit the frame capture rate. If these restrictions limit the frame rate to 15 frames per second, the Bt835's time scaling operation enables the system to capture every other frame, instead of allowing the hard disk timing restrictions to dictate which frame to capture. This maintains an even distribution of captured frames and alleviates the jerky effects caused by systems that simply burst in data when bandwidth becomes available.

The Bt835 provides temporal decimation on either a field or frame basis. The temporal decimation register (TDEC) is loaded with a value from 1 to 60 (NTSC) or 1 to 50 (PAL/SECAM). This value represents the number of fields or frames skipped by the chip during a sequence of 60 for NTSC, or 50 for PAL/SECAM. Skipped fields and frames are considered inactive, indicated by the ACTIVE pin remaining low. Consequently, if QCLK is programmed to depend on ACTIVE, QCLK becomes inactive as well.

Examples:

TDEC = 0x02	Decimation is performed by frames. Two frames are skipped per 60 frames of video, assuming NTSC decoding. Frames 1–29 are output normally, then ACTIVE remains low for one frame. Frames 30–59 are then output, followed by another frame of inactive video.
TDEC = 0x9E	Decimation is performed by fields. Thirty fields are output per 60 fields of video, assuming NTSC decoding. This value outputs every other field, or every odd field of video, starting with field one in frame one.
TDEC = 0x01	Decimation is performed by frames. One frame is skipped per 50 frames of video, assuming PAL/SECAM decoding.
TDEC = 0x00	Decimation is not performed. Full frame rate video is output by the Bt835.

When changing programming in the temporal decimation register, 0x00 should be loaded first, and then the decimation value. This ensures the decimation counter is reset to zero. If zero is not first loaded, the decimation may start on any field or frame in the sequence of 60 (or 50 for PAL/SECAM). On power-up, this preload is not necessary because the counter is internally reset.

When decimating fields, the FLDALN bit in the TDEC register can be programmed to choose whether the decimation starts with an odd field or an even field. If the FLDALN bit is set to logical 0, the first field dropped during the decimation process will be an odd field. Conversely, setting the FLDALN bit to logical 1 causes the even field to be dropped first in the decimation process.

1.7 Video Adjustments

The Bt835 provides programmable hue, contrast, saturation, and brightness.

1.7.1 The Hue Adjust Register (HUE)

The hue adjust register is used to offset the hue of the decoded signal. In NTSC, the hue of the video signal is defined as the phase of the subcarrier with reference to the burst. The value programmed in this register is added or subtracted from the phase of the subcarrier, which effectively changes the hue of the video. The hue can be shifted by plus or minus 90 degrees. Because of the nature of PAL/SECAM encoding, hue adjustments cannot be made when decoding PAL/SECAM.

1.7.2 The Contrast Adjust Register (CONTRAST)

The contrast adjust register, also called the luma gain, provides the ability to change the contrast from approximately 0 percent to 200 percent of the original value. The decoded luma value is multiplied by the 9-bit coefficient loaded into this register.

1.7.3 The Saturation Adjust Registers (SAT_U, SAT_V)

The saturation adjust registers are additional color adjustment registers. It is a multiplicative gain of the U and V signals. The value programmed in these registers are the coefficients for the multiplication. The saturation ranges from approximately 0 percent to 200 percent of the original value.

Since U and V are offset in the analog domain, the default ratios should be maintained for proper angular decoding of color. However, when using CCIR656, there is no similar U-V offset. Since U and V are equal, the values should be equal.

1.7.4 The Brightness Register (BRIGHT)

The brightness register is simply an offset for the decoded luma value. The programmed value is added or subtracted from the original luma value, which changes the brightness of the video output. The luma output ranges from 0 to 255. Brightness adjustment can be made over a range of –128 to +127.

1.7.5 Automatic Gain Control (AGC)

The Bt835 automatically applies gain to any video signals with suppressed amplitude chroma or luma. If the video being digitized has a non-standard sync height to video height ratio, the digital code used for AGC can be changed by enabling the CRUSH (bit 0) in the ADC register (0x1C), which can then be adjusted by changing the WC_UP (0x1D) and WC_DN (0x1E) registers appropriately. AGC (and White Crush) can be disabled by setting the AGC_EN (bit 4 of ADC register 0x1C) to a 1. When this is done, the ADC must have an external reference supplied to pin 57, REFP. White Crush will not function in this mode.

1.7.6 White Crush

1.7.6.1 Overview

Standard AGC techniques utilize the amplitude of the sync tip to set the gain of the video system. If the sync tip to video ratio is not proportional, the AGC will apply an incorrect gain to the video signal, resulting in a display that is either too dark or too bright. The White Crush function compensates for video signals that do not maintain proper sync tip to white ratios.

1.7.6.2 Comparison of AGC

Conexant video decoders have two stages of AGC, used to equalize the incoming video to a standard amplitude. This is done to accommodate variations due to uncalibrated sources, losses due to long cables, and tuner conversion inefficiencies. The video decoder bases its equalization process on the assumption that the signal is proportional, measuring the height of the sync tip, then increasing the gain of the entire signal until the sync tip is at a nominal amplitude of 40 IRE. This rescales the black to white amplitude to the proper levels.

The first level of AGC compares the decoded back porch value to a nominal value. A change in the reference ladder is made (based on this comparison), to bring the decoded back porch in line with the nominal. This is the most common form of AGC and is found in most decoder systems.

1.7.6.3 White Crush

There is a drawback to the standard AGC method. The incoming signal may not maintain a proper video-to-sync ratio. An AGC based solely on back porch could yield a signal that is either too dark or too bright. To address this problem, a secondary circuit known as White Crush can be used which senses the occurrence of pixels over a nominal range. At the end of a field or frame where these pixels are detected, a value is added to the back porch, which lowers the expected back porch. This compensates for an attenuated sync tip. To ensure that the picture does not become too dark, it is necessary to provide a means of raising the expected back porch value. To do this, the decoder examines the value of every pixel in the active region. If the majority of the pixels are below a user-selected value, the image is deemed to be too dark, and the back porch is raised.

1.7.6.4 The Solution

The White Crush circuitry examines the decoded video signal to determine if the sync tip ratio is incorrect. If a sync tip is reduced, the resulting video signals will saturate the ADC, resulting in overflows. If a sync tip is too large, the majority of pixels will be below a user-defined threshold.

When an overflow condition is detected, an offset is added to the expected back porch level. This offset is user-defined in the White Crush Down register. The size of this value determines how quickly a correction is made to an overflow condition. Over time, this action will cause the expected backporch value to more closely represent the incoming sync tip. In turn, the analog AGC will adjust the decoded video signal to match the expected sync tip height which results in a properly saturated video signal.

When the majority of pixels are below a user defined threshold, the value stored in the White Crush Up register is added to the expected backporch value. This value sets the step size for correcting a *too dark* condition. Once the expected backporch value is modified, the analog AGC behaves the same as it otherwise would have for a reduced sync tip condition.

1.7.6.5 Up/Down Registers

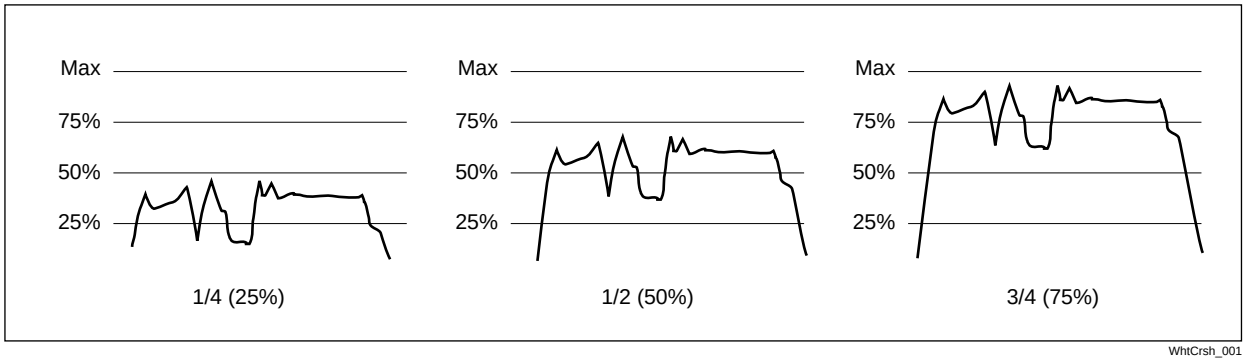
The default values programmed in the White Crush Up and White Crush Down registers are a good compromise for most video sources. Experience has determined that the best results were obtained by using a White Crush Up value that is larger than the White Crush Down value.

1.7.6.6 MAJS

The Majority Selected (MAJS) bits select the majority point level (51%) for the White Crush Up function. When a majority of the pixels in a frame or field are below a user selected value, the image is considered to be too dark. The White Crush Up logic increases the expected back porch value until the majority of pixels are above the specified level.

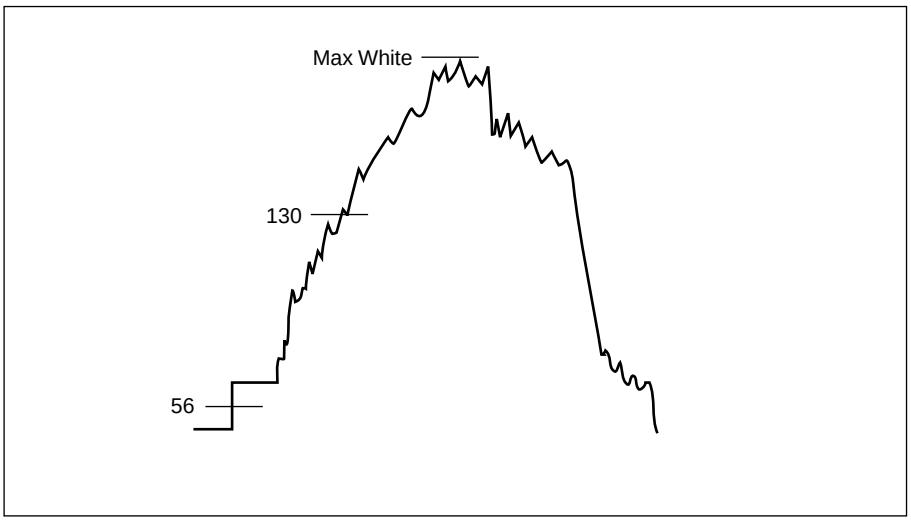
As illustrated in Figure 1-17, the settings of 1/4, 1/2, and 3/4 maximum luma check the decoded video against a fixed value of 25%, 50%, and 75%, of peak white, respectively.

Figure 1-17. MAJS Fixed Values



The automatic setting tracks the Average Picture Level (APL), as illustrated in Figure 1-18, and uses this level as its decision point. This is the default setting for the White Crush circuitry. The threshold is reset to a value of 96 when video is not present. This is equal to 1/2 of the peak white value. The APL value is updated once per frame or field, depending upon the state of the FRAME bit.

Figure 1-18. White Crush Average Picture Level (APL)



The APL value is incremented if 50% or more of the pixels in the previous frame/field were *greater* than the current value. Similarly, the value is decremented if the previous frame/field has more than 50% of its pixels *below* the current value.

1.7.6.7 WCFRM

The White Crush Frame (WCFRM) bit determines the frequency of updates to the expected backporch value. Changing the value from Frame Rate Updates to Field Rate Updates doubles the speed of corrections to the expected backporch value.

1.7.6.8 Enable

The White Crush circuitry must be enabled to be effective. The default value disables White Crush.

Due to the nuances of video signals, White Crush settings are somewhat subjective. No one value is adequate to suit all sources. The values programmed were derived by examining the effects of various values on a variety of sources.

Setting the decoder to respond too quickly can create objectionable artifacts that detract from the content. If the response is too slow, it will defeat the advantages provided by White Crush (the image is corrected so slowly that detail is lost). Extensive lab testing has determined the default values that work best for all conditions tested. Specific decoder applications may warrant deviation from these values when specific conditions are to be excluded from the expected usage. For example: if the decoder is placed in an environment where a camera is hard-wired to the decoder, then compensation for VCR artifacts and tuners, are of little importance. The default values were selected to apply to the most universal conditions.

1.7.7 ACC (Automatic Chrominance Gain Control)

The automatic chrominance gain control compensates for reduced chrominance and color-burst amplitude. This can be caused by high-frequency loss in cabling. Here, the color-burst amplitude is calculated and compared to nominal. The color-difference signals are then increased or decreased in amplitude according to the color-burst amplitude difference from nominal. The maximum amount of chrominance gain is 0.5 to 16 times the original amplitude. This compensation coefficient is then multiplied by the value in the saturation adjust register for a total chrominance gain range of 0 to 16 times the original signal. Automatic chrominance gain control is disabled by setting the CAGC bit in the CONTROL_1 (0x16) register to a logical 0.

1.7.8 Low Color Detection and Removal

If a color burst of 25 percent (NTSC) or 35 percent (PAL/SECAM) or less of the nominal amplitude is detected for 127 consecutive scan lines, the color-difference signals U and V are set to 0. When the low color detection is active, the reduced chrominance signal is separated from the composite signal to generate the luminance portion of the signal. The resulting Cr and Cb values are 128. Output of the chrominance signal is re-enabled when a color burst of 43 percent (NTSC) or 60 percent (PAL/SECAM) or greater of nominal amplitude is detected for 127 consecutive scan lines.

Low color detection and removal is disabled by setting the CKILL bit in the CONTROL_1 (0x16) register to a logical 0.

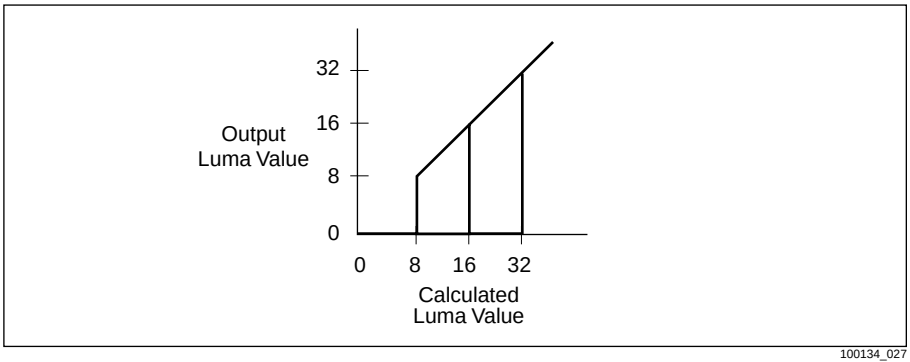
1.7.9 Coring

The Bt835 video decoder performs a coring function, in which it forces all values below a programmed level to zero. This is useful because the human eye is more sensitive to variations in black images. By taking near-black images and turning them into black, the image appears clearer to the eye.

Four luma coring values can be selected by the CONTROL_2 (0x17) register. These are 0, 8, 16, or 32 above black. If the total luminance level is below the selected limit, the luminance signal is truncated to the black value. If the luma range is limited (i.e., black is 16), the coring circuitry automatically references the appropriate value for black, as illustrated in Figure 1-19.

Similarly, four chroma coring values can be selected by the CONTROL_2 (0x17) register. These are 0, 2, 4, or 8 above black.

Figure 1-19. Coring Map

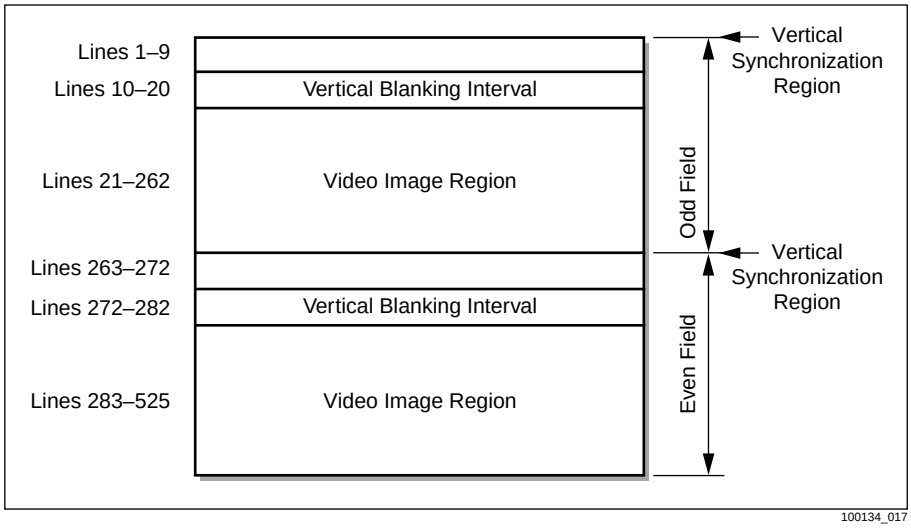


1.8 Bt835 VBI Data Output Interface

1.8.1 Introduction

A frame of video is composed of 525 lines for NSTC and 625 for PAL/SECAM. Figure 1-20 illustrates an NTSC video frame in which there are a number of distinct regions. The video image or picture data is contained in the ODD and EVEN fields within lines 21 to 262, and lines 283 to 525, respectively. Each field of video also contains a region for vertical synchronization (lines 1 through 9, and 263 through 272), as well as a region which can contain non-video ancillary data (lines 10 through 20, and 273 through 282). We will refer to the regions which are between the vertical synchronization region and the video picture region as the vertical blanking interval or VBI portion of the video signal.

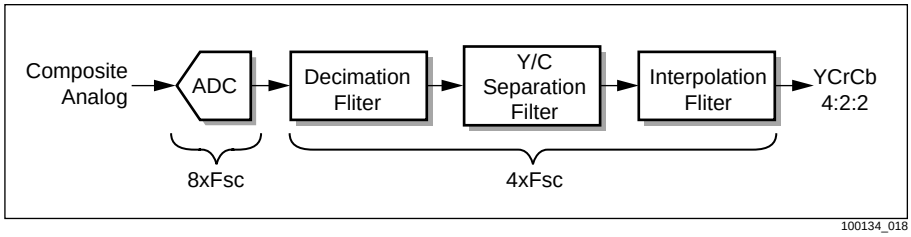
Figure 1-20. Regions of the Video Frame



1.8.2 Overview

In the default configuration of the Bt835, the VBI region of the video signal is treated the same way as the video image region of the signal. The Bt835 decodes this signal as if it were video. For example, it will digitize at 8xFsc, decimate/filter to a 4xFsc sample stream, separate color to derive luma and chroma component information, and interpolate for video synchronization and horizontal scaling. This process is illustrated in Figure 1-21.

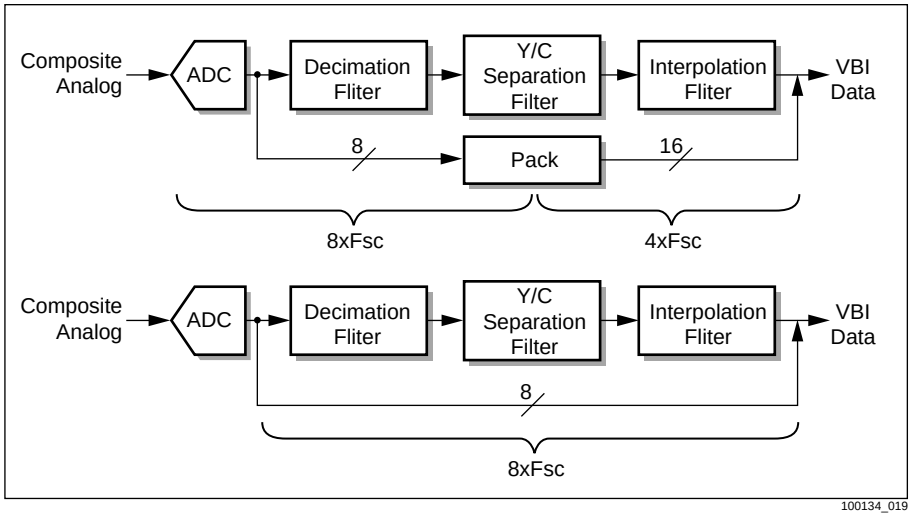
Figure 1-21. Bt835 YCrCb 4:2:2 Data Path



The Bt835 can be configured in a mode known as VBI data passthrough to enable capture of the VBI region ancillary data for later processing by software. In this mode, the VBI region of the video signal is processed as follows:

- The analog composite video signal is digitized at 8*Fsc (28.63636 MHz for NTSC and 35.46895 MHz for PAL/SECAM). This 8-bit value represents a number range from the bottom of the sync tip to the peak of the composite video signal.
- The 8-bit data stream bypasses the decimation filter, Y/C separation filters, and the interpolation filter (refer to Figure 1-22).
- The Bt835 provides the option to pack the 8*Fsc data stream into a 2-byte-wide stream at 4*Fsc before outputting it to the VD[15:0] data pins. Alternatively, it can be output as an 8-bit 8*Fsc data stream on pins VD[15:8]. In the packed format, the first byte of each pair on a 4*Fsc clock cycle is mapped to VD[15:8], and the second byte is mapped to VD[7:0], with VD[7] and VD[15] being the MSBs. The Bt835 uses the same 16-pin data port for VBI data and YCrCb 4:2:2 image data. The byte pair ordering is programmable.

Figure 1-22. Bt835 VBI Data Path



- The VBI datastream is not pipeline-delayed to match the YCrCb 4:2:2 image output data with respect to horizontal timing (i.e., valid VBI data is output earlier than YCrCb 4:2:2, relative to the Bt835 HRESET signal).
- A larger number of pixels per line is generated in VBI output mode than in YCrCb 4:2:2 output mode. The downstream video processor must be capable of dealing with a varying number of pixels per line to capture VBI data, as well as YCrCb 4:2:2 data from the same frame.
- The following pins can be used to implement this solution: VD[15:0], VACTIVE, HACTIVE, DVALID, $\overline{\text{VRESET}}$, $\overline{\text{HRESET}}$, CLKx1, CLKx2, QCLK. This allows the downstream video processor to correctly load the VBI data and the YCrCb 4:2:2 data.
- Because the 8*Fsc data stream does not pass through the interpolation filter, the sample stream is not locked/synchronized to the horizontal sync timing. The only implication of this is that the sample locations on each line are not correlated vertically.

1.8.3 Functional Description

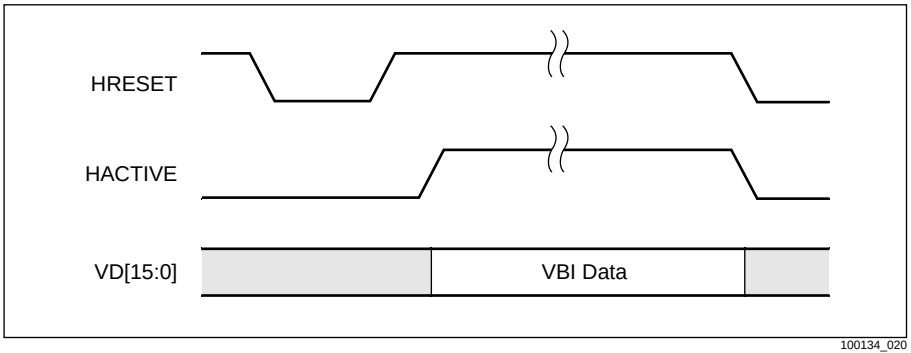
There are three modes of operation for the Bt835 VBI data passthrough feature:

1. VBI data passthrough disabled. During this default mode of operation, the device decodes composite video and generates a YCrCb 4:2:2 data stream.
2. VBI line output mode. The device outputs unfiltered 8*Fsc data only during the vertical interval, which is defined by the VACTIVE output signal provided by the Bt835. Data is output between the trailing edge of the $\overline{\text{VRESET}}$ signal and the leading edge of VACTIVE. When VACTIVE is high, the Bt835 outputs standard YCrCb 4:2:2 data. This mode of operation enables capture of VBI lines containing ancillary data, in addition to processing normal YCrCb 4:2:2 video image data.
3. VBI frame output mode. In this mode, the Bt835 treats every line in the video signal as if it were a vertical interval line and outputs only the unfiltered 8*Fsc data on every line (i.e., it does not output any image data). This mode of operation is designed for use in still-frame capture/processing applications.

1.8.4 VBI Line Output Mode

The VBI line output mode is enabled via the VBIEN bit in the CONTROL_1 register (0x16). When enabled, the VBI data is output during the VBI active period. The VBI horizontal active period is defined as the interval between consecutive Bt835 $\overline{\text{HRESET}}$ signals. Specifically, it starts at a point one CLKx1 interval after the trailing edge of the first $\overline{\text{HRESET}}$, and ends with the leading edge of the following $\overline{\text{HRESET}}$. This interval is coincident with the HACTIVE signal, as illustrated in Figure 1-23.

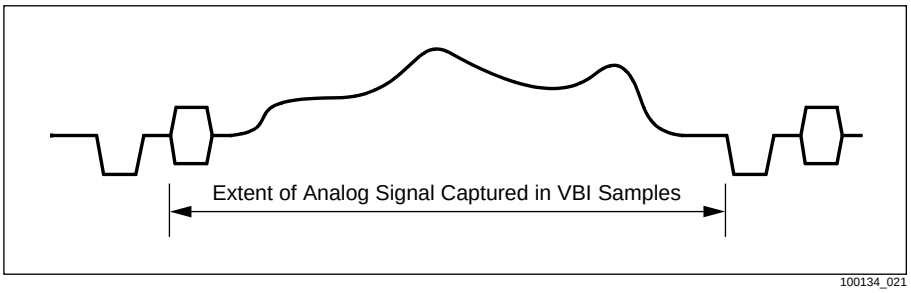
Figure 1-23. VBI Line Output Mode Timing



DVALID is always at a logical value of one during VBI. Also, QCLK is operating continuously at CLKx1 or CLKx2 rate during VBI. Valid VBI data is available one CLKx1 (or QCLK) interval after the trailing edge of $\overline{\text{HRESET}}$. When the Bt835 is configured in VBI line output mode, it generates invalid data outside the VBI horizontal active period. In standard YCrCb output mode, the horizontal active period starts at a time point that is delayed from the leading edge of $\overline{\text{HRESET}}$, as defined by the value programmed in the HDELAY register.

The VBI data sample stream, produced during the VBI horizontal active period, represents an 8*Fsc sampled version of the analog video signal, starting in the vicinity of the sub-carrier burst and ending after the leading edge of the horizontal synchronization pulse. This is illustrated in Figure 1-24.

Figure 1-24. VBI Sample Region

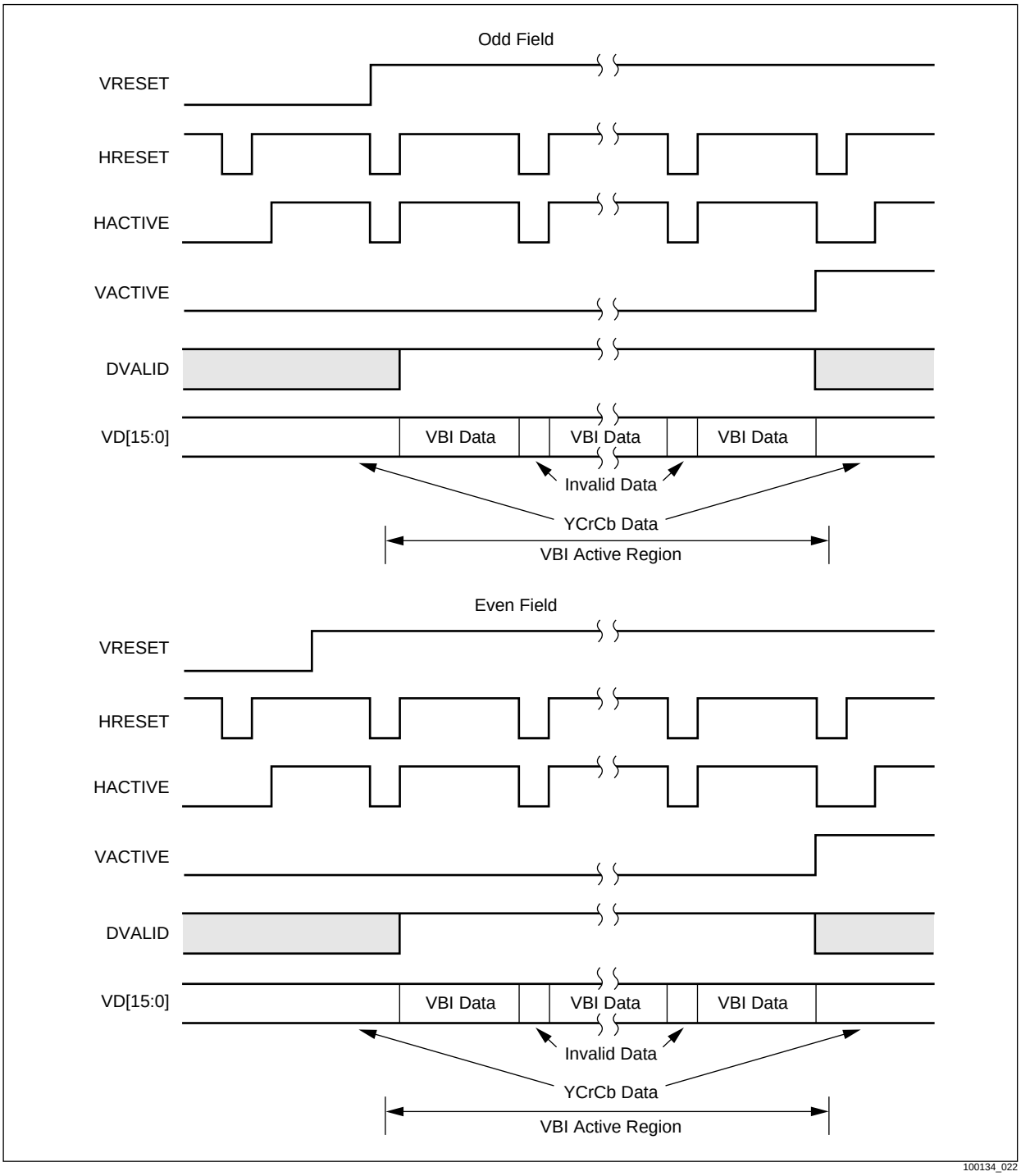


The number of VBI data samples generated on each line may vary, depending on the stability of the analog composite video signal input to the Bt835. The Bt835 generates 845 16-bit VBI data words for NTSC and 1070 16-bit VBI data words for PAL/SECAM on each VBI line at a CLKx1 rate. This is assuming a nominal or ideal video input signal (i.e., the analog video signal has a stable horizontal time base). This is equivalent to 1690 8-bit VBI data samples for NTSC and 2140 8-bit VBI data samples for PAL/SECAM. These values can deviate from the nominal, depending on the actual line length of the analog video signal.

The VBI vertical active period is the period between the trailing edge of the Bt835 $\overline{\text{VRESET}}$ signal and the leading edge of VACTIVE. Note that the extent of the VBI vertical active region can be controlled by setting different values in the VDELAY register. This provides the flexibility to configure the VBI vertical active region as any group of consecutive lines, starting with line 10 and extending to the line number set by the equivalent line count value in the VDELAY register (i.e., the VBI vertical active region can be extended into the video image region of the video signal).

The VBI horizontal active period starts with the trailing edge of an $\overline{\text{HRESET}}$; therefore, if a rising edge of $\overline{\text{VRESET}}$ occurs after the horizontal active period has already started, the VBI active period starts on the following line. The HACTIVE pin is held at a logical value of one during the VBI horizontal active period. DVALID is held high during both the VBI horizontal active and horizontal inactive periods (i.e., it is held high during the whole VBI scan line). These relationships are illustrated in Figure 1-25.

Figure 1-25. Location of VBI Data

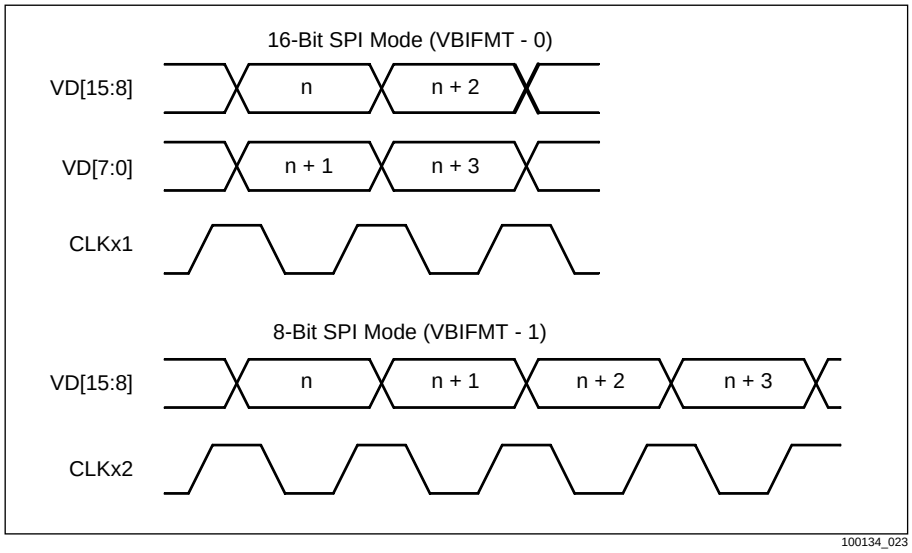


The Bt835 can provide VBI data in all the pixel port output configurations (i.e., 16-bit SPI, 8-bit SPI, ByteStream™, and VIP modes).

A video signal must be present on the Bt835 analog input as defined by the status of the VPRES bit in the STATUS register. This enables the Bt835 to generate VBI data. If the status of the VPRES bit reflects no analog input, the Bt835 generates YCrCb data to create a flat blue field image.

The order in which VBI data is presented on the output pins is programmable. Setting the VBIFMT bit in the CONTROL_1 register to a logical 0 places the nth data sample on VD[15:8] and the nth+1 sample on VD[7:0]. Setting VBIFMT to a logical 1 reverses the above. Similarly, in ByteStream and in 8-bit output modes, setting VBIFMT = 0 generates a VBI sample stream with an ordering sequence of n+1, n, n+3, n+2, n+5, n+4, etc. Setting VBIFMT = 1 for ByteStream/8-bit output generates a sequence of n+1, n+2, n+3, etc., as illustrated in Figure 1-26.

Figure 1-26. VBI Sample Ordering



To capture VBI data produced by the Bt835, a video processor/controller should be able to:

- Keep track of the line count to select a limited number of specific lines for processing VBI data.
- Handle data type transitioning on the fly, from the vertical interval to the active video image region. For example, during the vertical interval with VBI data passthrough enabled, the processor/controller must grab every byte pair while HACTIVE is high-using the 4*Fsc clock or QCLK. However, when the data stream transitions into YCrCb 4:2:2 data mode with VACTIVE going high, the video processor must interpret the DVALID signal (or use QCLK for the data load clock) from the Bt835 for pixel qualification, and use only valid pixel cycles to load image data (a default Bt835 operation).
- Handle a large and varying number of horizontal pixels per line in the VBI region, compared to the active image region.

1.8.5 VBI Frame Output Mode

In VBI frame output mode, the Bt835 generates VBI data continuously (i.e., there is no VBI active interval). In essence, the Bt835 acts as an ADC, continuously sampling the entire video signal at 8*Fsc. The Bt835 generates $\overline{\text{HRESET}}$,$\overline{\text{VRESET}}$, and FIELD timing signals in addition to the VBI data, but the DVALID, HACTIVE, and VACTIVE signals are all held high during VBI frame output operation. The behavior of the $\overline{\text{HRESET}}$,$\overline{\text{VRESET}}$, and FIELD timing signals is the same as normal YCrCb 4:2:2 output operation. The $\overline{\text{HRESET}}$,$\overline{\text{VRESET}}$, and FIELD timing signals can be used by the video processor to detect the beginning of a video frame/field, at which point it can start to capture a full frame/field of VBI data.

The number of VBI data samples generated on each line may vary, depending on the stability of the analog composite video signal input to the Bt835. The Bt835 generates 910 16-bit VBI data words for NTSC, and 1135 16-bit VBI data words for PAL/SECAM for each line of analog video input—at a CLKx1 rate. This is assuming a nominal or ideal video input signal (i.e., the analog video signal has a stable horizontal time base). This is equivalent to 1820 8-bit VBI data samples for NTSC, and 2270 8-bit VBI data samples for PAL/SECAM-for each line of analog video input. These values can deviate from the nominal, depending on the actual line length of the analog video signal.

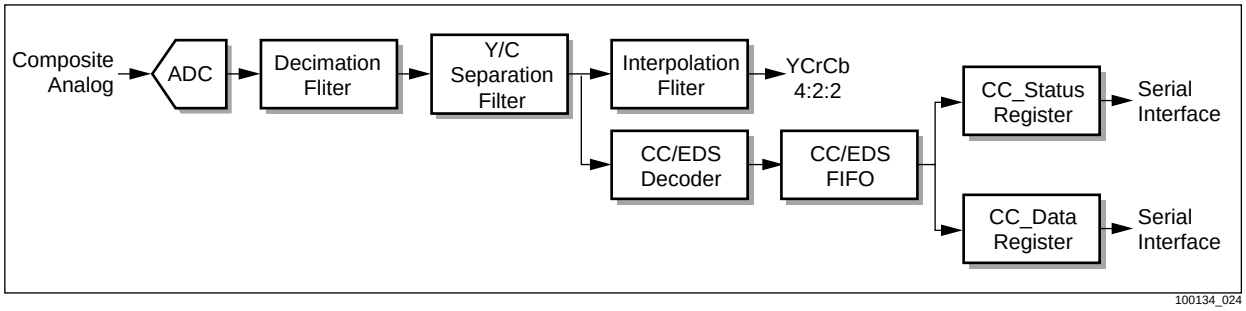
VBI frame output mode is enabled via the FRAME bit in the CONTROL_1 register. The output byte ordering can be controlled by the VBIFMT bit, as described for VBI line output mode. If both VBI line output and VBI frame output modes are enabled at the same time, the VBI frame output mode takes precedence.

1.9 Closed Captioning and Extended Data Services Decoding

For systems capable of capturing Closed Captioning (CC) and Extended Data Services (EDS) and which adhere to the EIA-608 standard, two bytes of information are presented to the video decoder on line 21 (odd field) for CC. An additional two bytes are presented on line 284 (even field) for EDS.

The data presented to the video decoder is an analog signal on the composite video input. The signal contains information which identifies it as the CC/EDS data. It is followed by a control code and two bytes of digital information transmitted by the analog signal. For purposes of CC/EDS, only the luma component of the video signal is relevant. Therefore, the composite signal goes through the decimation and Y/C separation blocks of the Bt835 before any CC/EDS decoding takes place. Figure 1-27 illustrates a representation of this procedure.

Figure 1-27. CC/EDS Data Processing Path

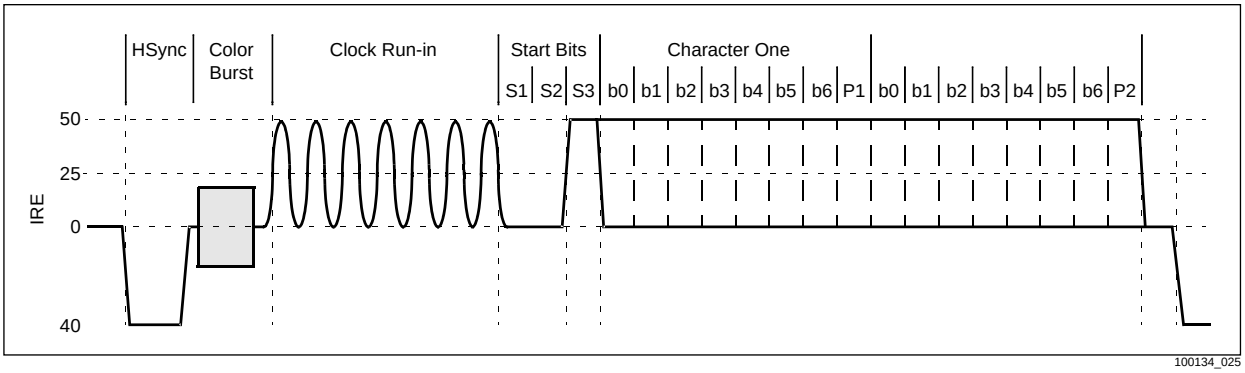


The Bt835 can be programmed to decode CC/EDS data via the corresponding bits in the CC_STATUS register. The CC and EDS are independent, and the video decoder may capture one or both in a given frame. The CC/EDS signal is illustrated in Figure 1-28. In CC/EDS decode mode, the CC/EDS data capture commences once the following occurs:

1. Bt835 has detected that line 21 of the field is being displayed.
2. The clock run-in signal is present.
3. The correct start code (001) is recognized by Bt835.

Each of the two bytes of data transmitted to the video decoder per field contains a 7-bit ASCII code and a parity bit. The convention for CC/EDS data is odd parity.

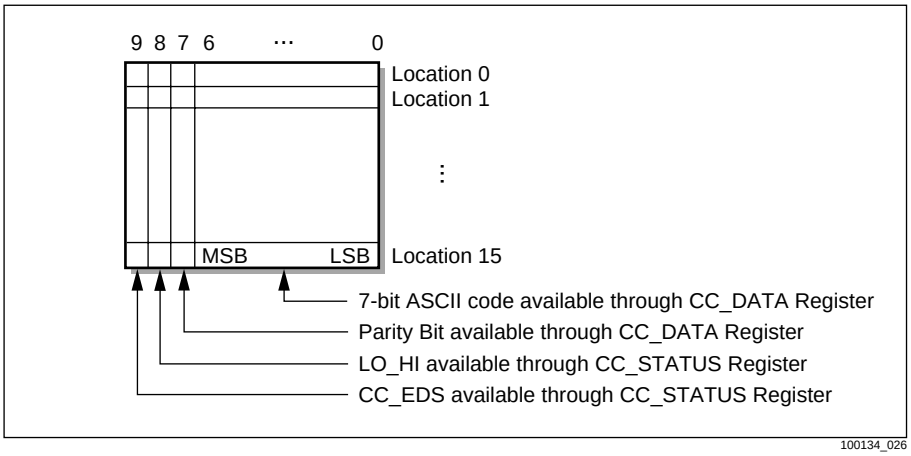
Figure 1-28. CC/EDS Incoming Signal



The Bt835 provides a 16 x 10 location FIFO for storing CC/EDS data. Once the video decoder detects the start signal in the CC/EDS signal, it captures the low byte of CC/EDS data first and checks to see if the FIFO is full. If the FIFO is not full, the data is stored in the FIFO, and is available to the user through the CC_DATA register (0x20). The high byte of CC/EDS data is captured next and placed in the FIFO. Upon being placed in the 10-bit FIFO, two additional bits are attached to the CC/EDS data byte by Bt835's CC/EDS decoder. These two bits indicate whether the given byte stored in the FIFO corresponds to CC or EDS data and whether it is the high or low byte of CC/EDS. These two bits are available to the user through the CC_STATUS register bits CC/EDS and LO/HI, respectively.

The parity bit is stored in the FIFO, as illustrated in Figure 1-29. Additionally, the Bt835 stores the results of the parity check in the PAR_ERR bit in the CC_STATUS register.

Figure 1-29. Closed Captioning/Extended Data Services FIFO



The 16-location FIFO can hold eight lines worth of CC/EDS data, at two bytes per line. Initially, when the FIFO is empty, bit DA in the CC_STATUS register (0x1F) is set low and indicates that no data is available in the FIFO. Subsequently, when data has been stored in the FIFO, the DA bit is set to logical high. Once the FIFO is half full, the CC_VALID interrupt pin signals to the system that the FIFO contents should be read in the near future. The CC_VALID pin is enabled via the INT_EN bit in the CC_STATUS register (0x1F). The system controller can then poll the CC_VALID bit in the STATUS register (0x00). This ensures that the Bt835 initiated the CC_VALID interrupt. This bit can also be used in applications where the CC_VALID pin is disabled by the user.

When the first byte of CC/EDS data is decoded and stored in the FIFO, the data is immediately placed in the CC_DATA and CC_STATUS registers, and is available to be read. Once the data is read from the CC_DATA register, the information in the next location of the FIFO is placed in the CC_DATA and CC_STATUS registers.

If the controller in the system ignores the Bt835 CC_VALID interrupt pin for a sufficiently long period of time, then the CC/EDS FIFO will become full, and the Bt835 will not be able to write additional data to the FIFO. Any incoming bytes of data will be lost, and an overflow condition will occur; bit OR in the CC_STATUS register will be set to a logical 1. The system can clear the overflow condition by reading the CC/EDS data and creating space in the FIFO for new information. As a result, the overflow bit is reset to a logical 0.

Asynchronous reads and writes to the CC/EDS FIFO will routinely occur. The CC/EDS circuitry writes the data; the reads occur as the system controller reads CC/EDS data from Bt835. These reads and writes sometimes occur simultaneously. The Bt835 gives priority to the read operations. When the CC_DATA register data is specifically being read to clear an overflow condition, the simultaneous occurrence of a read and a write will not cause the overflow bit to be reset, even though the read has priority. An additional read must be made to the CC_DATA register to clear the overflow condition. As always, the write data will be lost while the FIFO is in overflow condition.

The FIFO is reset when both CC and EDS bits are disabled in the CC_STATUS register; any data in the FIFO is lost.

2.0 Electrical Interfaces

2.1 Input Interface

2.1.1 Analog Signal Selection

The Bt835 contains an on-chip 4:1 MUX. For the Bt835, this multiplexer can be used to switch between four composite sources, or three composite sources and one S-Video source. In the first configuration, connect the inputs of the multiplexer (MUX[0], MUX[1], MUX[2], and MUX[3]) to the four composite sources. In the second configuration, connect three inputs to the composite sources and the other input to the luma component of the S-Video connector. When implementing S-Video, the input to the chroma A/D (CIN) should be connected to the chroma signal of the S-Video connector.

2.1.2 Multiplexer Considerations

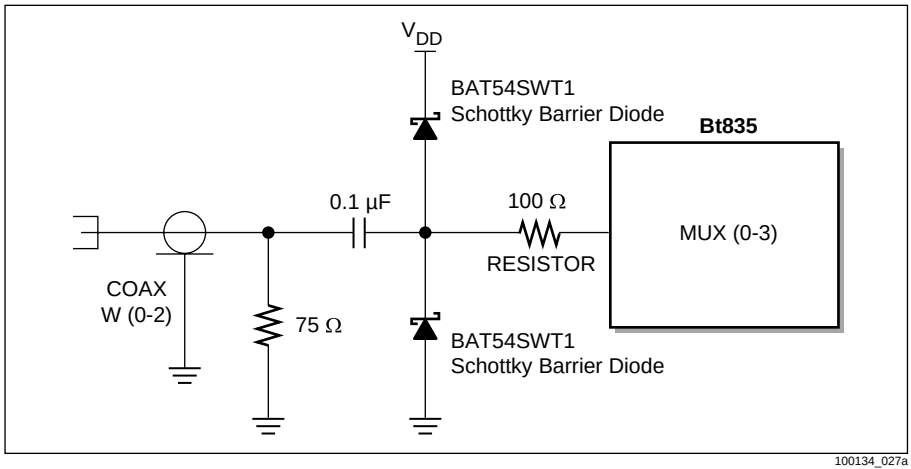
The multiplexer is not a break-before-make design. Therefore, during the multiplexer switching time, it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω

The multiplexers cannot be switched on a real-time pixel-by-pixel basis.

When used in a hostile environment and no active intervening input circuitry (e.g., tuner or op amp) is used, extra protection may be used by adding external protection diodes and a series resistor in the path of the composite/luma inputs, reducing the risk of voltage or current spikes coming into and possibly damaging the part. The diodes must be fast Shottky-type diodes. Figure 2-1 illustrates the specifics.

Diodes should be carefully chosen to conduct only above the input signal level, over the entire expected operating range, including any DC offsets, but below the V_{DD} level. This is required if these modifications will not degrade the video quality or sync locking capability of the Bt835 decoder. The diodes are strictly to help prevent damage due in part to unusually high, out of specification, voltage or current spikes on the video inputs.

Figure 2-1. Diode Protection (If required)



2.1.3 Auto Line Count Detection of NTSC or PAL/SECAM Video

If the Bt835 is configured to decode both NTSC and PAL/SECAM, the Bt835 can be programmed to automatically detect the line count being input to the chip. Auto line count detection automatically reprograms the PLL for the line count detected.

The Bt835 determines the video source input to the chip by counting the number of lines in a frame. Auto Line Count detection brings the Bt835 closer to a correct image. Further programming is required to refine the signal based on the input standard. See Table 1-4.

2.1.4 Flash A/D Converters

The Bt835 uses two on-chip flash A/D converters to digitize the video signals.

2.1.5 A/D Clamping

An internally generated clamp control signal is used to clamp the inputs of the A/D converter for DC restoration of the video signals. Clamping for composite and S-video analog inputs occurs within the horizontal sync tip.

2.1.6 Power-Up Operation

Upon power-up, the Bt835 device defaults to NTSC-M format with all digital outputs three-stated.

2.1.7 Digital Video Input Option

The VSIF and TG_CTL registers, 0x23 and 0x24, control the digital video port on the Bt835. The VSIF register controls the format of the video input to the decoder. The default is analog video from the 835 A/D(s). To use the digital input, change the VSFMT[2:0] bits in the VSIF register. Several input format options are available, including CCIR 656, Bytestream, and external sync methods of accepting the digital video. The system clock is controlled in the TG_CTL register. Typically in this application, the user inputs the digital clock corresponding to the digital video. In cases where the digital input clock frequency is different from the crystal input to the PLL (e.g., CCIR 656), the TG_RAM must also be reprogrammed. The option also exists to output a clock on the DIG_CLK pin.

2.1.8 Crystal Inputs and Clock Generation

The Bt835 has two pins for crystal or oscillator connection: XT0I/XT0O.
A typical crystal is specified as follows:

- 14.31818 MHz
- Fundamental
- Parallel resonant
- 30 pF load capacitance (varies by manufacturer)
- 50 ppm
- Series resistance 80 Ω or less

The following crystals are recommended for use with the Bt835:

1. Standard Crystal Corp.
   Phone: (626) 443-2121
   Fax: (626) 443-9049
   Standard: Part # AAK14M318180KLE20A

2. MMD
   Phone: (714) 753-5888
   Fax: (714) 753-5889
   Standard: Part # A18CA1-14.31818 MHz
   Low Profile: Part # B18CA1-14.31818 MHz

3. General Electric Devices (G.E.D)
   Phone: (760) 591-4170
   Fax: (760) 591-4164
   Standard: Part # PKHC49-U14.31818-020-005-050R
   Low Profile: Part # PKHC49-US14.31818-020-005-050R

4. Monitor Products Co., Inc.
   Phone: (619) 433-4510
   Fax: (619) 434-0255
   Standard: Part # MM49N1C3A-14.31818 MHz
   Low Profile: Part # SMS49N1C3A-14.31818 MHz

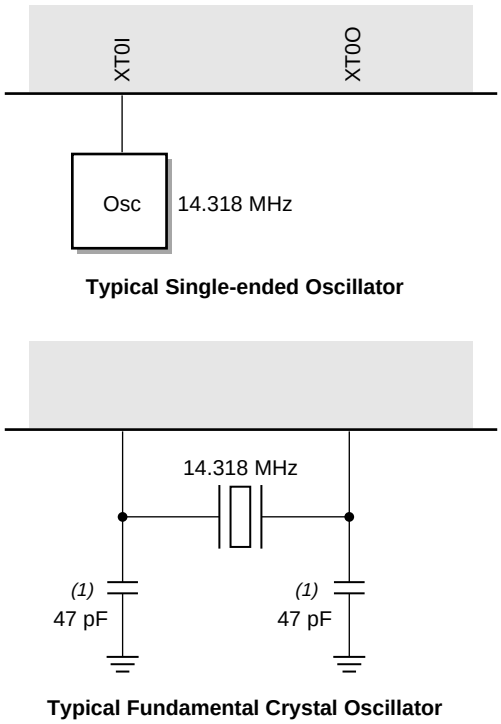
5. Fox Electronics
   Phone: (941) 693-0099
   Fax: (941) 693-1554
   Standard: Part # 49-014.318180-1
   Low Profile: Part # 49S-014.318180-1

6. Hooray Electronics Co. (H.E.C.)
   Phone: (818) 879-7414
   Fax: (818) 879-7417
   Standard: Part # H143-18
   Low Profile: Part # HH143-18

The clock source tolerance should be 50 parts-per-million (ppm) or less, but 100 ppm is acceptable. Devices that output CMOS voltage levels are required. The load capacitance in the crystal configurations may vary, depending on the magnitude of board parasitic capacitance. The Bt835 is dynamic; to ensure proper operation, the clocks must always be running with a minimum frequency of 14.318 MHz. Figure 2-2 illustrates the two clock options.

The CLKx1 and CLKx2 outputs from the Bt835 can be generated from an internal PLL. CLKx2 operates at 8x FSC, while CLKx1 operates at 4xFSC (where FSc represents the frequency of the NTSC or PAL subcarrier).

Figure 2-2. Clock Options



NOTE(S):
(1) Typical values shown. Values vary by board layout and xtal MFR. Use the values specified by the crystal vendor.

100134_027b

2.1.9 PLL Phase Locked Loop

2.1.9.1 What It Is

The PLL uses a phase detector, which compares the frequency of a Voltage Controlled Oscillator (VCO) to an incoming carrier signal, or a reference frequency generator. The output of the phase detector, after passing through a loop filter, is fed back to the VCO to keep it precisely in phase with the incoming reference frequency.

2.1.9.2 Background

Previous decoders have required a variety of crystals for NTSC and PAL, which have different line counts, subcarriers, and line times. Specific requirements, such as square pixel decoding, multiple resolutions, various output clock rates, and automatic standard selection, allowed the designer to select a variety of crystals to achieve the desired clock. Multiple clocks increased cost, took more board space, and created noisier EMI conditions.

2.1.9.3 Why We Need It

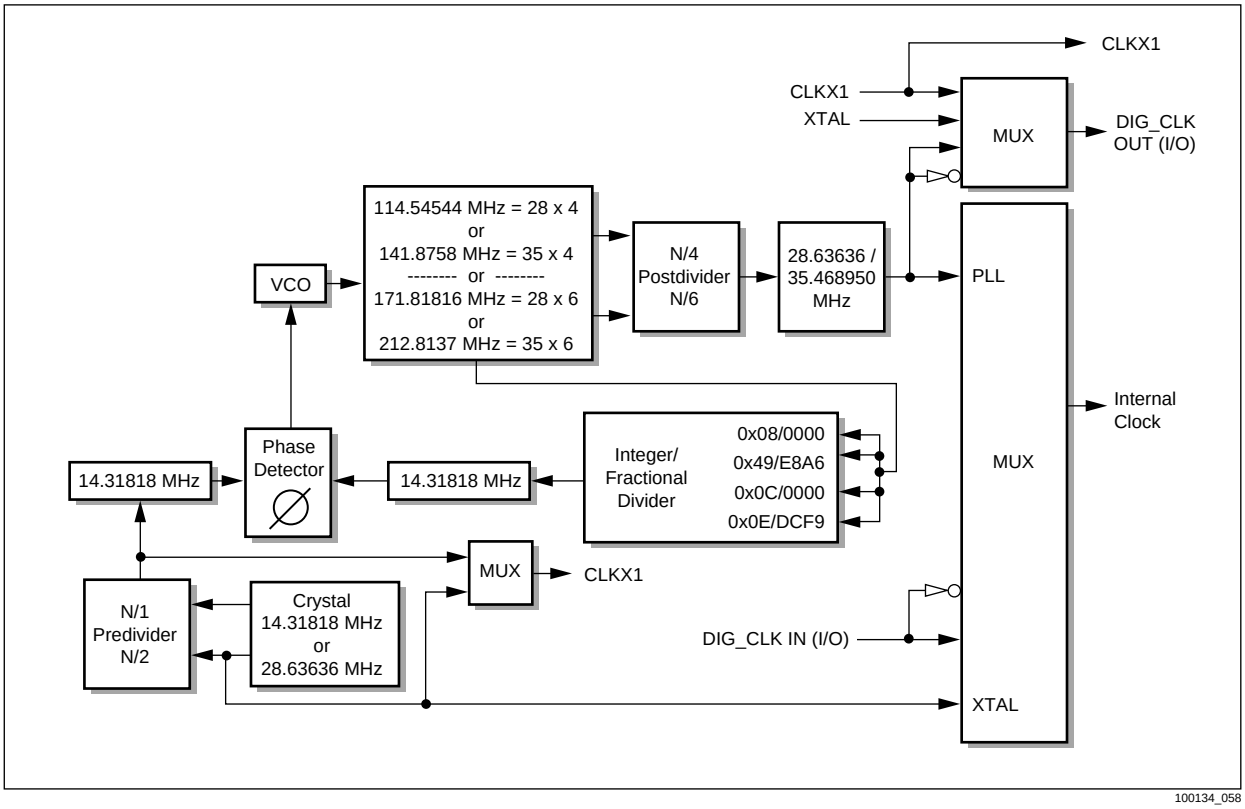
The PLL converts a single input clock to a variety of frequencies. This eliminates the need for several crystals or supporting filters, and reduces board space. It also simplifies circuit design for the hardware designer.

2.1.9.4 How It Does It

By dividing the output of the VCO, errors in phase can be fed to the phase detector to match the desired incoming frequency. An example is 2x. To obtain double frequency out, a divide by 2 counter is placed between the VCO and the phase detector. This fools the phase detector into matching the divided signal to the incoming clock frequency, producing a very small error voltage to the VCO, which adjusts its frequency either up or down and completes the loop.

This is a simplified description for illustrative purposes. In reality, the VCO runs at a very high frequency and is predivided to increase resolution for accuracy. Filters are used to prevent harmonic imaging and to damp responses to stabilize performance.

Figure 2-3. Functional Block Diagram



2.1.9.5 Programming the PLL

The PLL can be configured to produce the required 8 x F_{SC} internal and output frequency, either to 28.63636 MHz for standards using a 3.579545 MHz subcarrier, or to 35.468950 MHz for standards using a 4.43361875 MHz subcarrier. Although alternate values can be programmed, internal hard-coded counters will prevent proper color decoding and filtering. This may be acceptable for monochrome sources, but cannot be used for color sources.

PLL integer range is limited to 6 through 63. A value of 00 will sleep the PLL. Values outside the acceptable ranges (1 through 5, and above 63) can result in unpredictable behavior or loss of clock.

Any crystal value can be used, but the default PLL programming for NTSC and PAL assumes a 14.31818 MHz input frequency.

The Bt835 PLL has been designed and tested with a range of clock sources from a 14.31818 MHz source to a 35.468950 MHz. Although the PLL will possibly operate outside this range, it is neither tested nor guaranteed.

The XTAL input assumes a 28.63636 MHz source for NTSC, or 35.468950 MHz for PAL. If the PLL is not used, a 28 MHz source must be used for NTSC, but, by selecting the PLL, a less expensive and more common 14.31818 MHz can be used. If a 28 MHz source is used, the PLL_X bit can be set to divide the input frequency by 2, thereby simulating a 14 MHz source. This would be useful in systems where a 28 MHz source already exists.

The PLL_C bit controls the post divider and defaults to divide by 6. This is the preferred value, as the VCO loops are more stable at the higher VCO frequency.

To program the PLL, use the following formula:

(Output Frequency) × (Postdivider) ⁄ (Frequency In, After Predivider) = (INTEGER + FRACTION)

This yields a decimal result, which must then be converted to hexidecimal. The INTEGER result is then programmed into the PLL_XCI location for either 28 or 35 MHz, and the FRACTION value is programmed into the PLL_F (Fraction) for the matching register.

2.1.9.6 Things to look out for (exceeding values, resets, etc.)

If the Bt835's PLL is enabled before initialization, there is a risk that the PLL may not be running properly, or may even be stopped. Polling bit 3 of the status register, 0x00, indicates this condition. A 0 means the PLL is not locked; a 1 indicates lock. If the Bt835 is clocked by a stopped PLL, the part will be inaccessible by the two-wire serial interface, and will require a power cycle reboot to recover. This is because the Bt835's two-wire serial interface circuitry is also clocked by the master source clock.

A 0000 in register 0x25–PLL_F 28 MHz and 0x0C in register 0x27–PLL_XCI 28 MHz produces 28 MHz and is the default for these registers.

DCF9 in register 0x28–PLL_F 35 MHz and 0x0CE in register 0x2A–PLL_XCI 35 MHz produces 35 MHz and is the default for these registers.

While both registers can be programmed with either value, the auto-detect function assumes that if it counts 525 lines, then it selects values from registers 0x25 and 0x27; if it counts 625 lines, then it selects values from registers 0x28 and 0x2A.

2.1.9.7 Troubleshoot the PLL

If the PLL is suspected of trouble, the output can be routed outside the part. Use bits 2:3, TGCKO, of register 0x24–TG_CTL, to select the digital video clock output to route the PLL output to an external pin for viewing on a scope. Be sure that the CKDIR bit is at the default value of 0 to configure the DIGCLK pin as an output.

The crystal frequency is output on CLKX1 if the crystal is selected, or one-half the crystal frequency if the PLL is selected.

2.1.9.8 PLL Initialization

Upon power-up, there is the possibility that the PLL initializes to an indeterminate state. If this occurs, it puts the VCO in an unrecoverable extremely-high frequency state. If enabled in this state, the Bt835 draws more current, and although it ceases to function and all two-wire serial communications are lost, it is not a destructive mode. A power reset is all that is required to resume operation if this state is accidentally encountered.

To prevent this, reset the PLL control logic prior to enabling the PLL as follows (this is a good idea, even if the PLL is locked or not used, to reduce current):

1. Read the status before enabling the PLL bit 3 in register 0x00–STATUS (1 = locked, 0 = not locked).
2. Ensure the PLL is not selected (it may still be running, even if unlocked) by confirming that register 0x24, TGCKI[1:0] is set to 00.
3. Auto-detect can select either NTSC or PAL, and also selects the appropriate clock source; therefore, both the 28 MHz and 35 MHz registers must be reset.

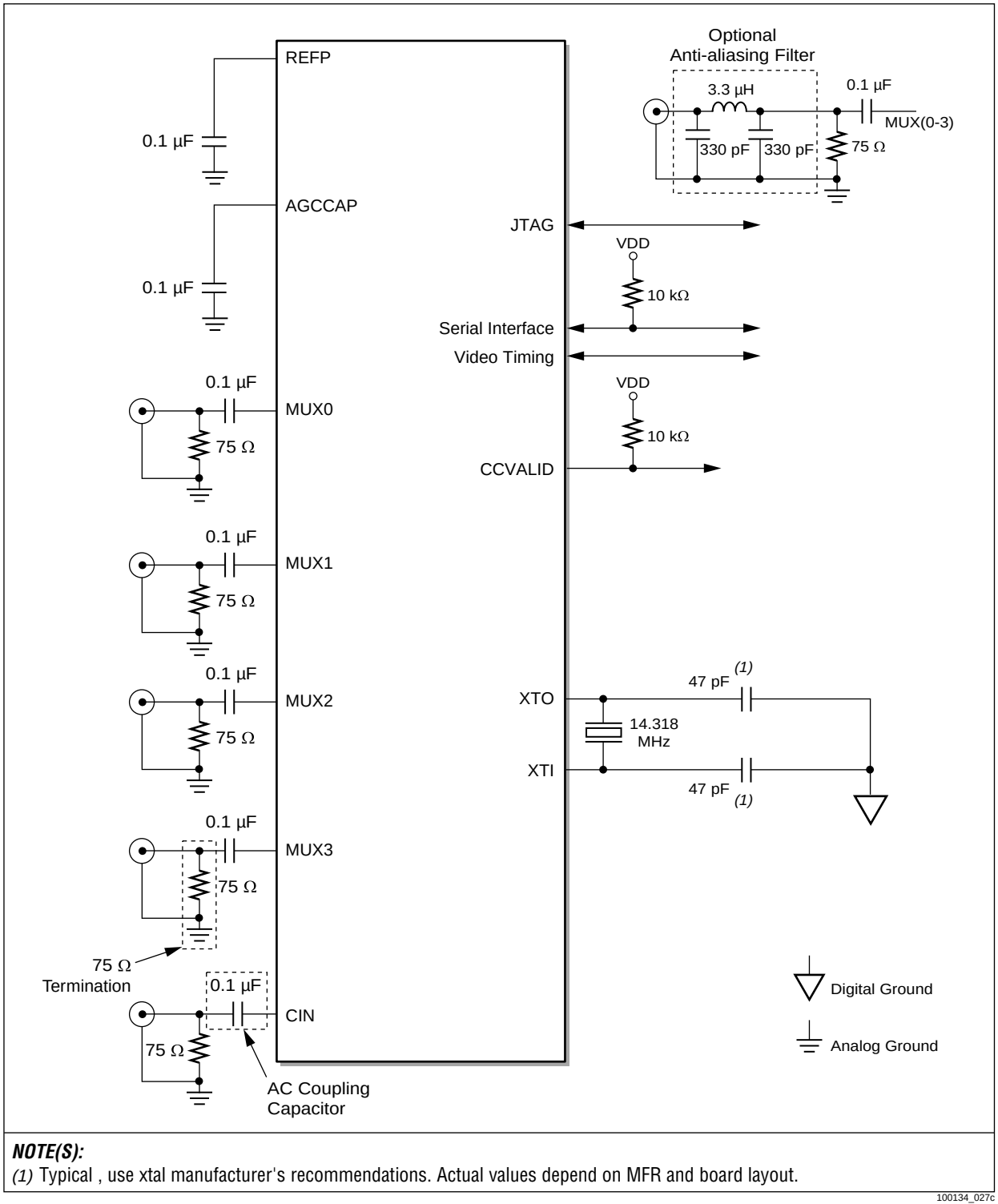
4. Read register 0x27–PLLXCI 28 MHz to determine the state of bits 7:6 so they can be returned to their previous values, if desired.
5. Read register 0x2A–PLLXCI 35 MHz to determine the state of bits 7:6 so they can be returned to their previous values, if desired.
6. Sleep the PLL by setting bits 5:0 to all 0s. Although only the active register sleeps the PLL, do this for both register 0x28 and register 0x2A, as the auto-detect can switch the clock source on demand.
7. Unsleep the PLL by restoring the defaults (or desired values obtained earlier) to registers 0x27 and 0x2A.
8. Enable the PLL using register 0x24–TG_CTL, TGCKI[1:0] set to 01. This selects the PLL as the decoder's primary clock source.

Whether using NTSC or PAL, do not leave the alternate 35 MHz (or 28 MHz) register in sleep mode as the auto-detect function could accidentally select the sleep-mode register, causing the part to stop due to lack of an input clock. Without an input clock, there is no internal clocking, therefore you will not be able to reprogram the part. Only a power cycle cures this condition.

2.1.10 2X Oversampling and Input Filtering

To avoid aliasing artifacts, digitized video may need to be band-limited. Because the Bt835 samples at 8xFsc, usually no filtering is required at the input to the A/Ds. However, if noise or other signal content is expected above 14.32 MHz in NTSC and 17.73 MHz in PAL, the optional anti-aliasing filter illustrated in Figure 2-4 may be included in the input signal path. After digitalization, the samples are digitally low-pass filtered and then decimated to CLKx1. The response of the digital low-pass filter is illustrated in Figure 2-5. The digital low-pass filter provides the digital bandwidth reduction to limit the video to 6 MHz.

Figure 2-4. Bt835 Typical External Circuitry

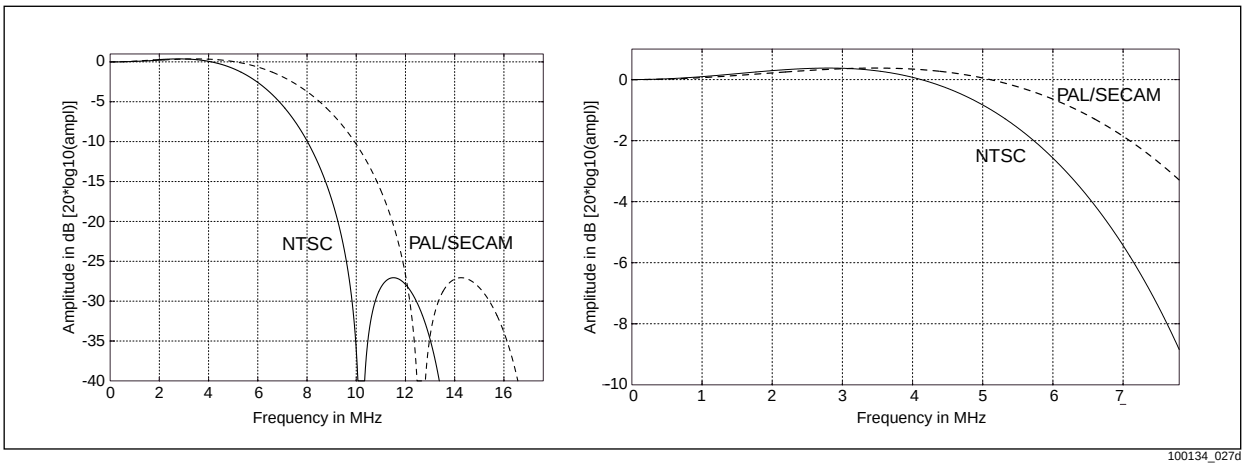


NOTE(S):

(1) Typical , use xtal manufacturer's recommendations. Actual values depend on MFR and board layout.

100134_027c

Figure 2-5. Luma and Chroma 2x Oversampling Filter



2.2 Output Interface

2.2.1 Output Interfaces

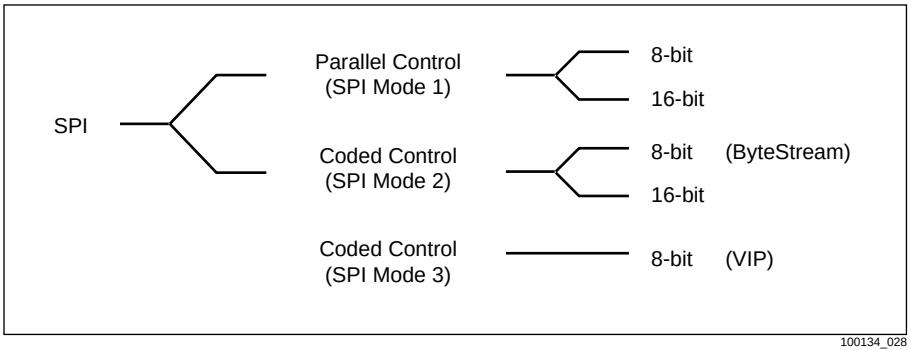
The Bt835 supports a Synchronous Pixel Interface (SPI). SPI supports 8-bit and 16-bit YCrCb 4:2:2 data streams.

Bt835 outputs all pixel and control data synchronous with CLKx1 (16-bit mode), or CLKx2 (8-bit mode). Events such as $\overline{\text{HRESET}}$ and $\overline{\text{VRESET}}$ can be encoded as control codes in the data stream to enable a reduced pin interface (ByteStream).

The VESA VIP interface mode is similar in concept to ByteStream, but uses ITU-R-656 header codes for video synchronization.

Mode selections are controlled by the CONTROL_2 (0x17) register. Figure 2-6 illustrates a diagram summarizing the different operating modes. Each mode will be covered individually in detail. On power-up, the Bt835 automatically initializes to SPI mode 1, at 16 bits wide.

Figure 2-6. Output Mode Summary



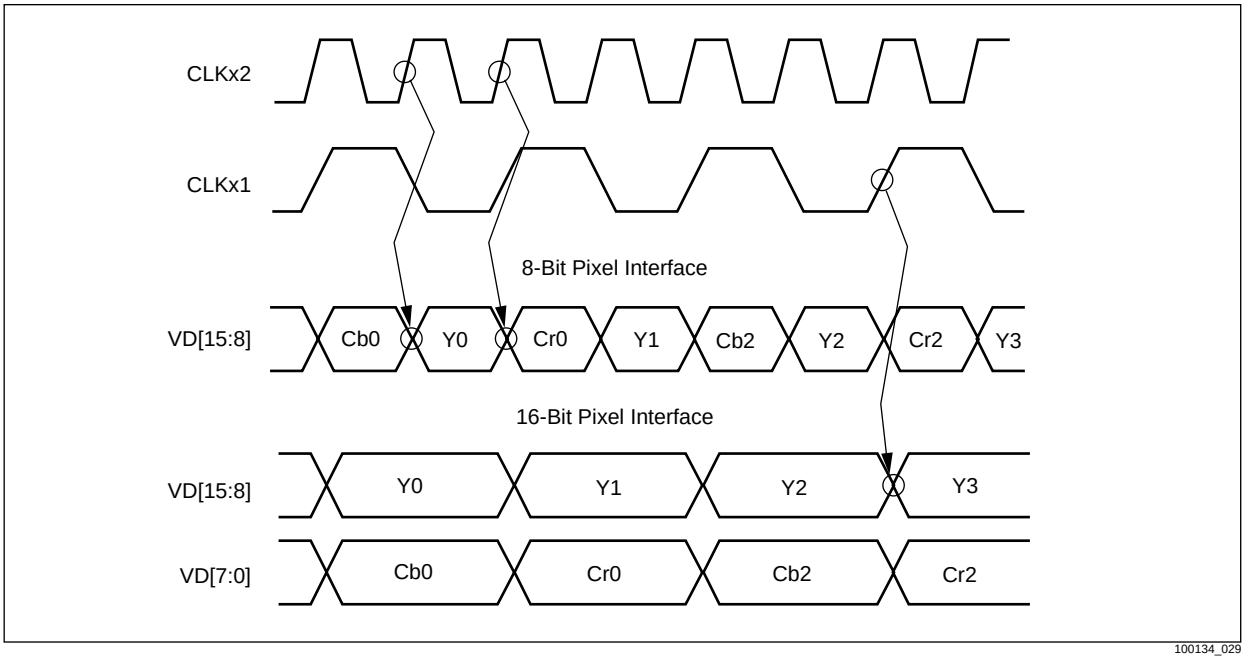
2.2.2 YCrCb Pixel Stream Format, SPI Mode 8- and 16-bit Formats

When the output is configured for an 8-bit pixel interface, data is output on pins VD[15:8], with eight bits of chrominance data preceding eight bits of luminance data for each pixel. New pixel data is output on the pixel port after each rising edge of CLKx2. When the output is configured for the 16-bit pixel interface, the luminance data is output on VD[15:8], and the chrominance data is output on VD[7:0]. In 16-bit mode, data is output with respect to CLKx1. Refer to Table 2-1 for a summary of output interface configurations. The YCrCb 4:2:2 pixel stream follows the CCIR recommendation, as illustrated in Figure 2-7.

Table 2-1. Pixel/Pin Map

16-bit Pixel Interface																
Pin Name	VD15	VD14	VD13	VD12	VD11	VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0
Data Bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	CrCb7	CrCb6	CrCb5	CrCb4	CrCb3	CrCb2	CrCb1	CrCb0
8-bit Pixel Interface																
Pin Name	VD15	VD14	VD13	VD12	VD11	VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0
Y Data Bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	—	—	—	—	—	—	—	—
C Data Bit	CrCb7	CrCb6	CrCb5	CrCb4	CrCb3	CrCb2	CrCb1	CrCb0	—	—	—	—	—	—	—	—

Figure 2-7. YCrCb 4:2:2 Pixel Stream Format (SPI Mode, 8 and 16 Bits)



2.2.3 Synchronous Pixel Interface (SPI, Mode 1)

Upon power-on reset, the Bt835 initializes to SPI output, mode 1. In this mode, Bt835 outputs all horizontal and vertical blanking interval pixels, in addition to the active pixels synchronous with CLKx1 (16-bit mode), or CLKx2 (8-bit mode). Figure 2-8 illustrates Bt835 SPI-1. The basic timing relationships remain the same for 16-bit or 8-bit modes. 16-bit modes use CLKx1 as the reference; 8-bit modes use CLKx2. Figure 2-9 illustrates the video timing for SPI mode 1.

Figure 2-8. Bt835 Synchronous Pixel Interface, Mode 1 (SPI-1)

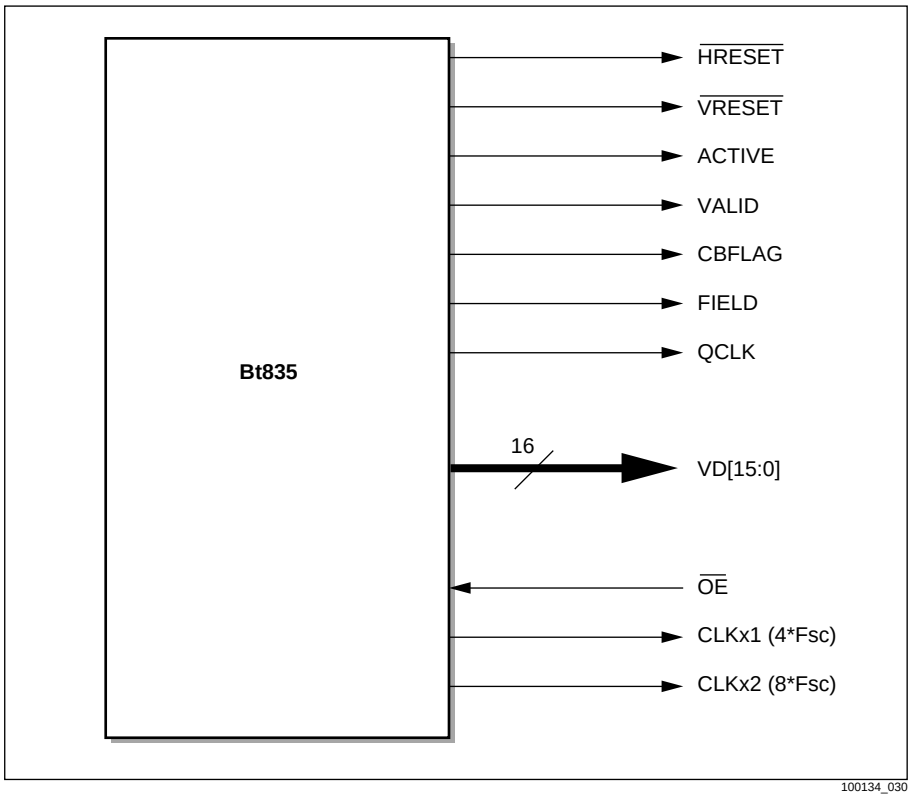
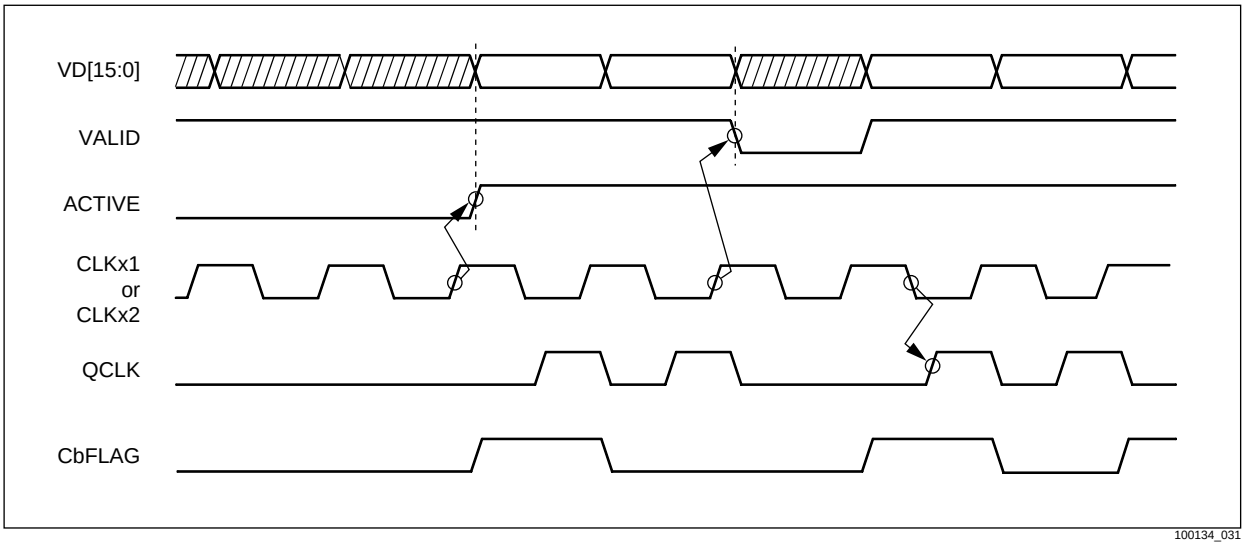


Figure 2-9. Basic Timing Relationships for SPI Mode 1



2.2.4 Synchronous Pixel Interface (SPI, Mode 2, ByteStream)

In SPI mode 2, the Bt835 encodes all video timing control signals onto the pixel data bus. ByteStream is the 8-bit version of this configuration. Because all timing data is included on the data bus, a complete interface to a video controller can be implemented in only nine pins: one for CLKx2, and eight for data.

When using coded control, the RANGE bit must be programmed low, and the BSTRM bit must be programmed high. When the RANGE bit is low, the chrominance pixels (both Cr and Cb) are saturated to the range 2 to 253, and the luminance range is limited to the range 16 to 253. In SPI mode 2, the chroma values of 255 and 254, and the luminance values of 0 to 15 are inserted as control codes to indicate video events (Table 2-2). A chroma value of 255 is used to indicate that the associated luma pixel is a control code; a pixel value of 255 also indicates that the Cb Flag is high (i.e., the current pixel is a Cb pixel). Similarly, a pixel value of 254 indicates that the luma value is a control code, and the CbFlag is low (Cr pixel).

The first pixel of a line is guaranteed to be a Cb flag; however, due to code precedence relationships, the $\overline{\text{HRESET}}$ code may be delayed by one pixel, so $\overline{\text{HRESET}}$ can occur on a Cr or a Cb pixel. Also, at the beginning of a new field, the relationship between $\overline{\text{VRESET}}$ and $\overline{\text{HRESET}}$ may be lost, typically with video from a VCR. As a result, $\overline{\text{VRESET}}$ can occur during either a Cb or a Cr pixel. Figure 2-10 illustrates coded control for SPI mode 2 (ByteStream).

Table 2-3 shows the pixel data output ranges. Independent of RANGE, decimal 128 indicates zero color information for Cr and Cb. Black is decimal 16 when RANGE is equal to 0. Code 0 occurs when RANGE = 1.

Figures 2-11 and 2-12 illustrate video timing for SPI modes 1 and 2.

Table 2-2. Description of the Control Codes in the Pixel Stream

Luma Value	Chroma Value	Video Event Description
0x00	0xFF 0xFE	This is an invalid pixel; last valid pixel was a Cb pixel. This is an invalid pixel; last valid pixel was a Cr pixel.
0x01	0xFF 0xFE	Cb pixel; last pixel was the last active pixel of the line. Cr pixel; last pixel was the last active pixel of the line.
0x02	0xFF 0xFE	Cb pixel; next pixel is the first active pixel of the line. Cr pixel; next pixel is the first active pixel of the line.
0x03	0xFF 0xFE	Cb pixel; HRESET of a vertical active line. Cr pixel; HRESET of a vertical active line.
0x04	0xFF 0xFE	Cb pixel; HRESET of a vertical blank line. Cr pixel; HRESET of a vertical blank line.
0x05	0xFF 0xFE	Cb pixel; VRESET followed by an even field. Cr pixel; VRESET followed by an even field.
0x06	0xFF 0xFE	Cb pixel; VRESET followed by an odd field. Cr pixel; VRESET followed by an odd field.

Figure 2-10. Data Output in SPI Mode 2 (ByteStream™)

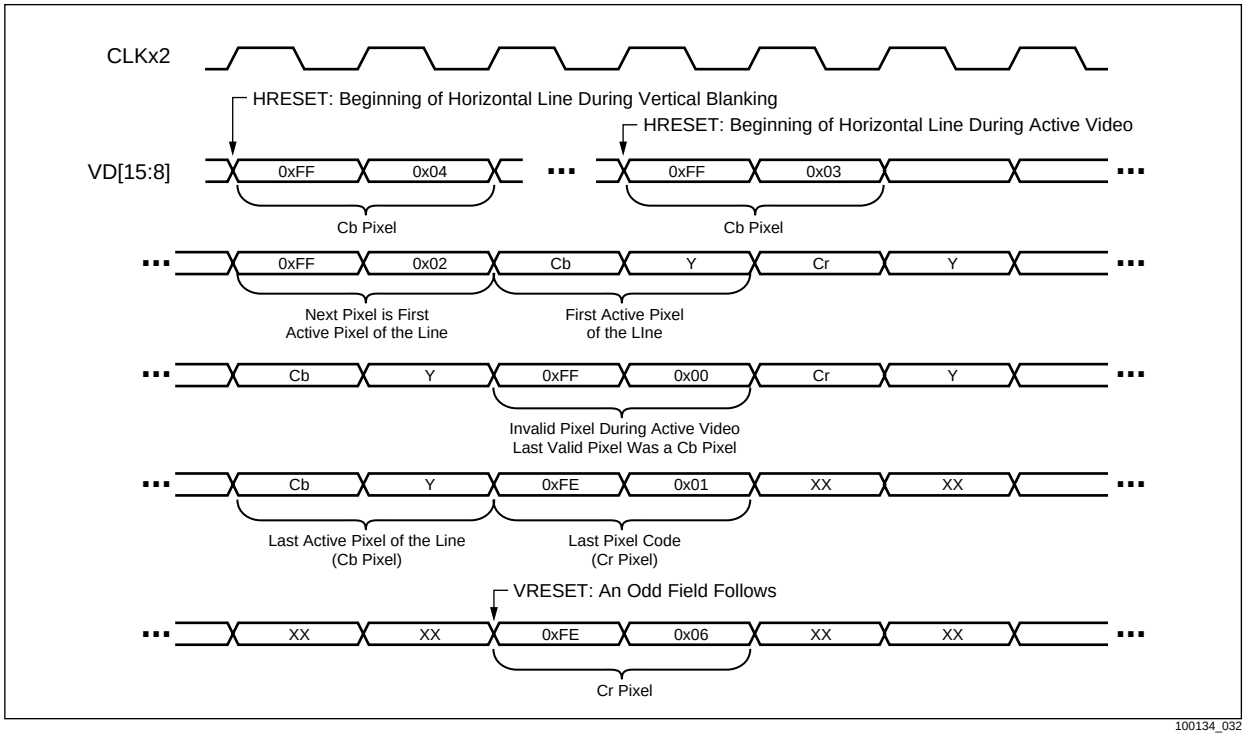


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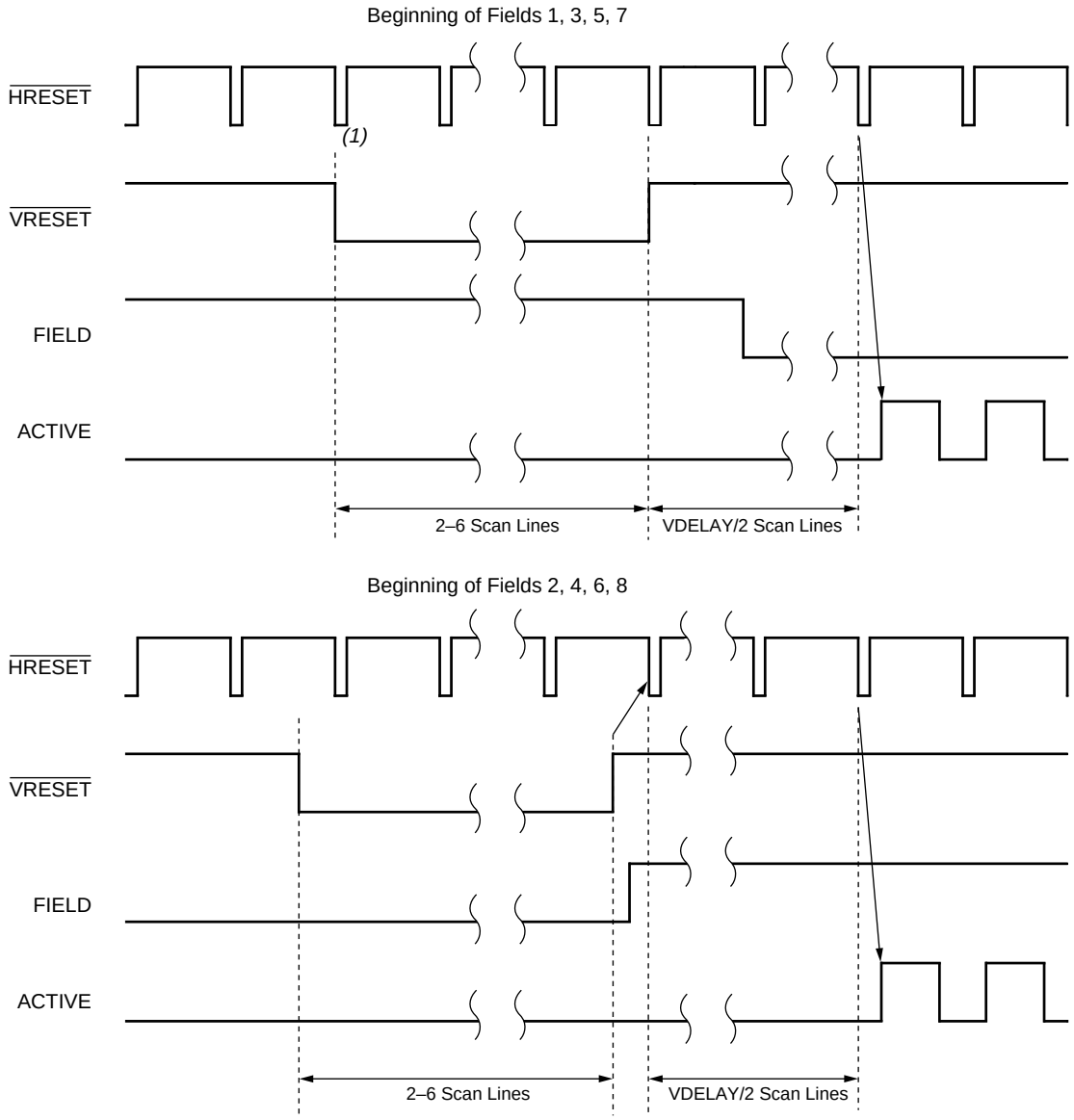
Figure 2-11. Video Timing in SPI Modes 1 and 2



NOTE(S):

(1) $\overline{\text{HRESET}}$ Precedes $\overline{\text{VRESET}}$ by two clock cycles at the beginning of fields 1, 3, 5, and 7 to facilitate external field generation.

2. ACTIVE pin may be programmed to be composite ACTIVE or horizontal ACTIVE.
3. ACTIVE, $\overline{\text{HRESET}}$, $\overline{\text{VRESET}}$, and FIELD are shown here with their default polarity. the polarity is programmable via the VPOLE register.
4. FIELD translations with the end of horizontal active video defined by HDELAY and HACTIVE.

100134_033

Figure 2-12. Horizontal Timing Signals in the SPI Modes

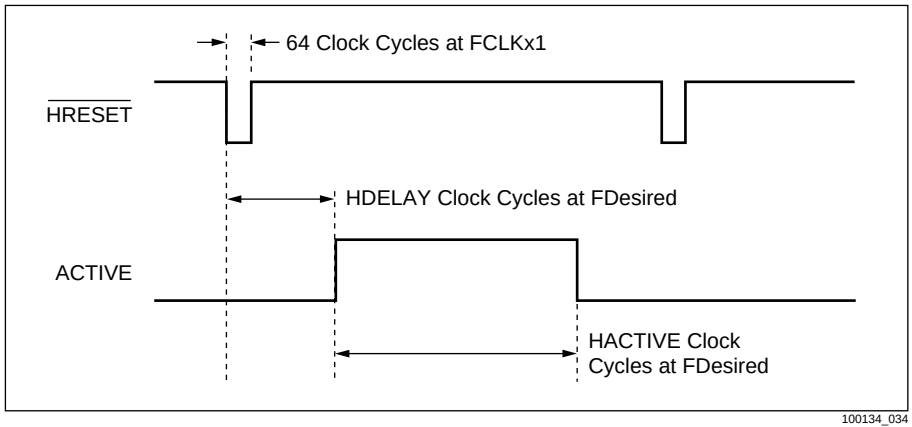


Table 2-3. Data Output Ranges

	RANGE = 0	RANGE = 1
Y	16 —> 253	0 —> 255
Cr	2 —> 253	2 —> 253
Cb	2 —> 253	2 —> 253

2.2.5 Synchronous Pixel Interface (Mode 3, VIP Interface)

In Video Interface Port (VIP) mode, the Bt835 video decoder transports several types of real time signal streams. Among these signals are:

- Active visible video, represented in digital baseband component YUV which can be scaled both horizontally and vertically.
- Raw ADC output samples of digital CVBS composite video during selected VBI lines representing VBI data.
- Other real time capture related data, excluding ancillary data.

The VIP Interface provides decoded active visible video, as selected by a video acquisition window definition of active pixels per line and active lines per field. Active video and raw ADC samples are interleaved into one single data stream, and they are synchronized and separated by unique ITU-R-656 header codes. According to the data type and the timing references, luma and chroma signals will be enveloped by appropriate Start of Active Video (SAV) or End of Active Video (EAV) header codes. VBI data is transported as raw ADC samples. The VIP Interface port does not support ancillary data. All timing reference control signals are transported through a VIP Interface block, pipelined to match any delay introduced in the data paths.

In the VIP mode, data must be clocked using 8-bit clock, CLKX2. It is possible to use QCLK to obtain additional setup and hold time if QCLK is first programmed to eliminate additional gating. To do this, the VLDFMT bit, bit 1 of CONTROL_3, register 0x18, should be set to 0, and bus width, LEN, should be set to 8 bit, for a value of 0x12 for this register.

In addition. the RANGE bit (bit 1 in CONTROL_2) must be set to 0: (16–253); and BSTRM bit, bit 2, should be set to the default 0, no Bytestream control codes, and VIPEN must be set to a 1, to change the default 0x01 to 0x05 for this register.

VIP Interface mode is enabled via a user programmable bit, VIPEN. When the VIPEN bit is disabled, all video signals are transported through the interface unaltered.

EAV codes always precede SAV codes in a digital video line.

Table 2-4. ITU-R-656 Specification on Range of Active Video Data

LUMA		CHROMA		
Range (decimal)	Y	Range (decimal)	C_r	C_b
Black	16	No Color	128	128
White	235	100% Saturation	16-240	16-240

Active video data is sampled as YC_rC_b (YUV) 4:2:2 and transmitted as a byte serial stream in the following order:

$$C_b – Y – C_r – Y – C_b – Y – C_r – Y \text{ - - - - - -}$$

2.2.5.1 Bt835 VIP Code (T, F, V, H) Generation

Y, Cr, Cb data is all represented in 8-bit word format. However, during VIP mode control codes, SAV and EAV, are inserted into the data stream before the start of active video and after the end of active video, respectively, in a digital video line. SAV and EAV codes consists of a hexadecimal four-word sequence in the following format: FF, 00, 00, XY. The first three words FF, 00, 00, are a fixed preamble where FF and 00 are reserved for use in timing reference signals. The fourth word, XY, contains information such as the state of field blanking, the state of vertical line blanking, and the state of horizontal line blanking. The upper nibble of byte XY represents the actual reference information, and the lower nibble is used as error protection and correction parity bits.

According to ITU-R- 656 and VESA VIP Interface Spec 1.1, the upper nibble X of the reference byte contains the three reference bits F, V, H. The BT835 also includes a T-bit, and the bits occur in the sequence TFVH.

In the analog domain, a line begins with the front porch, the sync tip, the back porch, and then active video. In VIP, a line begins with EAV, followed by active video, followed by SAV. The bits T, F, V can only change in the EAV code. Table 2-5 describes each bit in a word, XY, in detail.

Table 2-5. Reference Byte, XY[7:0] and its Individual Bit Information

Bits	Name	Event Description
XY[7]	T-bit, Task Bit	Active Video Data: T-bit = 1, VBI Data: T-bit = 0.
XY[6]	F-bit, Field ID	Even Field: F-bit = 1, Odd Field: F-bit = 0.
XY[5]	V-bit, Vertical Blanking ID	Active Video Line: V-bit = 0, Lines during Vertical Blanking: V-bit = 1.
XY[4]	H-bit, Horizontal Blanking ID	Active Pixels: H-bit = 0, Pixels during Horizontal Blanking: H-bit = 1.
XY[3]	P3, Parity Error Detection Bit	((H-bit ___ V-bit) ___ (Inverse(T-bit)))
XY[2]	P2, Parity Error Detection Bit	((F-bit ___ H-bit) ___ (Inverse(T-bit)))
XY[1]	P1, Parity Error Detection Bit	((F-bit ___ V-bit) ___ (Inverse(T-bit)))
XY[0]	P0, Parity Error Detection Bit	((F-bit ___ V-bit) ___ (H-bit))
NOTE(S): _ indicates “Exclusive OR” bit wise operation.		

T-bit Normally, video lines that are not selected by the active video acquisition window do not appear on the VIP bus. An exception is VBI data. The VBI data is transported in a manner similar to the active video data except it is not multiplexed into chroma and luma, but treated as a single stream of raw ADC samples.

The task bit T, distinguishes between visible active video to be displayed, and selected raw VBI-ADC samples, that are to be placed in off-screen memory. It is always high, unless VBI is enabled. When the VBIEN register bit is high, the T-bit will go low during the VBI.

This transition to low occurs at the EAV associated with the last line when VRESET is low, and is described in detail:

VRESET transitions to low at the beginning of the first serration pulse, and transitions high at the end of the last post-equalization pulse. While VRESET will vary by a half line depending on whether it is an odd and even field, the T-bit will only transition on the next EAV following, or coincident with a VRESET, which is not a half line, but a whole line. It will therefore transition high to low at the very next EAV that occurs after VRESET goes low to high (see Figure 2-13 for details).

The T-bit then transitions from low to high at the same point where the V-bit transitions high, which occurs at the EAV just prior or equal to VACTIVE going high (see Figure 2-14).

It only changes during the EAV codes.

NOTE: CCIR-656 does not recognize the use of the the T-bit, and expects it to always be high.

Figure 2-13. T-bit Low

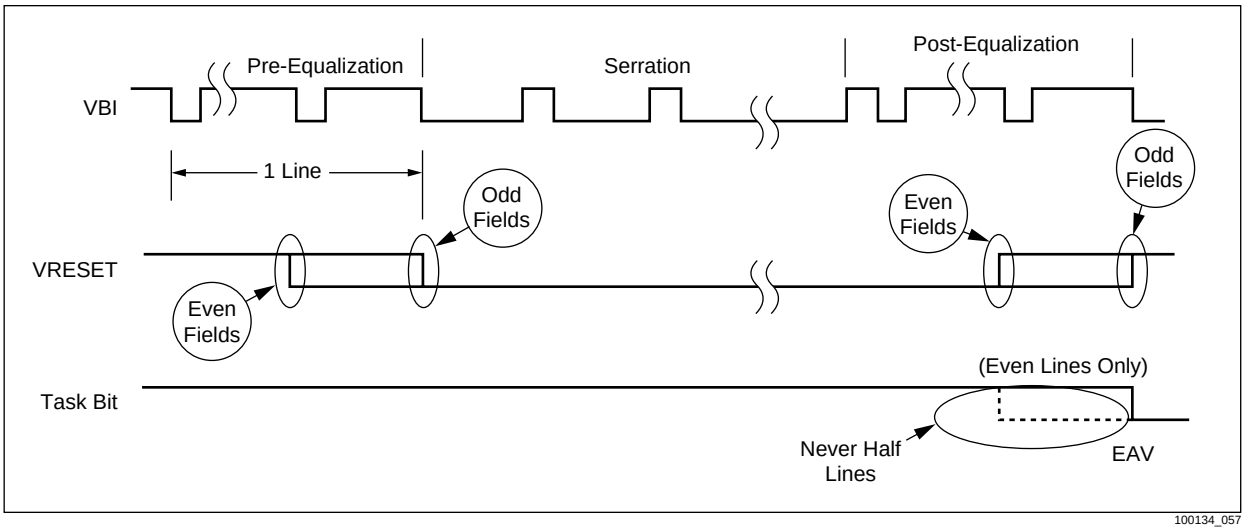
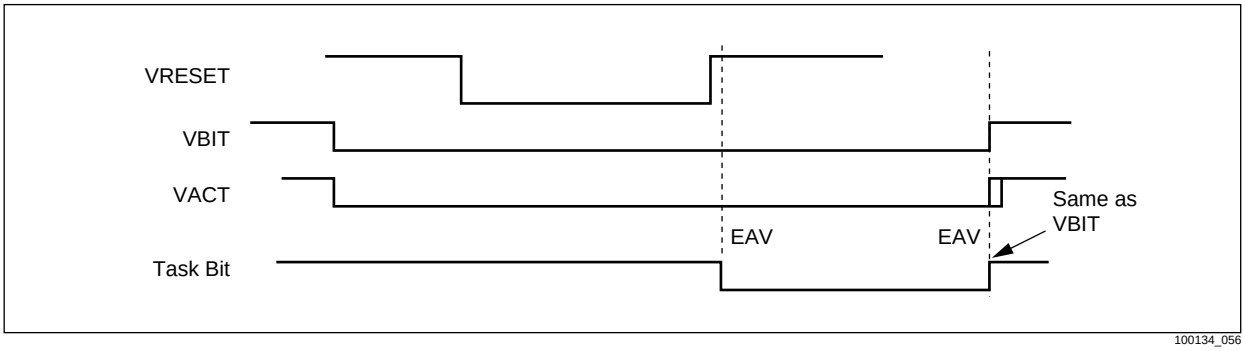
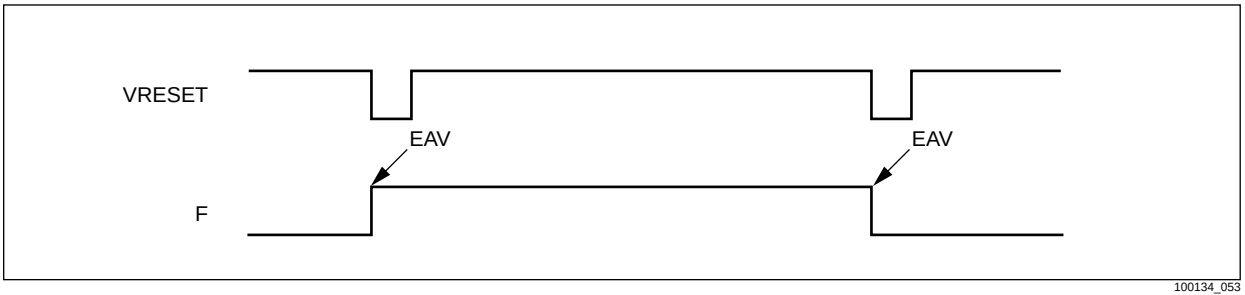


Figure 2-14. T-bit High



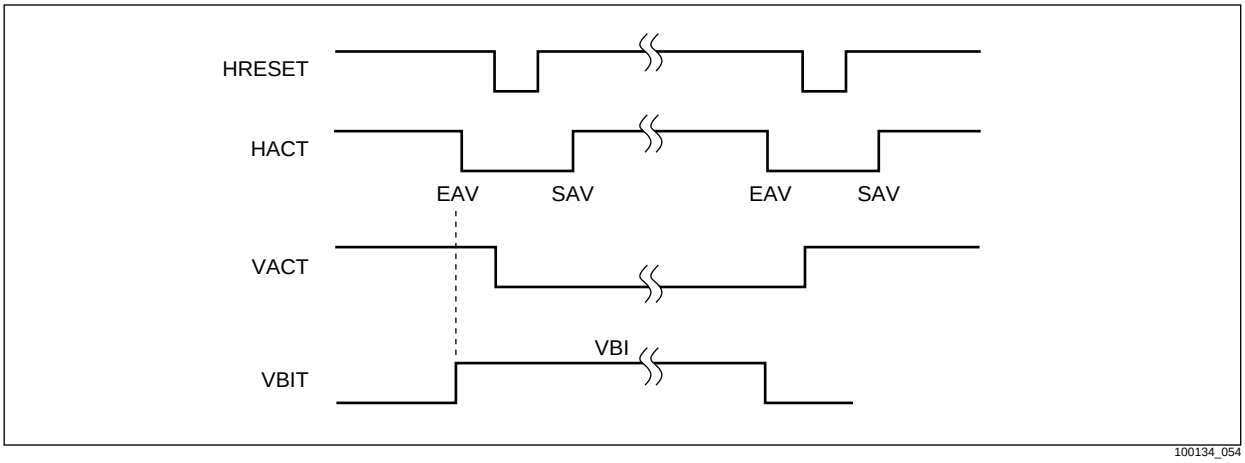
F-bit The field ID bit F, indicates odd or even fields by indicating a 1 for an even field, and a 0 for odd fields. It toggles only on the EAV code that precedes the leading edge of VRESET (see Figure 2-15 for details).

Figure 2-15. F-bit



V-bit The V bit indicates the vertical blanking region of a digital video field and is derived from the VACTIVE signal. It changes from low to high at the last EAV generated by the end of HACTIVE for the last line before VACTIVE transitions from high to low. It changes from high to low at the last EAV generated by the end of HACTIVE for the last line before VACTIVE transitions from low to high. It only changes during the EAV codes (see Figure 2-16 for details).

Figure 2-16. V-bit



H-bit The H bit indicates the horizontal blanking region of a digital video line. For SAV codes, the H bit is always zero, and for EAV codes, the H bit is always one.

At the start of horizontal active video, the HACTIVE signal is held HIGH, and the H-bit is set LOW. At the end of horizontal active video, HACTIVE goes LOW and the H-bit is set to HIGH. In other words, the EAV code contains an H-bit equal to one and the SAV code contains an H-bit equal to zero. Note that, for line count purposes, the EAV marks the beginning of a digital video line.

It changes during both EAV and SAV codes (see Figure 2-17 for details).

Figure 2-17. H-bit

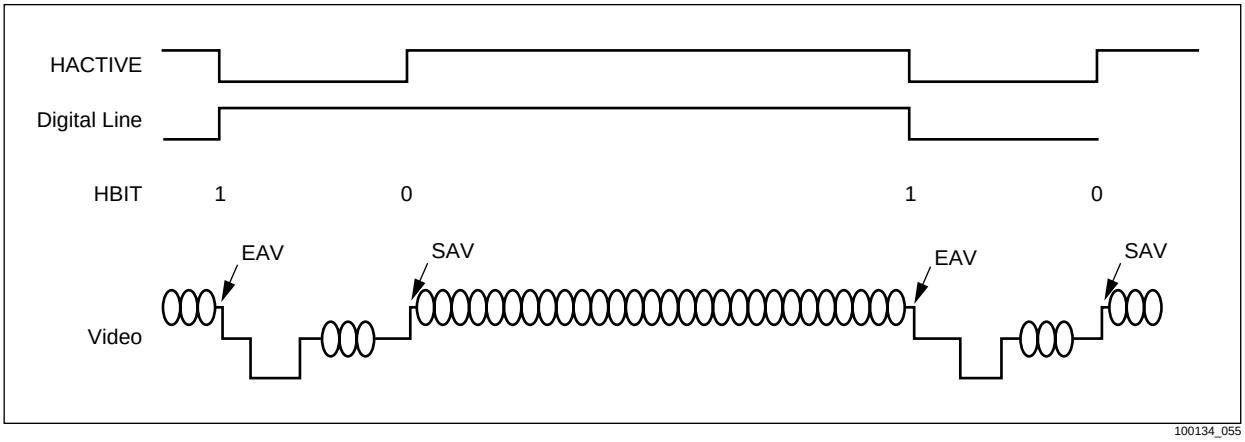


Table 2-6 lists SAV and EAV codes in relation to specific events occurring during a digital video line.

Table 2-6. VIP SAV and EAV Codes Under Full Resolution *(1 of 3)*

Code Type	Event Description	Inserted Headers and 'raster' Reference Code		Corresponding Discrete Pin/Signal	Comments
	TASKS (Active Video or VBI Mode)	Field ID			
		Odd	Even		
EAV	Previous pixel was last pixel of any active line but NOT the last line.		FF-00-00- D A 1101 1010	HACTIVE = 1, VACTIVE = 1, FIELD = 1, NVRESET = 1.	FIELD signal transitions with trailing edge of NVRESET
SAV	Next pixel is first pixel of any active 'acquired' line but NOT the last line.		FF-00-00- C 7 1100 0111	HACTIVE = 0, VACTIVE = 1, FIELD = 1, NVRESET = 1.	NVRESET is an active LOW signal.
EAV	Previous pixel was the last pixel of the last active line.		FF-00-00- F 1 1111 0001	HACTVE = 0, VACTIVE = 1, FIELD = 1, NVRESET = 1,	EAV code marks the beginning of a digital video line.
SAV	Next pixel is first pixel of first inactive line.		FF-00-00- E C 1110 1100	HACTIVE = 1, VACTIVE = 0, FIELD = 1, NVRESET = 1,	SAV arrives after EAV, following HACTIVE signal.

Table 2-6. VIP SAV and EAV Codes Under Full Resolution *(2 of 3)*

Code Type	Event Description	Inserted Headers and 'raster' Reference Code		Corresponding Discrete Pin/Signal	Comments
	TASKS (Active Video or VBI Mode)	Field ID			
		Odd	Even		
EAV	Previous pixel was last pixel of the line, immediately before NVRESET goes low.		FF-00-00- B 6 1011 0110	HACTIVE = 0, VACTIVE = 0, FIELD = 1, NVRESET = 1,	F-bit toggles with leading edge of NVRESET.
SAV	Next pixel is first pixel of line immediately after NVRESET becomes active low.		FF-00-00- A B 1010 1011	HACTIVE = 1, VACTIVE = 0, FIELD = 1, NVRESET = 0,	F-bit toggles in vertical blanking interval.
EAV	Previous pixel was last pixel of the line immediately before VBI mode is enabled.		FF-00-00- 3 8 0011 1000	HACTIVE = 0, VACTIVE = 0, FIELD = 1, NVRESET = 0,	VBI mode
SAV	Next pixel is first pixel of a line immediately after VBI mode is enabled.	FF-00-00- 2 5 0010 0101		HACTIVE = 1, VACTIVE = 0, FIELD = 0, NVRESET = 1,	Start of first VBI line
EAV	Previous pixel was last pixel of last line in vertical blanking interval during VBI mode.	FF-00-00- 9 D 1001 1101		HACTIVE = 0, VACTIVE = 0, FIELD = 0, NVRESET = 1,	Occurs during VBI mode.
SAV	Next pixel is first pixel of FIRST active 'acquired' line	FF-00-00- 8 0 1000 0000		HACTIVE = 1, VACTIVE = 1, FIELD = 0, NVRESET = 1,	Active video line data is processed at the rising (or leading) edge of VACTIVE.
EAV	Previous pixel was last pixel of any active line, but NOT the line immediately before last active line.	FF-00-00- 9 D 1001 1101		HACTIVE = 0, VACTIVE = 1, FIELD = 0, NVRESET = 1.	FIELD pinand F-bit in control codes, do not transition at the same time.
SAV	Next pixel is first pixel of any active 'acquired' line.	FF-00-00- 8 0 1000 0000		HACTIVE = 1, VACTIVE = 1, FIELD = 0, NVRESET = 1.	EAV code always precedes SAV code in a digital video line.
EAV	Previous pixel was last pixel of the line immediately before last active line ONLY.	FF-00-00- B 6 1011 0110		HACTIVE = 0, VACTIVE = 1, FIELD = 0, NVRESET = 1,	Indicates the arrival of last active line during active video.
SAV	Next pixel is first pixel of first inactive line.	FF-00-00- A B 1010 1011		HACTIVE = 1, VACTIVE = 0, FIELD = 0, NVRESET = 1,	Next pixel will be on the first vertical blanking line.
EAV	Previous pixel was last pixel of the line immediately before NVRESET goes low.	FF-00-00- F 1 1111 0001		HACTIVE = 0, VACTIVE = 0, FIELD = 0, NVRESET = 1,	Last line before NVRESET becomes active low.

Table 2-6. VIP SAV and EAV Codes Under Full Resolution *(3 of 3)*

Code Type	Event Description	Inserted Headers and 'raster' Reference Code		Corresponding Discrete Pin/Signal	Comments
	TASKS (Active Video or VBI Mode)	Field ID			
		Odd	Even		
SAV	Next pixel is first pixel of the first inactive line after NVRESET has gone low.	FF-00-00- E C 1110 1100		HACTIVE = 1, VACTIVE = 0, FIELD = 0, NVRESET = 1,	Next pixel is first pixel of the first inactive line after NVRESET has gone low.
EAV	Previous pixel was last pixel of the line immediately before VBI mode is enabled.	FF-00-00- 7 F 0111 1111		HACTIVE = 0, VACTIVE = 0, FIELD = 0, NVRESET = 0,	Last line before VBI mode is enabled.
SAV	Next pixel is first pixel of line immediately after VBI mode is enabled.		FF-00-00- 6 2 0110 0010	HACTIVE = 1, VACTIVE = 0, FIELD = 1, NVRESET = 1,	VBIEN signal triggers data in VBI lines to be processed.
EAV	Previous pixel was last pixel in vertical blanking interval during VBI mode.		FF-00-00- D A 1101 1010	HACTIVE = 0, VACTIVE = 0, FIELD = 1, NVRESET = 1,	Last line before active video lines.
SAV	Next pixel is first pixel of first active 'acquired' line.		FF-00-00- C 7 1100 0111	HACTIVE = 1, VACTIVE = 1, FIELD = 1, NVRESET = 1,	—
Pixel	Invalid pixel data clock between SAV and EAV, do not capture and do not increment	00		VALID = 0	Value 00 is not compliant with ITU-R-656, but is compatible with straightforward encoder and decoder logic implementation. 00 and FF are not valid pixel values.

VIP APPLICATION NOTES:

1. Certain VIP applications, such as a VCR in fast forward mode, can move the memory pointer of a FIFO to a new field, at the leading edge of VRESET instead of the leading edge of VACTIVE. In the Bt835, the NVRESET signal is used instead to indicate that VRESET is an active low signal. During VIP mode, Field ID is gated by NVRESET, and the Field ID transitions at the leading edge of NVRESET. However, if the leading edge of VACTIVE arrives before the trailing edge of NVRESET, the memory pointer may move to a new location prematurely, causing the first line of one field to be written at the bottom of another field. Thus, we recommend that the leading edge of VACTIVE be used to move the memory pointer of a FIFO in VCR applications.
2. During vertical scaling, the VALID and HACTIVE signals are gated off. This means that during a dropped line, no SAV or EAV codes are generated. And because the VALID signal is gated off, all pixels are treated as invalid pixels. Only invalid code 00 is inserted into the data stream of dropped lines. However, in the Bt835, HACTIVE is held HIGH, and VALID is held LOW during vertical scaling. This behavior causes a SAV code to be generated at the start of active video, but an EAV code does not get generated until after all dropped lines are filled with hex 00. EAV codes follow invalid data lines but precede another valid pixel line.
3. During temporal decimation, VACTIVE signal is forced inactive during a dropped field or frame. This means that although SAV and EAV codes are generated, all lines are being treated as occurring in the vertical blanking interval. Thus, vertical blanking ID, V bit, must be set to HIGH during dropped fields, indicating vertical blanking. However, the Bt835 does not support the temporal decimation of fields or frames in VIP.

2.2.6 CCIR601 Compliance

When the RANGE bit is set to zero, the output levels are fully compliant with the CCIR601 recommendation. CCIR601 specifies that nominal video has Y values ranging from 16 to 235, and Cr and Cb values ranging from 16 to 240. Excursions outside this range are allowed to handle non-standard video. It is mandatory that 0 and 255 be reserved for timing information.

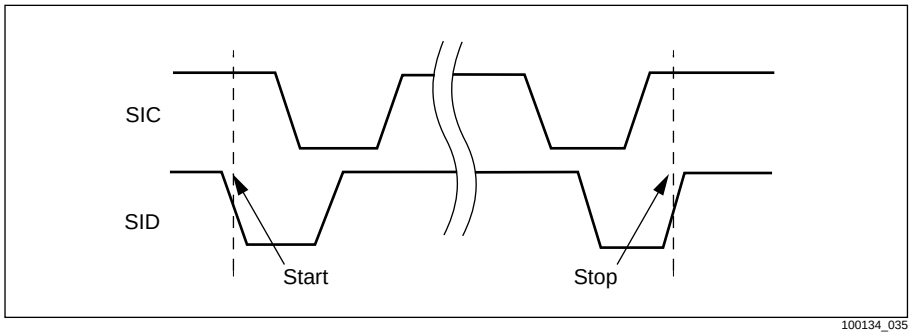
2.3 Serial Interface

The Bt835 communicates over a two-wire serial interface. Serial Clock (SIC) and Data Lines (SID) are used to transfer data between the bus master and the slave device. The Bt835 transfers data at a maximum rate of 100 kbps, and operates as a slave device.

2.3.1 Starting and Stopping

The relationship between SIC and SID is decoded to provide both a start and stop condition on the bus. To initiate a transfer on the serial interface bus, the master must transmit a start pulse to the slave device. This is accomplished by taking the SID line low while the SIC line is held high. The master should only generate a start pulse at the beginning of the cycle, or after the transfer of a data byte to or from the slave. To terminate a transfer, the master must take the SID line high while the SIC line is held high. The master can issue a stop pulse at any time during a cycle. Since the interface will interpret any transition on the SID line during the high phase of the SIC line as a start or stop pulse, care must be taken to ensure that data is stable during the high phase of the clock. This is illustrated in Figure 2-18.

Figure 2-18. The Relationship between SIC and SID



2.3.2 Addressing the Bt835

The Bt835 serial interface slave address consists of two parts: a 7-bit base address and a single bit R/$\overline{W}$ command. The R/$\overline{W}$ bit is appended to the base address to form the transmitted address, as illustrated in Figure 2-19 and Table 2-7.

Figure 2-19. Serial Interface Slave Address Configuration

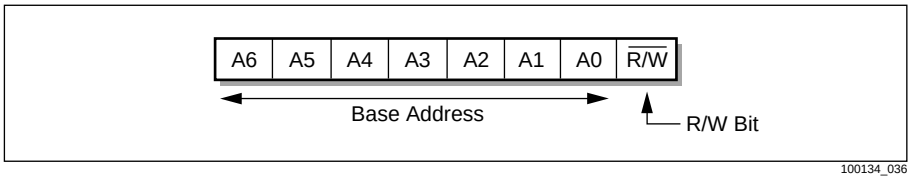


Table 2-7. Bt835 Address Matrix

Serial Address	ALTADDR Pin	Bt835 Base	R/$\overline{W}$ Bit	Action
88	0	10001000	0	Write
		10001000	1	Read
8A	1	10001010	0	Write
		10001010	1	Read

2.3.3 Reading and Writing

After transmitting a start pulse to initiate a cycle, the master must address the Bt835. To do this, the master must transmit one of the four valid Bt835 addresses, with the Most Significant Bit (MSB) transmitted first. After transmitting the address, the master must release the SID line during the low phase of the SIC and wait for an acknowledge. If the transmitted address matches the selected Bt835 address, the Bt835 responds by driving the SID line low, generating an acknowledge to the master. The master samples the SID line at the rising edge of the SIC line, and proceeds with the cycle. If no device responds, including the Bt835, the master transmits a stop pulse and ends the cycle.

If the slave address R/$\overline{W}$ bit is low (indicating a write) the master transmits an 8-bit byte to the Bt835, with the MSB transmitted first. The Bt835 acknowledges the transfer and loads data into its internal address register. The master then issues a stop command, a start command, or transfers another 8-bit byte, MSB first, which is loaded into the register specified to by the internal address register. The Bt835 then acknowledges the transfer and increments the address register in preparation for the next transfer. As before, the master may issue a stop command, a start command, or transfer another 8 bits to be loaded into the next location.

If the slave address R/$\overline{W}$ bit is high (indicating a read), the Bt835 transfers the contents of the register specified to by its internal address register, MSB first. The master acknowledges receipt of the data and pulls the SID line low. As with the write cycle, the address register is auto-incremented, in preparation for the next read.

To stop a read transfer, the host must *not* acknowledge the last read cycle. The Bt835 will then release the data bus in preparation for a stop command. If an acknowledge is received, the Bt835 proceeds to transfer the next register.

When the master generates a read from the Bt835, the Bt835 starts its transfer from whatever location is currently loaded in the address register. Because the address register might not contain the address of the desired register, the master executes a write cycle and sets the address register to the desired location. After receiving an acknowledgment for the transfer of data into the address register, the master initiates a read of the Bt835 by starting a new serial interface cycle with an appropriate read address. The Bt835 then transfers the contents of the desired register.

For example, to read register 0x0A, brightness control, the master starts a write cycle with an address of 0x88 or 0x8A. After receiving an acknowledge from the Bt835, the master transmits the desired address, 0x0A. After receiving an acknowledgment, the master then starts a read cycle with a slave address of 0x89 or 0x8B. The Bt835 acknowledges transfer and then transfers the contents of register 0x0A. Issuing a stop command after the write cycle is not needed. The Bt835 detects the repeated start command and starts a new cycle. This process is illustrated in Table 2-8 and Figure 2-20.

For detailed information on the serial interface, refer to *The I²C-Bus Reference Guide,* reprinted by Conexant.

Table 2-8. Example Serial Interface Data Transactions *(1 of 2)*

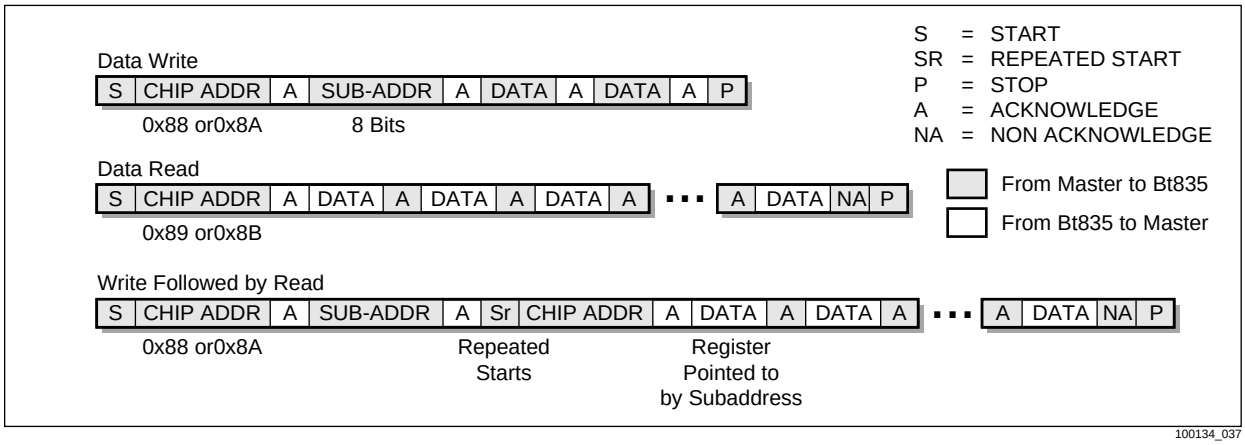
Master	Data Flow	Bt835	Comment
Write to Bt835			
Start	——>		Master sends Bt835 chip address, i.e., 0x88 or 0x8A.
		ACK	Bt835 generates ACK on successful receipt of chip address.
subaddress	——>		Master sends subaddress to Bt835.
		ACK	Bt835 generates ACK on successful receipt of subaddress.
Data(0)	——>		Master sends first data byte to Bt835.
		ACK(0)	Bt835 generates ACK on successful receipt of 1st data byte.
.	——>	.	
.	——>	.	
.	——>	.	
Data(n)	——>		Master sends nth data byte to Bt835.
		ACK(n)	Bt835 generates ACK on successful receipt of (n) data byte.
Stop			Master generates STOP to end transfer.

Table 2-8. Example Serial Interface Data Transactions *(2 of 2)*

Master	Data Flow	Bt835	Comment
Read from Bt835			
Start	——>		Master sends Bt835 chip address, i.e., 0x89 or 0x8B.
		ACK	Bt835 generates ACK on successful receipt of chip address.
	<——	Data(0)	Bt835 sends first data byte to Master.
ACK(0)			Master generates ACK on successful receipt of 1st data byte.
.	<——	.	
.	<——	.	
.	<——	.	
	<——	Data(n-1)	Bt835 sends (n-1) data byte to Master.
ACK(n-1)			Master generates ACK on successful receipt of (n-1) data byte.
	<——	Data(n)	Bt835 sends (n) data byte to Master.
NO ACK			Master does not acknowledge nth data byte.
Stop			Master generates STOP to end transfer.

NOTE(S):
where: Start — Start condition and Bt835 chip address (including the R/$\overline{W}$ bit).
Subaddress — The 8-bit subaddress of the Bt835 register, MSB first.
Data(n) — The data to be transferred to/from the addressed register.
Stop — Stop condition.

Figure 2-20. Serial Interface Protocol Diagram



2.3.4 Software Reset

The contents of the control registers can be reset to their default values by issuing a software reset. A software reset can be accomplished by writing any value to subaddress 0x1F. A read of this location returns an undefined value.

2.4 JTAG Interface

2.4.1 Need for Functional Verification

As the complexity of imaging chips increases, the need to easily access individual chips for functional verification becomes vital. The Bt835 incorporates special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group. Conforming to IEEE P1149.1 "Standard Test Access Port and Boundary Scan Architecture," the Bt835 has dedicated pins that are used for testability purposes only.

2.4.2 JTAG Approach to Testability

JTAG's approach to testability uses boundary scan cells placed at each digital pin and at the digital interface (a digital interface is the boundary between an analog block and a digital block within the Bt835). All cells are interconnected into a boundary scan register that applies or captures test data to verify functionality of the integrated circuit. JTAG is particularly useful for board testers using functional testing methods.

JTAG consists of five dedicated pins comprising the Test Access Port (TAP). These pins are Test Mode Select (TMS), Test Clock (TCK), Test Data Input (TDI), Test Data Out (TDO) and Test Reset ($\overline{\text{TRST}}$). The $\overline{\text{TRST}}$ pin will reset the JTAG controller when pulled low at any time. Verification of the integrated circuit and its connection to other modules on the printed circuit board can be achieved through these five TAP pins. With boundary scan cells at each digital interface and pin, the Bt835 has the capability to apply and capture the respective logic levels. Because all the digital pins are interconnected as a long shift register, the TAP logic has access and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned on the TDO pin and is externally checked. While isolating the Bt835 from other components on the board, the user has easy access to all Bt835 digital pins and digital interfaces through the TAP and can perform complete functionality tests without using expensive bed-of-nails testers.

2.4.3 Optional Device ID Register

The Bt835 has the optional device identification register defined by the JTAG specification. This register contains information concerning the revision, actual part number, and manufacturer's identification code specific to Conexant. This register can be accessed through the TAP controller via an optional JTAG instruction. Refer to Table 2-9.

Table 2-9. Device Identification Register

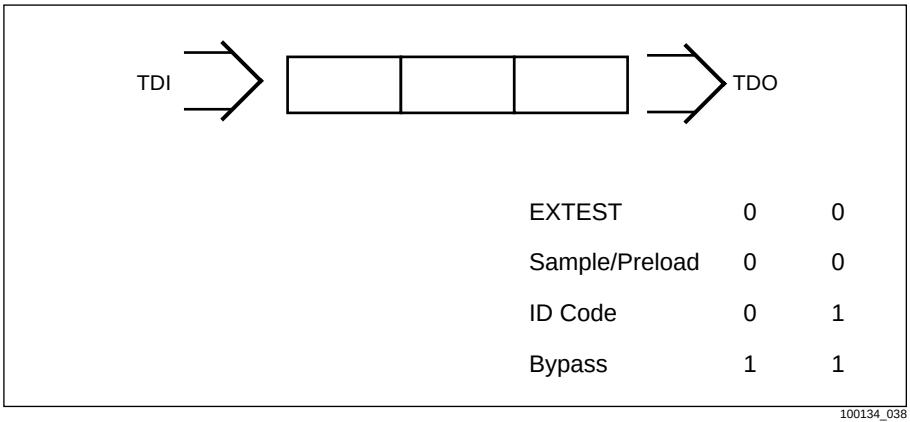
Version				Part Number														Manufacturer ID											
X	X	X	X	0	0	0	0	0	0	1	1	0	1	0	0	0	0	1	1	0	0	0	1	1	0	1	0	1	1	0	1
0				0835, 0x0343														0x0D6											
4 Bits				16 Bits														11 Bits											

2.4.4 Verification with the Tap Controller

A variety of verification procedures can be performed through the TAP controller. Using a set of four instructions, the Bt835 can verify board connectivity at all digital interfaces and pins. The instructions can be accessed by using a state machine standard to all JTAG controllers. These are Sample/Preload, Extest, ID Code, and Bypass illustrated in Figure 2-21. Refer to the IEEE P1149.1 specification for details concerning the instruction register and JTAG state machine.

Conexant has created a BSDL file with the AT&T BSD editor. Should JTAG testing be implemented, an ASCII version of the complete BSDL file can be obtained by contacting your local Conexant sales office.

Figure 2-21. Instruction Register



3.0 PC Board Layout Consideration

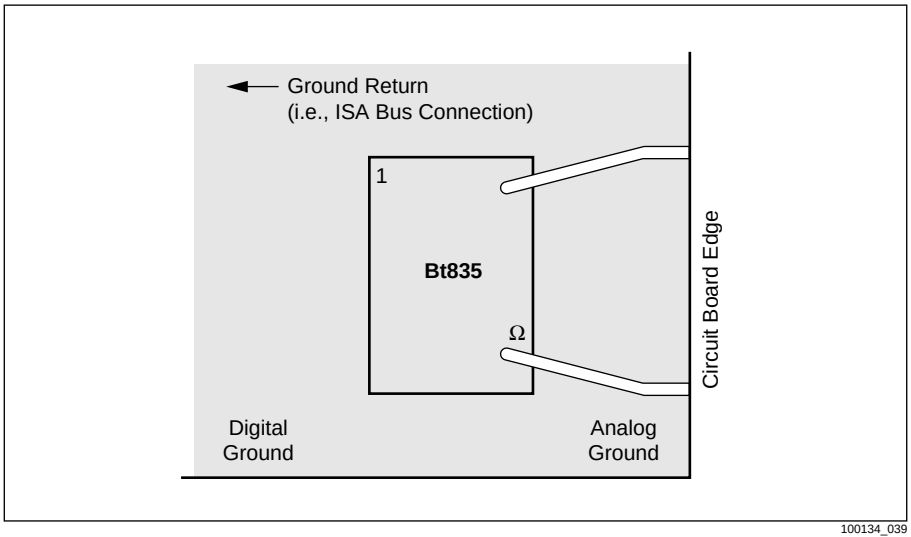
The layout for the Bt835 power and ground lines should be optimized for the lowest noise. This is accomplished by shielding the digital inputs and outputs and by providing good decoupling. The lead length between groups of power and ground pins should be minimized to reduce inductive ringing.

3.1 Ground Planes

The ground plane area should encompass all Bt835 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt835, analog input traces, any input amplifiers, and all digital signal traces leading to the Bt835.

The Bt835 has digital grounds (GND) and analog grounds (AGND). The layout for the ground plane should be set up so the two planes are at the same electrical potential, but they should be isolated from each other in the areas surrounding the chip. The return path for the current should occur through the digital plane. Figure 3-1 illustrates an example of ground plane layout.

Figure 3-1. Example Ground Plane Layout

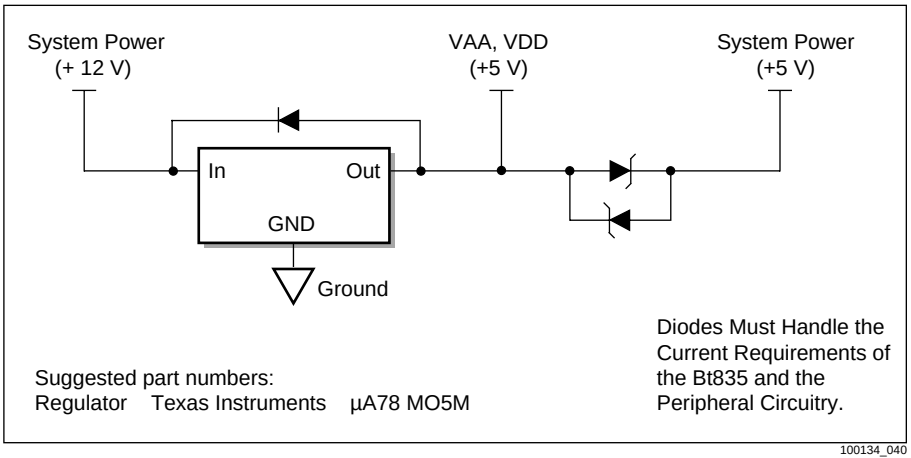


3.2 Power Planes

The power plane area should encompass all Bt835 power pins, the voltage reference circuitry, the power supply bypass circuitry, the analog input traces, any input amplifiers, and all the digital signal traces leading to the Bt835.

The Bt835 has digital power (VDD) and analog power (VAA). The layout for the power plane should be set up so the two planes are at the same electrical potential, but they should be isolated from each other in the areas surrounding the chip. Also, the current's return path should occur through the digital plane. This is the same layout as illustrated for the ground plane in Figure 3-1. The design of the Bt835 makes use of a regulator unnecessarily. While the Bt835 does not require its use, certain hostile environments may make its use desirable. In this event, and where power sequencing is a concern, the circuit in Figure 3-2 illustrates the desired scheme.

Figure 3-2. Optional Regulator Circuitry for 5 V Systems



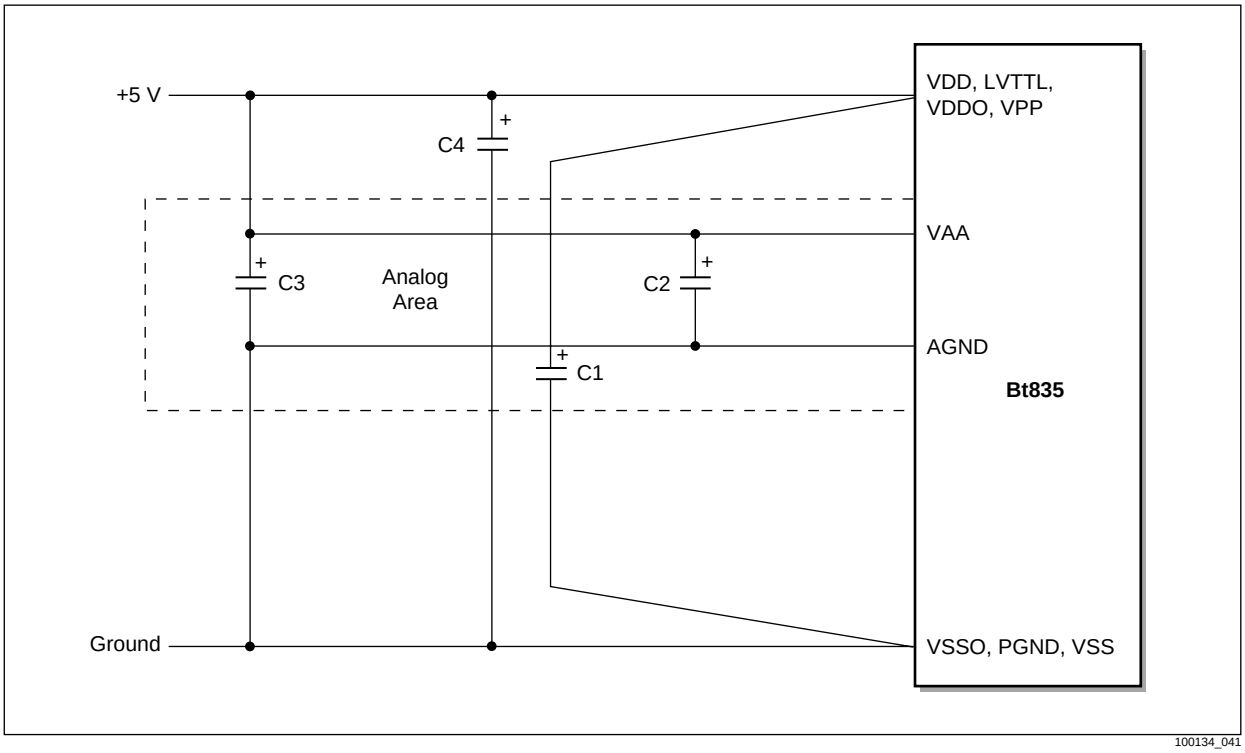
3.3 Supply Decoupling

Bypass capacitors should be installed with the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. These capacitors should also be placed as close as possible to the device.

Each group of VAA and VDD pins should have a 0.1 µF ceramic bypass capacitor to ground, located as close as possible to the device.

Additionally, 10 µF capacitors should be connected between the analog power and ground planes, as well as between the digital power and ground planes. These capacitors are at the same electrical potential, but provide additional decoupling by being physically close to the Bt835 power and ground planes. Figures 3-3 and 3-4 illustrate additional information about power supply decoupling.

Figure 3-3. Typical Power and Ground Connection Diagram and Parts List for 5 V I/O Mode



Location	Description	Vendor Part Number
C1, C2(1)	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C3, C4(2)	10 µF tantalum capacitor	Mallory CSR13G106KM

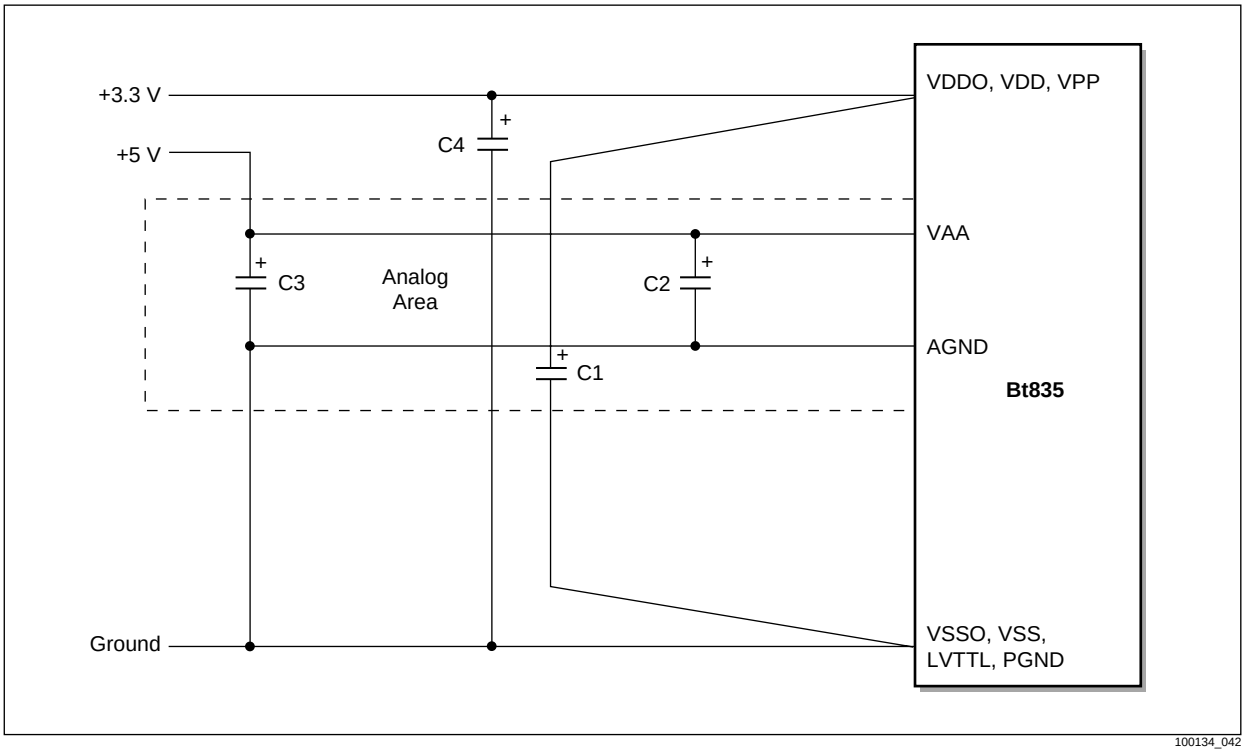
NOTE(S):

(1) A 0.1 µF capacitor should be connected between each group of power pins and ground as close to the device as possible (ceramic chip capacitors are preferred).

(2) The 10 µF capacitors should be connected between the analog supply and the analog ground, as well as the digital supply and the digital ground. These should be connected as close to the Bt835 as possible.

3. Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt835.

Figure 3-4. Typical Power and Ground Connection Diagram and Parts List for 3.3 V I/O Mode



Location	Description	Vendor Part Number
C1, C2*(1)*	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C3, C4*(2)*	10 µF tantalum capacitor	Mallory CSR13G106KM

NOTE(S):

(1) A 0.1 µF capacitor should be connected between each group of power pins and the ground, as close to the device as possible (ceramic chip capacitors are preferred).

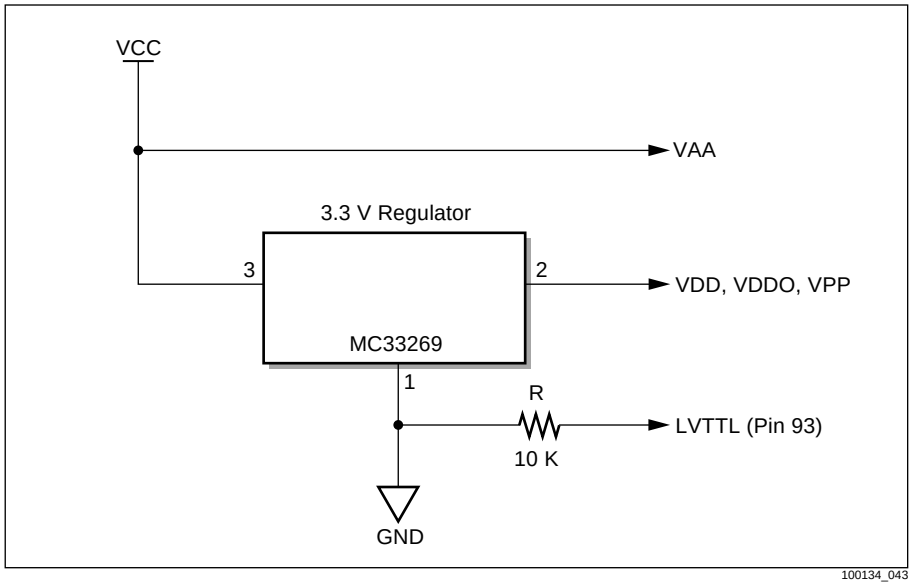
(2) The 10 µF capacitors should be connected between the analog supply and the analog ground, as well as the digital supply and the digital ground. These should be connected as close to the Bt835 as possible.

3. Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt835.

3.4 Voltage Regulator Circuit

Figure 3-5 illustrates a regulator circuit that can be used to operate the digital portion of the Bt835 at 3.3 V. For simplicity, supply decoupling is not shown here; please refer to Figure 3-4. The analog power supply must always remain at 5 V. All digital power, including VDD, VDDO, and VPP, must be run at either 3.3 V or 5 V. The part may be damaged if all of the digital power is not run at the same supply voltage. The LVTTL pin must be tied to ground for digital 3.3 V operation, and tied to VCC for digital 5 V operation.

Figure 3-5. Optional 3.3 V Regulator



3.5 Power-Up Sequencing

Time between analog and digital power application to the Bt835 should always be kept to a minimum. Although it is very difficult to apply all power at exactly the same time, analog and digital power should be applied as closely together as possible.

3.6 Digital Signal Interconnect

The digital signals of the Bt835 should be isolated as much as possible from the analog signals and other analog circuitry. Also, the digital signals should not overlay the analog power plane.

Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

3.7 Analog Signal Interconnect

Long lengths of closely spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the YIN and CIN inputs.

Also, high-speed TTL signals should not be routed close to the analog signals to minimize noise coupling.

3.8 Latchup Avoidance

Latchup is a failure mechanism inherent to any CMOS device. It is triggered by static or impulse voltages on any signal input pin exceeding the voltage on the power pins by more than 0.5 V, or falling below the GND pins by more than 0.5 V. Latchup can also occur if the voltage on any power pin exceeds the voltage on any other power pin by more than 0.5 V.

In some cases, devices with mixed signal interfaces, such as the Bt835, can appear more sensitive to latchup. In reality, this is not the case. However, mixed signal devices tend to interact with peripheral devices such as video monitors or cameras that are referenced to different ground potentials, or apply voltages to the device before its power system is stable. This interaction sometimes creates conditions amenable to the onset of latchup.

To maintain a robust design with the Bt835, the following precautions should be taken:

- Apply power to the device before or at the same time as the interface circuitry.
- Do not apply voltages below GND–0.5 V, or higher than VAA+0.5 V to any pin on the device. Do not use negative supply op amps or any other negative voltage interface circuitry. All logic inputs should be held low until power to the device has settled to the specified tolerance.
- Connect all VDDO, VPP, and VDD pins together through a low impedance plane.
- Connect all VSSO, VSS, and PGND pins together through a low impedance plane.

3.9 Sample Schematics

An example of a Bt835 typical circuit schematic is illustrated in Figure 3-6.

Figure 3-6. Bt835 Typical Circuit Schematic *(1 of 5)*

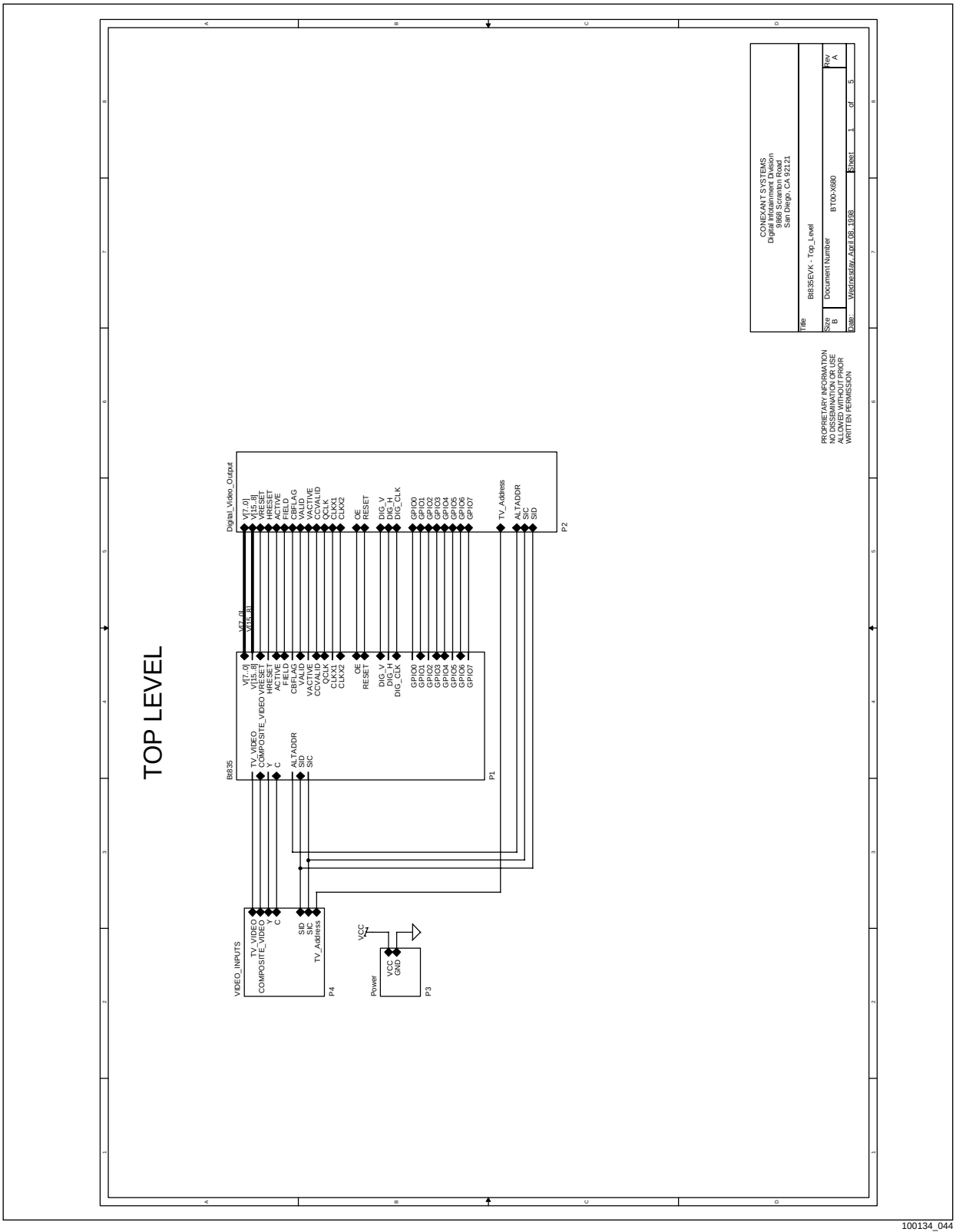
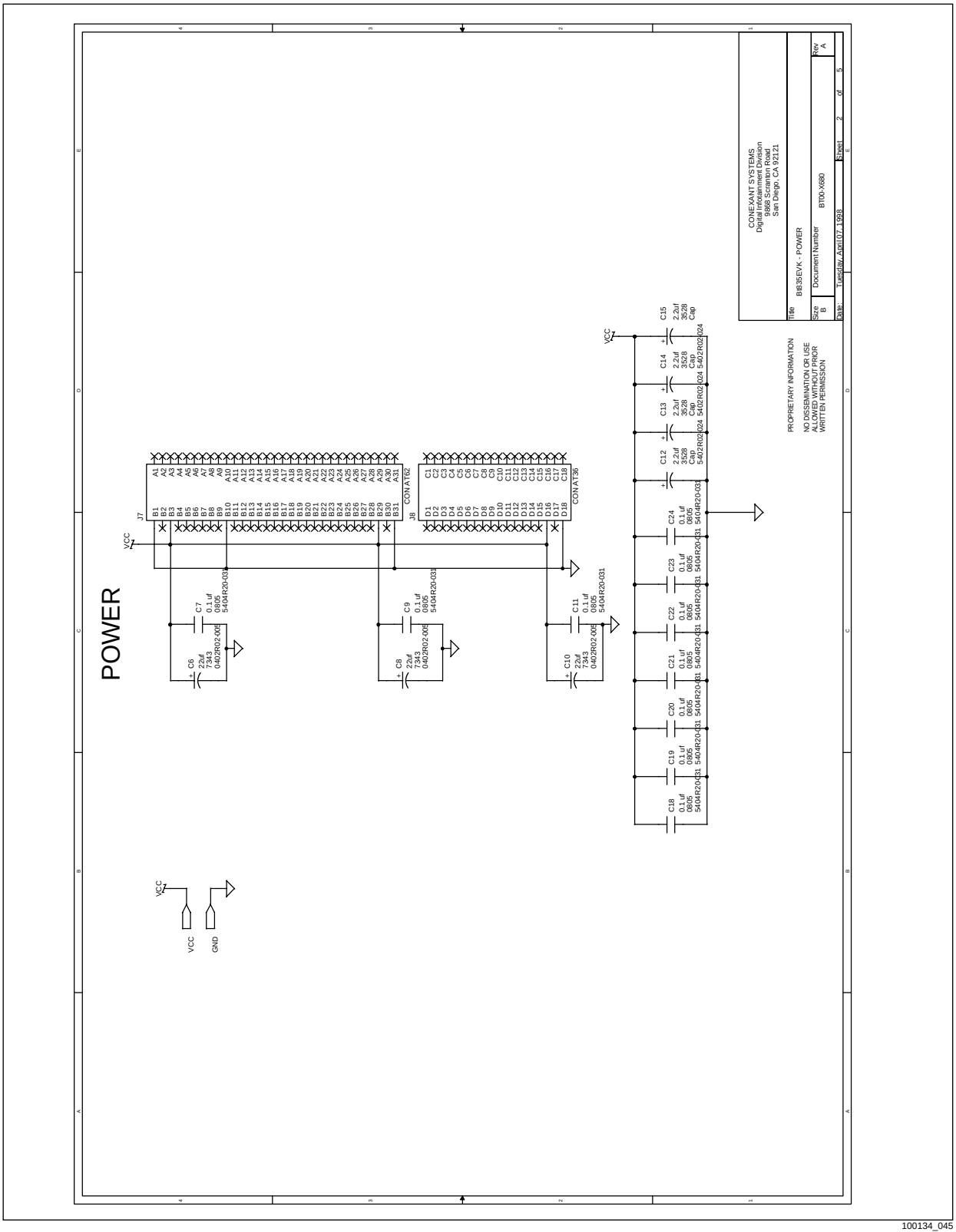
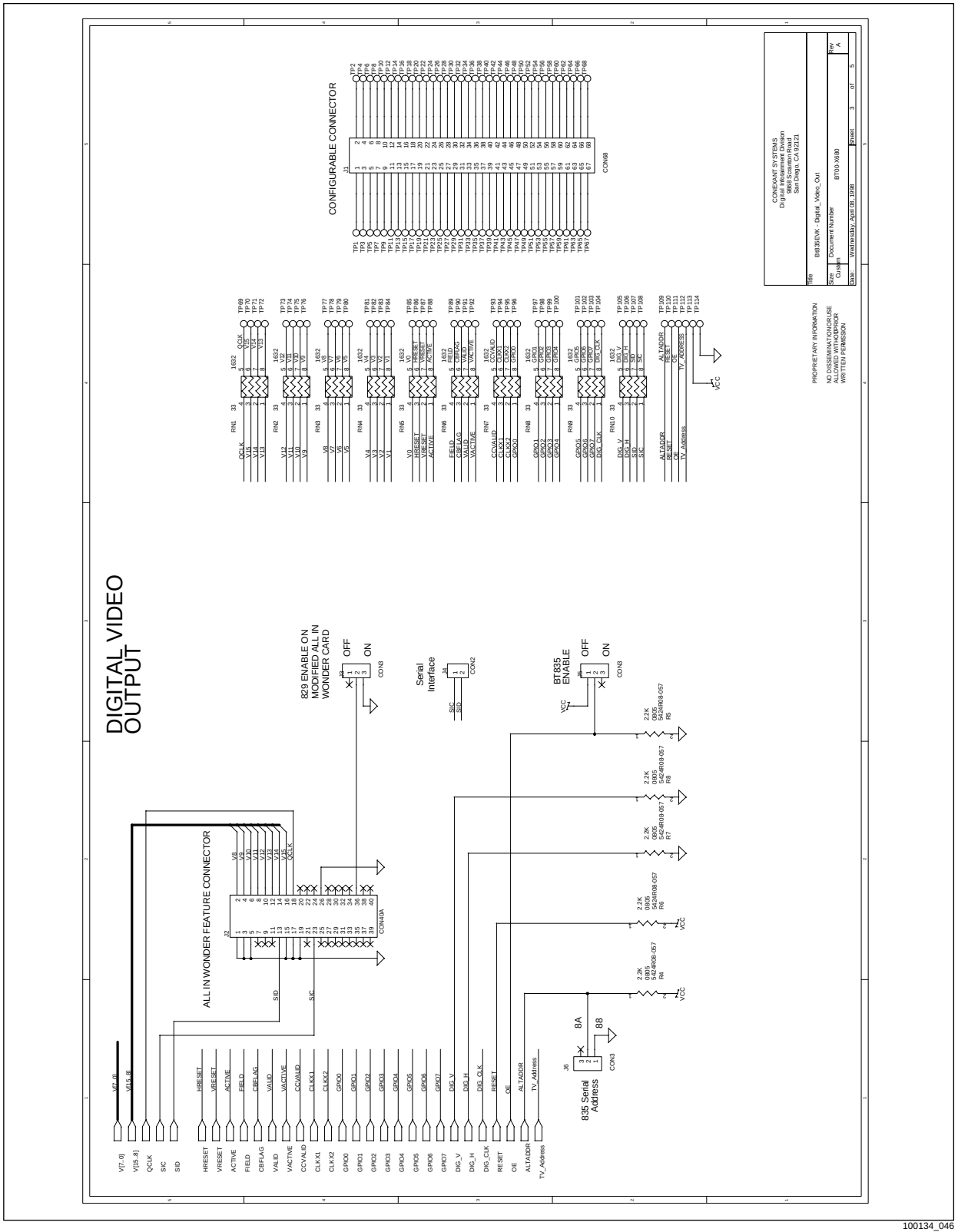


Figure 3-6. Bt835 Typical Circuit Schematic *(2 of 5)*



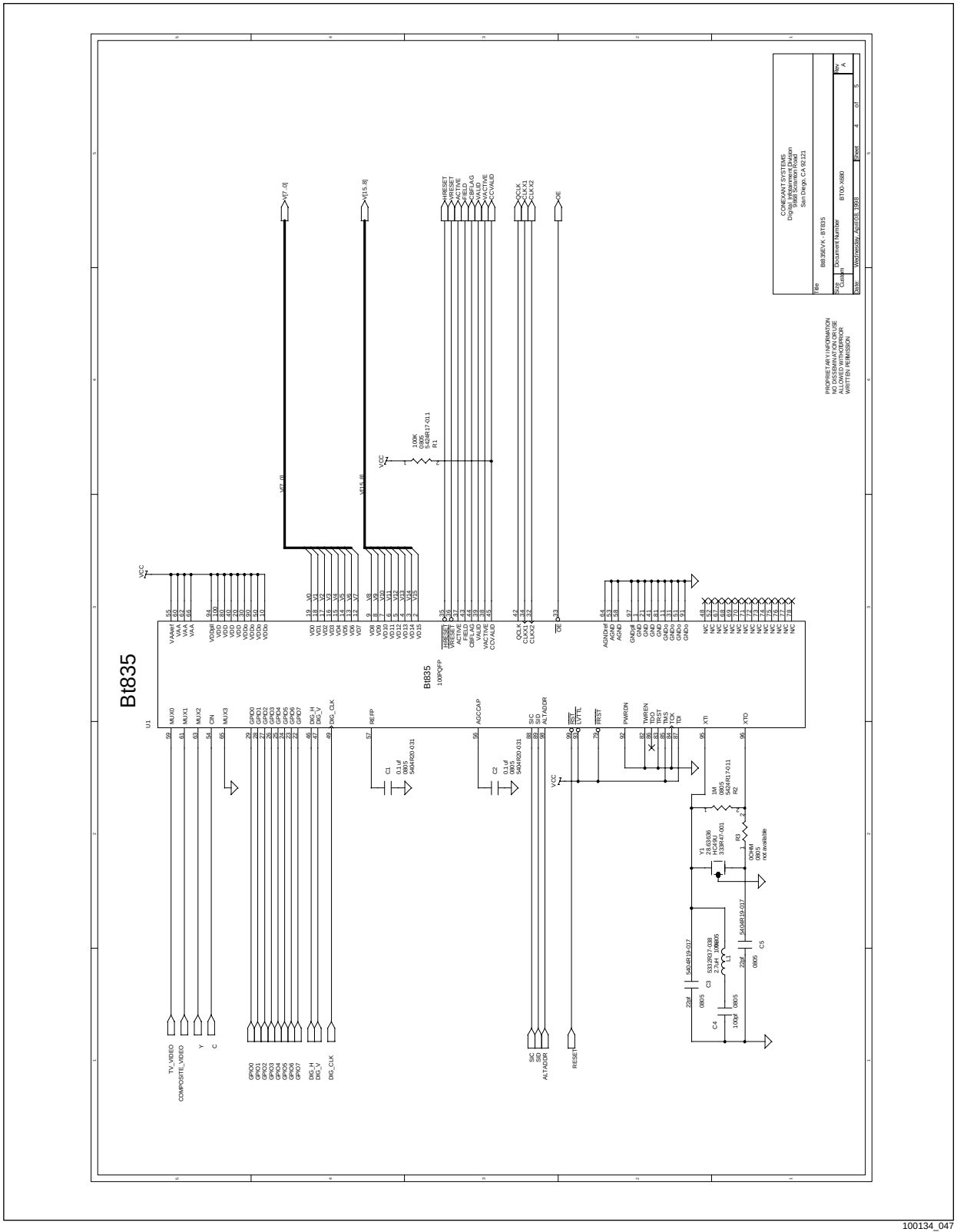
100134_045

Figure 3-6. Bt835 Typical Circuit Schematic *(3 of 5)*



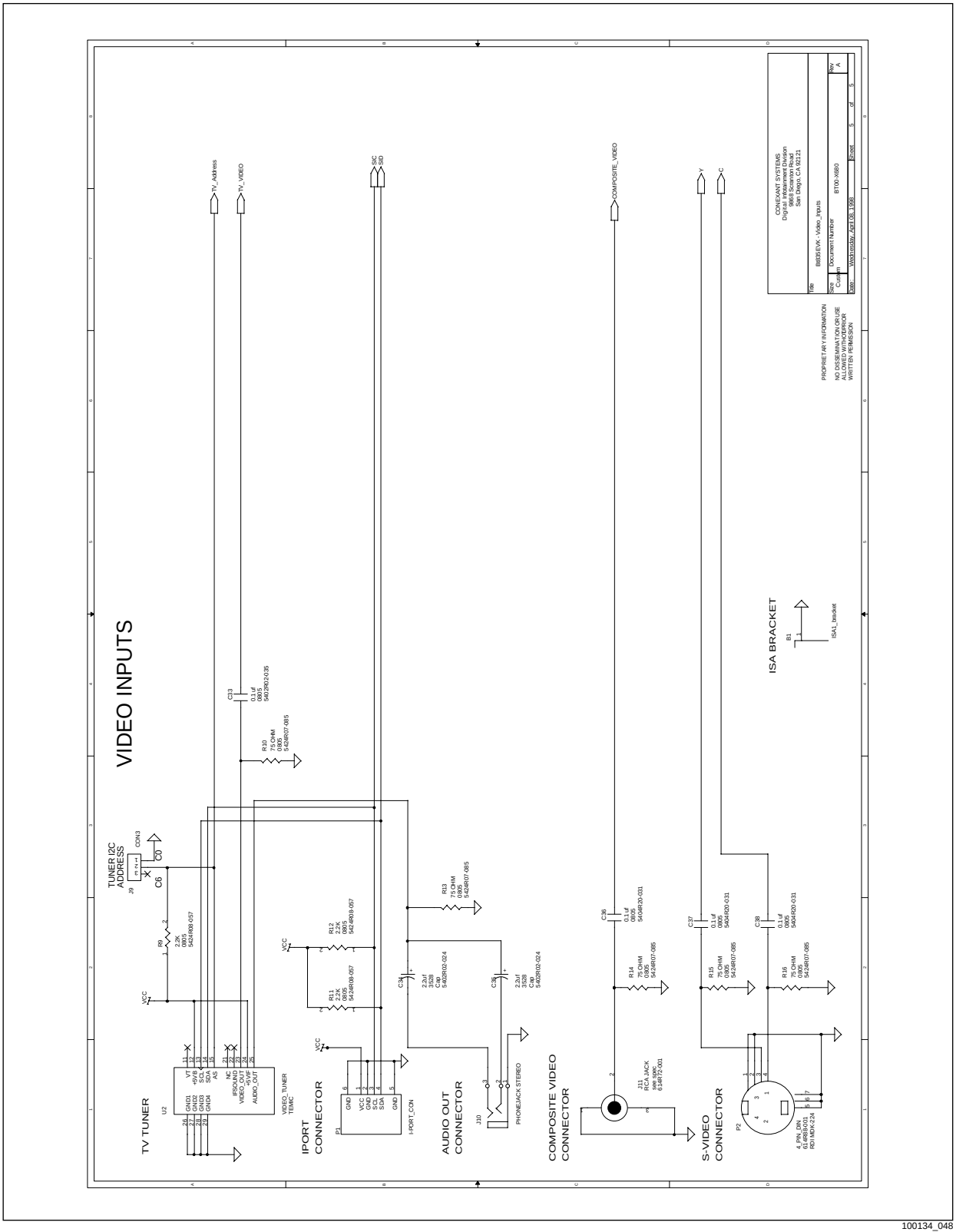
100134_046

Figure 3-6. Bt835 Typical Circuit Schematic *(4 of 5)*



100134_047

Figure 3-6. Bt835 Typical Circuit Schematic *(5 of 5)*



100134_048

4.0 Control Register Description

Registers in the Bt835 are either 8-bit or 16-bit registers. The 16-bit registers require two 8-bit register addresses, and are arranged in little endian format. Little endian format has the LSBs of the 16-bit word stored at the lower address and the MSBs stored in the upper address.

0x00—STATUS (DEFAULT 0x00)

The STATUS register reports status from various decoder functions. The MPU can read or write to this register at anytime. Writing 1s or 0s to the register resets it to its default of 0x00. The COF and LOF status bits hold their values until reset to their default values. The other six bits do not hold their values, but continually output the status. COF is the LSB.

7	6	5	4	3	2	1	0
VPRES	HLOCK	FIELD	NUML	PLL	CCVLD	LOF	COF

VPRES Video Present

0—No video detected (DEFAULT)
1—Video detected

HLOCK Horizontal Lock

0—Not locked (DEFAULT)
1—Locked

FIELD Field Identifier

0—Odd field (DEFAULT)
1—Even field

NUML Number of lines per frame

0—525 (DEFAULT)
1—625

PLL PLL Lock

0—PLL not locked (DEFAULT)
1—PLL locked

CCVLD CC Data Valid

0—No CC/EDS data (DEFAULT)
1—CC/EDS data available

LOF Luma ADC overflow. Indeterminate when ADC is sleeping.

0—Normal (DEFAULT)
1—Luma ADC overflow

COF Chroma ADC overflow. Indeterminate when ADC is sleeping.

0—Normal (DEFAULT)
1—Chroma ADC overflow

0x01—INPUT (DEFAULT 0x00)

The INPUT register controls the format of the incoming video, which mux input is being used, and the source of the sample clock. The details of this register are given below.

7	6	5	4	3	2	1	0
Reserved	MUXS[1:0]		Reserved	FMT[3:0]			

RESERVED Not used. (Set to 0.)

MUXS[1:0] Selects one of four video inputs

00—MUX0 (DEFAULT)
01—MUX1
10—MUX2
11—MUX3

RESERVED Not used. (Set to 0.)

FMT[3:0] Selects input video format

0000—Auto Line Count detection (DEFAULT)

Auto line count detection automatically reprograms the PLL for the line count detected. The Bt835 determines the video source input to the chip by counting the number of lines in a frame. Auto line count detection brings the Bt835 closer to a correct image. Further programming is required to refine the signal, based on the input standard (see Table 1-4).

0001—NTSC-M
0010—NTSC-J (No 7.5% setup)
0011—NTSC-4.43
0100—PAL-BDGHI
0101—PAL-M
0110—PAL-N
0111—PAl-Nc
1000—PAL-60
1001—SECAM

0x03, 0x02—VDELAY (DEFAULT 0x0016)

The VDELAY register is a 16-bit register which occupies two address locations, starting at 0x02. VDELAY, as with all 16-bit registers in the Bt835, is little endian. That is, the LSBs are stored at the lower address, and the MSBs are stored in the upper address. In this case, VDELAY[7:0] are at location 0x02, while VDELAY[15:8] are at location 0x03. Values between 1 and 1023, inclusive, can be programmed into the VDELAY register.

0x05, 0x04—VACTIVE (DEFAULT 0x01E0)

The VACTIVE register is a 16-bit register, starting at location 0x04. Values between 0 and 1023, inclusive, can be programmed into the VACTIVE register.

0x07, 0x06—HDELAY (DEFAULT 0x0078)

The HDELAY register is a 16-bit register, starting at location 0x06. Values between 1 and 1023, inclusive, can be programmed into the HDELAY register.

0x09, 0x08—HACTIVE (DEFAULT 0x0280)

The HACTIVE register is a 16-bit register, starting at location 0x08. Values between 0 and 1023, inclusive, may be programmed into the HACTIVE register. Default produces 640 active pixels for NTSC.

0x0B, 0x0A—HSCALE (DEFAULT 0x02AC)

The HSCALE register is a 16-bit register, starting at location 0x0A. This register is programmed according to the equations given in Section 1.6.5.

0x0D, 0x0C—VSCALE (DEFAULT 0x0000)

The VSCALE register is a 16-bit register starting at location 0x0C. The VSCALE value is a 13 bit value, stored in the LSBs of the register. This register is programmed according to the equations given Section 1.6.5.

0x0E—VSCALE_CTL (DEFAULT 0x00)

The VSCALE_CTL register configures the vertical scaler.

7	6	5	4	3	2	1	0
Reserved	COMB[1:0]		NVINT	FIELD	VFILT[2:0]		

RESERVED Not used. (Set to 0.)

COMB[1:0] Comb Filter selection.

00—Full Comb filter (DEFAULT)
01—Chroma Comb filter ONLY
10—RSRVD
11—No Comb Filter

NVINT VS Interlace Format. Configures interpolation filters to optimize interfield artifacts/sharpness tradeoffs for interlace/non-interlace reconstruction of display.

0—Non-Interlace VS (DEFAULT) Used for single field capture.
1—Interlace VS Used for capturing both fields

FIELD Interfield interpolation

0—Disables interfield interpolation (DEFAULT)
1—Enables interfield interpolation

VFILT[2:0] Vertical filter format (see Table 1-5 for proper selection).

000—2 tap and Interpolation (DEFAULT)
001—3 tap and Interpolation
010—4 tap and Interpolation
011—5 tap and Interpolation
100—2 tap and No Interpolation
101—3 tap and No Interpolation
110—4 tap and No Interpolation
111—5 tap and No Interpolation

0x0F—TDEC (DEFAULT 0x00)

The TDEC register controls the temporal decimation of the input video stream. Frame and field decimation are not supported in VIP mode (Table 2-6, Note 3).

7	6	5	4	3	2	1	0
DECFLD	FLDALN	DRATE[5:0]					

DECFLD Defines whether decimation is by fields or frames.

0—Decimate frames (DEFAULT)
1—Decimate fields

FLDALN Aligns start of decimation with even or odd field.

0—Start on odd field (DEFAULT)
1—Start on even field

DRATE[5:0] Number of fields or frames dropped out of 50 (625/50) or 60 (525/60). This value should not exceed 60 for 60 Hz systems, or 50 for 50 Hz systems. DEFAULT is 0.

0x10—BRIGHT (DEFAULT 0x00)

The BRIGHT register is an 8-bit register which controls the brightness offset applied to the video. Values from 0x00 to 0xFF are allowed. The two's complement value programmed into this register is added to the decoded luminance portion of the video signal. Brightness is applied after contrast.

0x11—CONTRAST (DEFAULT 0x39)

The CONTRAST register holds the 8-bit contrast value. The decoded luminance portion of the video is multiplied by the contrast value. Values from 0x00 to 0xFF are allowed.

0x12—SAT_U (DEFAULT 0x7F)

The SAT_U register is an 8-bit gain applied to the decoded U vector of the chrominance. Values from 0x00 to 0xFF are allowed. Since U and V are offset in the analog domain, the ratio shown should be maintained for proper angular decoding. CCIR656 sources, however, have no offset, and therefore registers 12 and 13 will need to be set to equal values for this type of source.

0x13—SAT_V (DEFAULT 0x5A)

The SAT_V register is an 8-bit gain applied to the decoded V vector of the chrominance. Values from 0x00 to 0xFF are allowed.

0x14—HUE (DEFAULT 0x00)

The HUE register is an 8-bit value which applies phase offset to the decoders internal subcarrier. Values from 0x00 to 0xFF are allowed.

0x15—CONTROL_0 (DEFAULT 0x00)

7	6	5	4	3	2	1	0
LNOTCH	SVID	LDEC	HFILT[1:0]		PEAKEN	PSEL[1:0]	

LNOTCH Enables luma notch filter.

0—Notch enabled (DEFAULT)
1—Notch disabled

SVID Enables Y/C video. SVID has no effect on LNOTCH.

0—Y/C disabled (DEFAULT)
1—Y/C enabled

LDEC Enables luma filtering.

0—Luma filters enabled (DEFAULT)
1—Luma filters disabled

HFILT[1:0] When LDEC is a 0, used to select which horizontal low pass filter is used.

00—AUTO (DEFAULT)
01—CIF
10—QCIF (Required for SECAM)
11—ICON

PEAKEN Enables luminance peaking filters.

0—Peaking filters disabled (DEFAULT)
1—Peaking filters enabled

PSEL[1:0] Selects peaking response.

00—+2 dB at 3.58/4.43 MHz (DEFAULT)
01—+3.5 dB at 3.58/4.43 MHz
10—+5.0 dB at 3.58/4.43 MHz fsc
11—+6.0 dB at 3.58/4.43 MHz fsc

0x16—CONTROL_1 (DEFAULT 0x1C)

7	6	5	4	3	2	1	0
VBIEN	FRAME	VBITFMT	CAGC	CKILL	SC_SPD	HACT	SCAGC

VBIEN Enables VBI capture.

0—Disable VBI capture (DEFAULT)
1—Enable VBI capture

FRAME VBI Frame (raw) mode.

0—VBI frame mode disabled (DEFAULT)
1—VBI frame mode enabled

VBIFMT VBI Output Format (Byteswap).

0—Pixel N on VD[15:8], Pixel N+1 on VD[7:0] (DEFAULT)
1—Pixel N on VD[7:0], Pixel N+1 on VD[15:8]

CAGC Enables QAM Chroma AGC (for NTSC/PAL).

0—Chroma AGC disabled (SECAM)
1—Chroma AGC enabled (DEFAULT, NTSC/PAL))

CKILL Enable Low color removal.

0—Color killer disabled (SECAM)
1—Color killer enabled (DEFAULT, NTSC/PAL)

SC_SPD Chroma lock speed.

0—Slow
1—Normal (DEFAULT)

HACT HACTIVE extend.

0—Reset HACTIVE with HRESET (DEFAULT)
1—Extend HACTIVE beyond HRESET

SCAGC SECAM Chroma AGC/SECAM color killer.

0—SECAM CAGC/color killer disabled (DEFAULT)
1—SECAM CAGC/color killer enabled

0x17—CONTROL_2 (DEFAULT 0x01)

7	6	5	4	3	2	1	0
YCORE[1:0]		CCORE[1:0]		VIPEN	BSTRM	RANGE	VERTEN

YCORE[1:0] Selectable Luma coring.

00—No luma coring (DEFAULT)
01—8 lsbs
10—16 lsbs
11—32 lsbs

CCORE[1:0] Selectable Chroma coring.

00—No chroma coring (DEFAULT)
01—2 lsbs
10—4 lsbs
11—8 lsbs

VIPEN Enables VIP control code insertion.

0—No VIP control codes (DEFAULT)
1—VIP control codes inserted. SPI Mode 3 (VIP)

BSTRM Enables ByteStream control code insertion.

0—No Bytestream control codes (DEFAULT)
1—ByteStream control codes inserted. SPI Mode 2 (Bytestream)

RANGE Luma output range control.

0—Normal (16–253) (DEFAULT). VIP and Bytestream.
1—Full Range (0–255)

VERTEN Adds vertical detection to VPRES algorithm.

0—No vertical detection
1—Use vertical detection in VPRES (DEFAULT)

0x18—CONTROL_3 (DEFAULT 0xD0)

7	6	5	4	3	2	1	0
NOUTEN	OES[1:0]		LEN	HSFMT	ACTFMT	VLDFMT	CLKGT

NOUTEN Output enable. Works in conjunction with pin 33, $\overline{OE}$. If either $\overline{OE}$ or this register bit = 1 then the outputs are three-stated according to OES[1:0].

0—Enable outputs
1—Three-state outputs selected by OES[1:0] (DEFAULT)

OES[1:0] Output enable select.
OES[1:0] controls which outputs three-state when the $\overline{OE}$ pin or the OUTEN bit is asserted. The pins are divided into three groups: timing ($\overline{HRESET}$, $\overline{VRESET}$, ACTIVE, VACTIVE, CBFLAG, DVALID, and FIELD), clocks (CLKx1, CLKx2, and QCLK), and data (VD[15:0]). CCVALID cannot three state.

00—Three state timing and data only
01—Three state data only
10—Three state all (DEFAULT)
11—Three state clocks and data only

LEN Output bus width.

0—8 bit output on VD[15:8]
1—16 bit output on VD[15:0] (DEFAULT)

HSFMT NHRESET format.

0—NHRESET is 64 CLKX1 cycles (DEFAULT)
1—NHRESET is 1 CLKX1 cycle

ACTFMT ACTIVE format.

0—ACTIVE is composite active (DEFAULT)
1—ACTIVE is horizontal active

VLDFMT VALID format. Controls QCLK and Valid

0—VALID indicates nonscaled pixels. QCLK is gated according to CLKGT, bit 0 and ACTFMT, bit 2. (DEFAULT)
1—VALID is logical AND of nominal VALID and ACTIVE, where ACTIVE is controlled by ACTFMT. QCLK is inverted CLKX1 or CLKX2, and not gated.

CLKGT QCLK gating.

0—CLKx1 (16-bit) or CLKx2 (8-bit) is inverted and gated with VALID and ACTIVE to create QCLK. (DEFAULT)
1—CLKx1 or CLKx2 is inverted and gated with VALID to create QCLK.

0x19—VPOLE (DEFAULT 0x00)

7	6	5	4	3	2	1	0
Reserved	VALID	VACTIVE	CBFLAG	FIELD	ACTIVE	HRESET	VRESET

RESERVED Reserved for future use. (Set to 0.)

VALID

0—VALID pin active high (DEFAULT)
1—VALID pin active low

VACTIVE

0—VACTIVE pin active high (DEFAULT)
1—VACTIVE pin active low

CBFLAG

0—CBFLAG pin active high (DEFAULT)
1—CBFLAG pin active low

FIELD

0—FIELD pin active indicates EVEN field (DEFAULT)
1—FIELD pin active indicates ODD field

ACTIVE

0—ACTIVE pin active high (DEFAULT)
1—ACTIVE pin active low

HRESET

0—HRESET pin active high (DEFAULT)
1—HRESET pin active low

VRESET

0—NVRESET pin active low (DEFAULT)
1—NVRESET pin active high

0x1A—AGC_DELAY (DEFAULT 0x68)

7	6	5	4	3	2	1	0
AGC[7:0]							

AGC[7:0] AGC gate delay for back-porch sampling. Hex value is number of CLKX1 cycles from center of falling edge of HSYNC to center of AGC window. This window is 8 CLKX1 cycles wide, and should be positioned centered over burst. AGC only samples low-pass filtered luma. The following equation should be used to determine the value for this register:

$$ADELAY = (Desired\_Delay * f_{Sample\_Clock}) + 7$$

For example, for an NTSC input signal:

$$ADELAY = (6.8\ \mu s * 14.32\ MHz) + 7$$
$$= 104\ (0x68)$$

0x1B—BG_DELAY (DEFAULT 0x5D)

7	6	5	4	3	2	1	0
BG[7:0]							

BG[7:0] Burst gate delay for sub-carrier sampling. Hex value is number of CLKX1 cycles from center of falling edge of HSYNC to center of burst gate. This should be positioned centered over burst. The following equation should be used to determine the value for this register:

$$BDELAY = (Desired\_Delay * f_{Sample\_Clock})$$

For example, for an NTSC input signal:

$$BDELAY = (6.5\ \mu s * 14.32\ MHz)$$
$$= 93\ (0x5D)$$

0x1C—ADC (DEFAULT 0x02)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	AGC_EN	CLKSLP	YSLP	CSLP	CRUSH

RESERVED Reserved for future use (set to 0).

AGC_EN AGC enable.

0—Enable AGC (DEFAULT)
1—Disable AGC

CLKSLP Sleeps system clock.

0—Normal clock operation (DEFAULT)
1—Sleep system clock. Serial bus is still accessible in this mode.

YSLP Sleep luma ADC.

0—Normal luma ADC operation (DEFAULT)
1—Sleep luma ADC

CSLP Sleep chroma ADC.

0—Normal chroma ADC operation
1—Sleep chroma ADC (DEFAULT)

CRUSH Enable white crush circuitry

0—Disable white crush (DEFAULT)
1—Enable white crush

0x1D—WC_UP (DEFAULT 0xCF)

7	6	5	4	3	2	1	0
MAJS[1:0]		UPCNT[5:0]					

MAJS[1:0] These bits determine the majority comparison point for the white crush up function.

00—3/4 maximum luma
01—1/2 maximum luma
10—1/4 maximum luma
11—Automatic (DEFAULT)

UPCNT[5:0] White crush up count value. Twos complement number, a positive sign bit is assumed.

0x1E—WC_DN (DEFAULT 0x7F)

7	6	5	4	3	2	1	0
Reserved	WCFRM	DNCNT[5:0]					

RESERVED Reserved for future use (set to 0).

WCFRM This bit programs the rate at which the DNCNT and UPCNT values are accumulated.

0—Once per field
1—Once per frame (DEFAULT)

DNCNT[5:0] White crush down count value. Two's complement, a negative sign bit is assumed. DEFAULT (0x3F)

0x1F—CC_STATUS (DEFAULT 0x80)

All bits may be written to, but only bits 4 and 5 are control bits.

7	6	5	4	3	2	1	0
PARERR	INT_EN	EDS	CC	OR	DA	CC/EDS	LO/HI

PARERR Parity Error flag. Status bit.

0—No parity error
1—Odd Parity error (DEFAULT)

INT_EN CCVALID interrupt mask. Status bit. Mirrors what the Bt835 sends to the CC-Valid interrupt pin.

0—CCVALID interrupt masked (DEFAULT)
1—CCVALID interrupts enabled

EDS Enables EDS capture. Control bit.

0—No EDS capture (DEFAULT)
1—EDS capture enabled

CC Enables CC capture. Control bit.

0—No CC capture (DEFAULT)
1—CC capture enabled

OR FIFO overflow. Status bit.

0—No overflow since bit was cleared (DEFAULT)
1—Overflow

DA Data Available. Status bit.

0—FIFO is empty (DEFAULT)
1—One or more bytes available

CC/EDS Status of current byte in FIFO.

0—CC byte (DEFAULT)
1—EDS byte

LO/HI Status of current byte in FIFO.

0—Low byte (DEFAULT)
1—High byte

0x20—CC_DATA (DEFAULT 0xB8)

7	6	5	4	3	2	1	0
CCDATA[7:0]							

CCDATA[7:0] Captured CC or EDS data.

0x21—GPIO (DEFAULT 0x00)

The GPIO register is an eight bit register which either drives the GPIO pins or reflects their state. Writes to this register drive the related GPIO pins. Reads reflect the status of the GPIO pins. To properly read a GPIO pin, it must be three stated via the GPIO_NOE register.

7	6	5	4	3	2	1	0
GPIO[7:0]							

GPIO[7:0] GPIO Data

0x22—GPIO_NOE (DEFAULT 0xFF)

The GPIO_NOE register controls the drive of each GPIO pin. The reset condition three states all GPIO pins. This allows the user to configure the power-up condition of their board.

7	6	5	4	3	2	1	0
NOE[7:0]							

NOE[7:0] Three state controls for the GPIO pins.

0—GPIO outputs enabled.
1—GPIO outputs three stated (DEFAULT).

0x23—VSIF (DEFAULT 0x00)

The VSIF register controls various aspects of the digital video input port.

7	6	5	4	3	2	1	0
Reserved	BCF	Reserved	SVREF[1:0]		VSFMT[2:0]		

RESERVED Reserved for future use (set to 0).

BCF Allows the chroma BPF to be bypassed.

0—Do not bypass chroma BPF. Required for analog input. (DEFAULT)
1—Bypass chroma BPF. Required for digital video input.

RESERVED Reserved for future use.

SVREF[1:0] Sync video reference

00—HS/VS aligned with Cb (DEFAULT)
01—HS/VS aligned with Y0
10—HS/VS aligned with Cr
11—HS/VS aligned with Y1

VSFMT[2:0] Video signal format. Controls digital data mux. Switches between A-D blocks for analog input and digital video input port. Configures digital input timing and control block modes.

000—Analog (DEFAULT)
001—CCIR 656
010—ByteStream
011—Reserved
100—External HSYNC,VSYNC
101—External HSYNC,FIELD
110—Reserved
111—Reserved

0x24—TG_CTL (DEFAULT 0x00)

This register controls access to the timing generator RAM, and all timing generator clocks. In each case, ensure a clock is present prior to selection.

Sequence for programming the TGRAM is:

0x41	DIGCLK IN
0x51	Reset Pointer
0x41	Normal mode
Load TGRAM starting at 0x40	Contact Conexant Sales for TGRAM files
0x51	Reset Pointer
0x41	Normal mode
0x63	Use TGRAM mode (DIGCLK Inverted)

7	6	5	4	3	2	1	0
Reserved	CKDIR	TGEN	TGARST	TGCKO[1:0]		TGCKI[1:0]	

RESERVED Reserved for future use. (Set to 0)

CKDIR Digital video clock direction.

0—DIGCLK is output (DEFAULT) - Always active at power up—NOT three-stated at power up.
1—DIGCLK is input

TGEN Timing generator video mode enable.

0—Read/Write mode (DEFAULT)
1—Timing generator mode

TGARST Timing generator address reset.

0—Normal mode (DEFAULT)
1—Reset TG ram address

TGCKO[1:0] Digital video clock output select.

00—CLKx1 (DEFAULT)
01—XTAL
10—PLL
11—PLL inverted

TGCKI[1:0] Decoder input clock select.

00—XTAL (DEFAULT)
01—PLL
10—DIG_CLK
11—DIG_CLK inverted

0x26, 0x25—PLL_F 28 MHz (DEFAULT 0x0000)

Fractional PLL bits. This register is selected automatically for 28.63636 MHz operation or digital video input mode. Defaults to 0x0000.

0x27—PLL_XCI 28 MHz (DEFAULT 0x0C)

Integer PLL bits. This register is selected automatically for 28.63636 MHz operation or digital video input mode. Defaults to 0x0C.

7	6	5	4	3	2	1	0
PLL_X	PLL_C	PLL_I[5:0]					

PLL_X PLL Reference XTAL pre-divider.

0—Divide XTAL by 1 (DEFAULT)
1—Divide XTAL by 2

PLL_C PLL VCO post-divider.

0—Use 6 for post-divider (DEFAULT)
1—Use 4 for post-divider

PLL_I[5:0] PLL_I input. Range 6–63. 00 sleeps PLL. Do not sleep PLL while active. Recovery requires power cycling.

0x29, 0x28—PLL_F 35 MHz (DEFAULT 0xDCF9)

Fractional PLL bits. This register is selected automatically for 35.468950 MHz operation or digital video input mode. Defaults to 0xDCF9.

0x2A—PLL_XCI 35 MHz (DEFAULT 0x0E)

Integer PLL bits. This register is selected automatically for 35.468950 MHz operation or digital video input mode. Defaults to 0x0E.

7	6	5	4	3	2	1	0
PLL_X	PLL_C	PLL_I[5:0]					

PLL_X PLL Reference XTAL pre-divider.

0—Divide XTAL by 1 (DEFAULT)
1—Divide XTAL by 2

PLL_C PLL VCO post-divider.

0—Use 6 for post-divider (DEFAULT)
1—Use 4 for post-divider

PLL_I[5:0] PLL_I input. Range 6–63. 00 sleeps PLL. Do not sleep PLL while active. Recovery requires power cycling.

0x2C, 0x2B—DVLCNT (DEFAULT 0x0000)

Digital video line count. This register allows the user to program the number of lines in a digital video source. If a zero is programmed, the decoder defaults to the standard number of lines for the selected format. Values of 0 to 1023, inclusive, may be programmed into the DVLCNT register.

0x2D—TEST REG. (DEFAULT 0x00)

MFR use.

0x2E—TEST REG. (DEFAULT 0x00)

MFR use.

0x40—7F TGRAM LOCATIONS

Contact Conexant Sales for files.

0xFA—TEST REG. (DEFAULT 0x00)

MFR use.

0xFB—COMB2H_CTL (DEFAULT 0x00)

7	6	5	4	3	2	1	0
DISIF	INVCBF	DISADAPT	NARROWADAPT	FORCE2H	FORCEREMOD	NCHROMAEN	NRMDEN

DISIF Disable Interpolation.

0—Enable IFX (DEFAULT)
1—Disable IFX

INVCBF Invert sense of CBFLAG.

0—Normal (DEFAULT)
1—Invert CBFLAG

DISADAPT Disable adaption algorithm.

0—Enable Adaption (DEFAULT)
1—Disable Adaption

NARROWADAPT Narrow adaption algorithm.

0—Normal (DEFAULT)
1—Narrow

FORCE2H Forces selection of 2H comb filtered chroma data, if 2H comb enabled with NCHROMAEN.

0—Adaptive 2H comb (DEFAULT)
1—2H comb forced on, no adaption

FORCEREMOD Forces remodulation of excess chroma.

0—Adaptive remodulation (DEFAULT)
1—Forced remodulation

NCHROMAEN Chroma 2H comb enable.

0—2H chroma comb enabled (DEFAULT)
1—2H chroma comb disabled

NRMDEN Remodulation enable.

0—Luma remodulation enable (DEFAULT)
1—Luma remodulation disabled

0xFC—TEST 1 REG. (DEFAULT 0x00)

MFR use only.

0xFD—TEST 2 REG. (DEFAULT 0x00)

MFR use only.

0xFE—IDCODE

Reflects device ID and part revision. Read only.

7	6	5	4	3	2	1	0
ID[3:0]				REV[3:0]			

ID[3:0] Device ID

0xA 0101–Bt835

REV[3:0] Device revision

		Marked
0x1	0000—Rev A	–11
0x2	0001—Rev B	–12
0x3	0011—Rev D	–13
0x4	0100—Rev E	–14

0xFF—SW_RESET

A write of any data to this address will reset all internal registers to the default state.

4.1 Register Summary

Table 4-1. Register Map *(1 of 2)*

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0x00	STATUS	R/W	VPRES	HLOCK	FIELD	NUML	PLL	CCVLD_CC	CC/EDS	COF
0X01	INPUT	W	—	MUXS[1:0]		—	FMT[3:0]			
0X0E	VSCALE_CTL	W	—	COMB[1:0]		NVINT	FIELD	VFILT[2:0]		
0X0F	TDEC	W	DECFLD	FLDALN	DRATE[5:0]					
0X15	CONTROL_0	W	LNOTCH	SVID	LDEC	HFILT[1:0]		PEAKEN	PSEL[1:0]	
0X16	CONTROL_1	W	VBIEN	FRAME	VBITFMT	CAGC	CKILL	SC_SPD	HACT	—
0X17	CONTROL_2	W	YCORE[1:0]		CCORE[1:0]		VIPEN	BSTRM	RANGE	VERTEN
0X18	CONTROL_3	W	NOUTEN	OES[1:0]		LEN	HSFMT	ACTFMT	VLDFMT	CLKGT
0X19	VPOLE	W	—	VALID	VACTIVE	CBFALG	FIELD	ACTIVE	HRESET	VRESET
0X1A	AGC_DELAY	W	AGC[7:0]							
0X1B	BG_DELAY	W	BG[7:0]							
0X1C	ADC	W	—	—	—	AGC_EN	CLKSLP	YSLP	CSLP	AGC_EN
0X1D	WC_UP	W	MAJS[1:0]		UPCNT[5:0]					
0X1E	WC_DN	W	—	WCFRM	DNCNT[5:0]					
0X1F	CC_STATUS	R/W	PARERR	INT_EN	EDS	CC	OR	DA	CC/EDS	LO/HI

Table 4-1. Register Map *(2 of 2)*

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0X20	CC_DATA	R	CCDATA[7:0]							
0X21	GPIO	R/W	GPIO [7:0]							
0X22	GPIO_NOE	W	NOE[7:0]							
0X23	VSIF	W	—	BCF	—	SVREF[1:0]		VSFMT[2:0]		
0X24	TG_CTL	W	—	CKDIR	TGEN	TGARST	TGCKO[1:0]		TGCKI[1:0]	
0X27	PLL_XCI 28 HMZ	W	PLL_X	PLL_C	PLL_I[5:0]					
0X2A	PLL_XCI 35 HMZ	W	PLL_X	PLL_C	PLL_I[5:0]					
0XFB	COMB2H_CTL	W	DISIF	INVCBF	DISADAPT	NARROWADAPT	FORCE2H	FORCEREMOD	NCHROMAEN	NRMDEN
0XFE	IDCODE	R	ID[3:0]			REV[3:0]				

5.0 Parametric Information

5.1 DC Electrical Parameters

Table 5-1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply — Analog	V_{AA}	4.75	5.00	5.25	V
Power Supply — 5.0 V Digital	V_{DD}	4.75	5.00	5.25	V
Power Supply — 3.3 V Digital	V_{DDO}	3.00	3.3	3.6	V
Maximum Δ $\lvert V_{DD} - V_{AA} \rvert$ (V_{DD} = 5 V)	—	—	—	0.5	V
MUX0, MUX1, MUX2, and MUX3 Input Range (AC coupling required)	—	0.5	1.00	2.00	V
VIN Amplitude Range (AC coupling required)	—	0.5	1.00	2.00	V
Ambient Operating Temperature	T_A	0		+70	°C

Table 5-2. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
V_{AA} (measured to AGND)	—	—	—	7.00	V
V_{DD} (measured to DGND)	—	—	—	7.00	V
Voltage on any signal pin (See the note below)	—	DGND – 0.5	—	V_{DD} + 0.5	V
Analog Input Voltage	—	AGND – 0.5	—	V_{AA} + 0.5	V
Storage Temperature	T_S	–65	—	+150	°C
Junction Temperature	T_J	—	—	+125	°C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}	—	V	+220	°C

NOTE(S): Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V, or drops below ground by more than 0.5 V, can induce destructive latchup.

Table 5-3. DC Characteristics (3.3 V digital I/O operation)

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs	—	—	—	—	—
Input High Voltage (TTL)	V_{IH}	2.0	—	V_{DDO} + 0.5	V
Input Low Voltage (TTL)	V_{IL}	—	—	0.8	V
Input High Voltage (XTI)	V_{IH}	2.3	—	V_{DDO} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	GND – 0.5	—	1.0	V
Input High Current (V_{IN}=V_{DD})	I_{IH}	—	—	10	µA
Input Low Current (V_{IN}=GND)	I_{IL}	—	—	–10	µA
Input Capacitance (f=1 MHz, V_{IN}=2.4 V)	C_{IN}	—	—	—	pF
Input High Voltage (NUMXTAL, ALTADDR)	V_{IH}	2.5	—	—	V
Digital Outputs	—	—	—	—	—
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4	—	V_{DDO}	V
Output Low Voltage (I_{OL}= 3.2 mA)	V_{OL}	—	—	0.4	V
Three-State Current	I_{OZ}	—	—	10	µA
Output Capacitance	C_O	—	5	—	pF
Analog Pin Input Capacitance	C_A	—	5	—	pF

Table 5-4. DC Characteristics (5 V only operation)

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs	—	—	—	—	—
Input High Voltage (TTL)	V_{IH}	2.0	—	V_{DD} + 0.5	V
Input Low Voltage (TTL)	V_{IL}	—	—	0.8	V
Input High Voltage (XTI)	V_{IH}	3.5	—	V_{DD} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	GND – 0.5	—	1.5	V
Input High Current (V_{IN}=V_{DD})	I_{IH}	—	—	10	µA
Input Low Current (V_{IN}=GND)	I_{IL}	—	—	–10	µA
Input Capacitance (f=1 MHz, V_{IN}=2.4 V)	C_{IN}	—	5	—	pF
Digital Outputs	—	—	—	—	—
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4	—	V_{DD}	V
Output Low Voltage (I_{OL}= 3.2 mA)	V_{OL}	—	—	0.4	V
Three-State Current	I_{OZ}	—	—	10	µA
Output Capacitance	C_O	—	5	—	pF
Analog Pin Input Capacitance	C_A	—	5	—	pF

5.2 AC Electric Parameters

Table 5-5. Clock Timing Parameters *(1 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
NTSC:					
CLKx1 Rate	F_{S1}	—	14.318180	—	MHz
CLKx2 Rate (50 PPM source required)	F_{S2}	—	28.636360	—	MHz
PAL/SECAM:					
CLKx1 Rate	F_{S1}	—	17.734475	—	MHz
CLKx2 Rate (50 PPM source required)	F_{S2}	—	35.468950	—	MHz
XT0 and XT1 Inputs					
Cycle Time	1	28.2	—	—	ns
High Time	2	12	—	—	ns
Low Time	3	12	—	—	ns

Table 5-5. Clock Timing Parameters *(2 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
CLKx1 Duty Cycle	—	45	—	55	%
CLKx2 Duty Cycle	—	40	—	60	%
CLKx2 to CLKx1 Delay	4	0	—	2	ns
CLKx1 to Data Delay	5	3	—	11 (25)[2]	ns
CLKx2 to Data Delay	6	3	—	11 (25)[2]	ns
CLKx1 (Falling Edge) to QCLK (Rising Edge)	41	0	—	8	ns
CLKx2 (Falling Edge) to QCLK (Rising Edge)	42	0	—	8	ns
8-Bit Mode[1]					
Data to QCLK (Rising Edge) Delay (Setup)	7b	5	—	—	ns
QCLK (Rising Edge) to Data Delay (Hold)	8b	15	—	—	ns
16-Bit Mode[1]					
Data to QCLK (Rising Edge) Delay (Setup)	7a	14	—	—	ns
QCLK (Rising Edge) to Data Delay (Hold)	8a	25	—	—	ns

NOTE(S):

(1) Because QCLK is generated with a gated version of CLKx1 or CLKx2, the timing in symbols 7 and 8 are subject to changes in the duty cycle of CLKx1 and CLKx2. If crystals are used as clock sources for the Bt829A, the duty cycle is symmetric. This assumption is used to generate the timing numbers shown in 7 and 8. For non-symmetric clock sources, use the following equations:

Data to QCLK (setup) 16-bit mode	xtal period + CLKx1 to qclk (max) - CLKx1 to data (max) or symbol 1 + symbol 41 (max) - symbol 5 (max) NTSC: 34.9 ns+ 8 ns- 11 ns= 31.9 ns PAL: 28.2 ns+ 8 ns-11 ns= 25.2 ns
QCLK to Data (hold) 16-bit mode	xtal period - CLKx1 to qclk (min) + CLKx1 to data (min) or symbol 1 - symbol 41 (min) + symbol 5 (min) NTSC: 34.9 ns- 0 ns+ 3 ns= 37.9 ns PAL: 28.3 ns- 0 ns+ 3 ns= 31.3 ns
Data to QCLK (setup) 8-bit mode	(xtal period)/2 + CLKx2 to qclk (max) - CLKx2 to data (max) or (symbol 1)/2 + symbol 42 (max) - symbol 6 (max) NTSC: 17.5 ns+ 8ns- 11 ns= 14.5 ns PAL: 14.1 ns+ 8 ns- 11 ns= 11.1 ns
QCLK to data (hold) 8-bit mode	(xtal period)/2 - CLKx2 to qclk (min) + CLKx2 to data (min) or (symbol 1)/2 - symbol 42 (min) + symbol 6 (min) NTSC: 17.5 ns- 0 ns+ 3 ns= 20.5 ns PAL: 14.1 ns- 0 ns+ 3 ns= 17.1 ns

(2) Parenthesis indicate max CLKx1/CLKx2 to Data Delay when using VDDO = 3.3 V.

Figure 5-1. Clock Timing Diagram

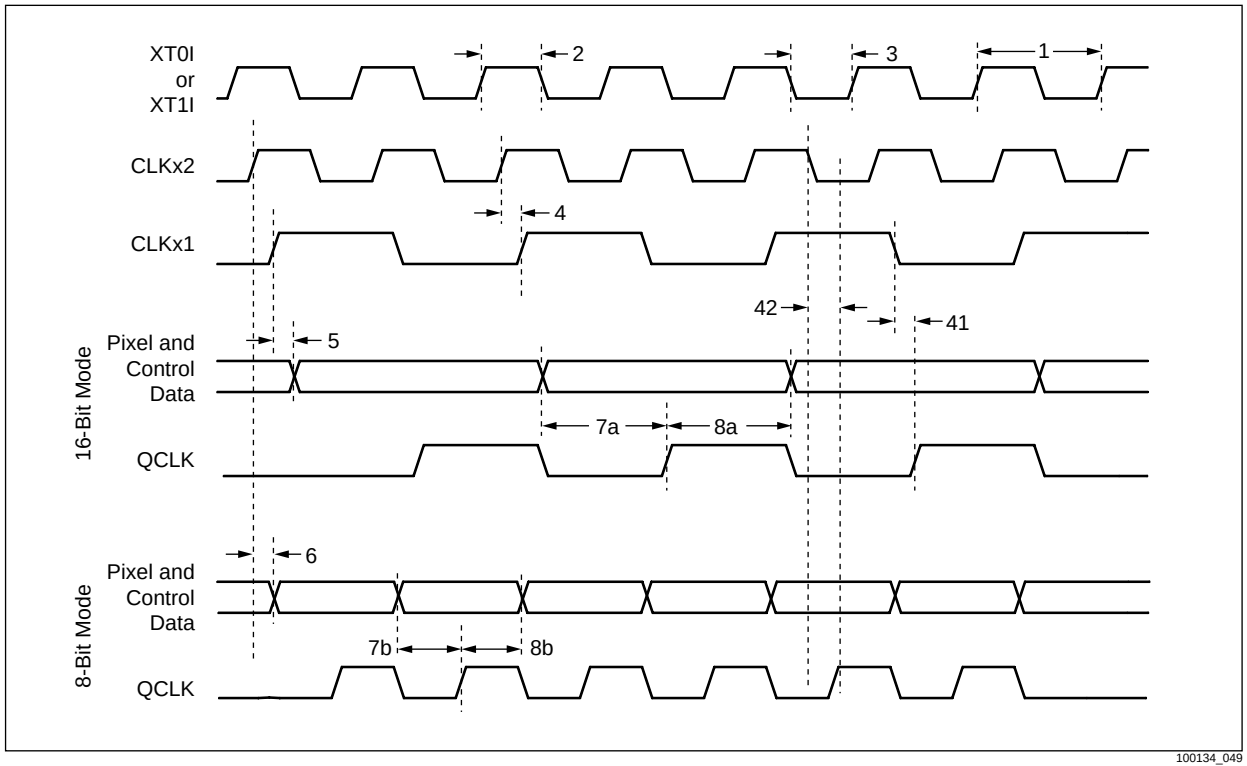


Table 5-6. Power Supply Current Parameters (VDD, VDDO, and VPP 3 V and 5 V Operation)

Parameter	Symbol	Min	Typ	Max	Units
Supply Current (Total for chip including IAA)	I	—	—	—	—
VDD, VDDO, VPP = 3 V or 5 V	—	—	—	—	—
V_{AA}=5.0 V, F_{CLKx2}=28.64 MHz, T=25°C			145/170	—	mA
V_{AA}=5.25 V, F_{CLKx2}=35.47 MHz, T=70°C			—	200/250	mA
V_{AA}=5.25 V, F_{CLKx2}=35.47 MHz, T=0°C			—	240/280	mA
Supply Current, Power Down			65	—	mA

Table 5-7. Output Enable Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
$\overline{OE}$ Asserted to Data Bus Driven	9	0	—	—	ns
$\overline{OE}$ Asserted to Data Valid	10	—	—	100	ns
$\overline{OE}$ Negated to Data Bus Not Driven	11	—	—	100	ns
$\overline{RST}$ Low Time	—	8	—	—	XTAL cycles

Figure 5-2. Output Enable Timing Diagram

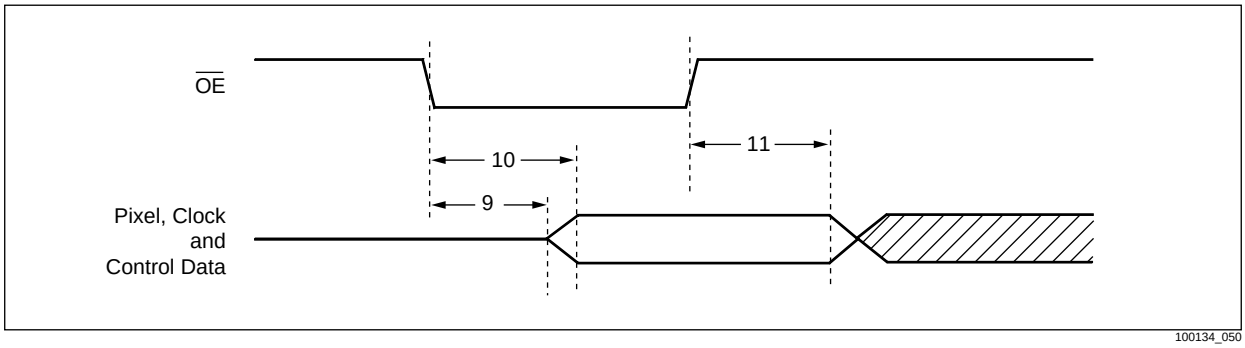


Table 5-8. JTAG Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
TMS, TDI Setup Time	12	—	10	—	ns
TMS, TDI Hold Time	13	—	10	—	ns
TCK Asserted to TDO Valid	14	—	60	—	ns
TCK Asserted to TDO Driven	15	—	5	—	ns
TCK Negated to TDO Three-stated	16	—	80	—	ns
TCK Low Time	17	25	—	—	ns
TCK High TIme	18	25	—	—	ns

Figure 5-3. JTAG Timing Diagram

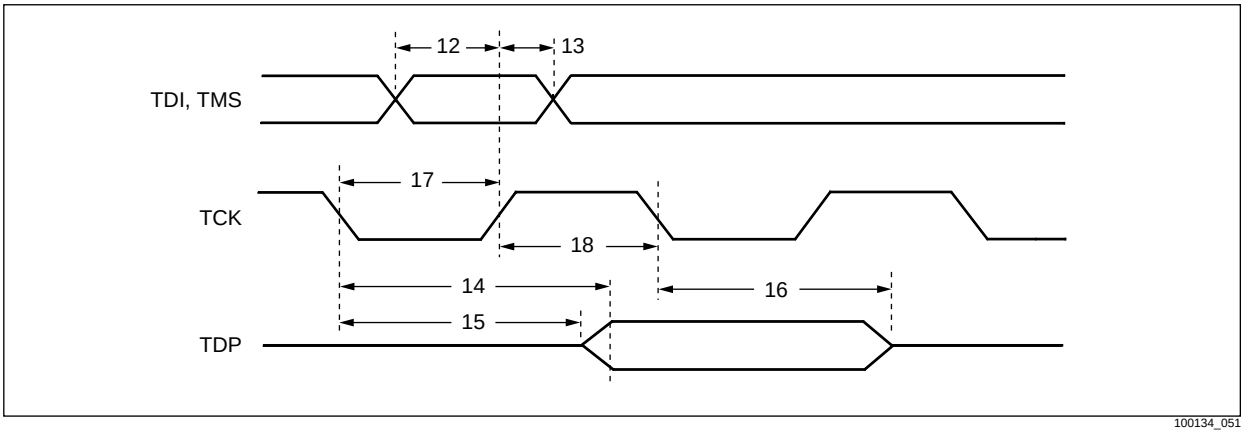
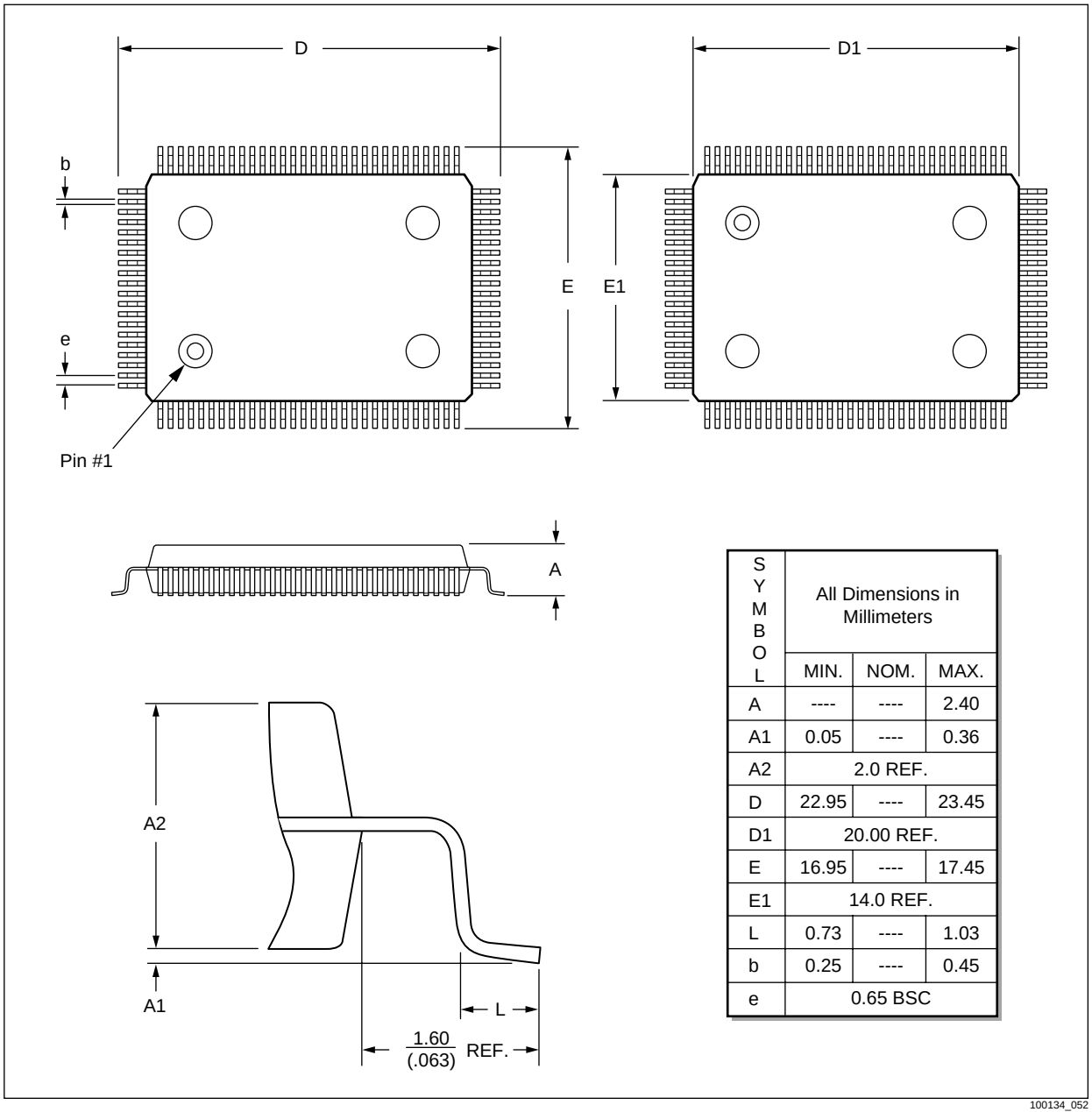


Table 5-9. Decoder Performance Parameters

Parameter	Symbol	Min	Typ	Max	Units
Horizontal Lock Range	—	—	—	±7	% of Line Length
Fsc, Lock-in Range	—	±800	—	—	Hz
Gain Range	—	–6	—	6	dB

NOTE(S): Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. Pixel and control data loads ≤ 30 pF and ≥10 pF. CLKx1 and CLKx2 loads ≤ 50 pF. Control data includes CBFLAG, DVALID, ACTIVE, VACTIVE, $\overline{\text{HRESET}}$, $\overline{\text{VRESET}}$ and FIELD.

Figure 5-4. 100-Pin PQFP Package Mechanical Drawing



SYMBOL	All Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	----	----	2.40
A1	0.05	----	0.36
A2	2.0 REF.		
D	22.95	----	23.45
D1	20.00 REF.		
E	16.95	----	17.45
E1	14.0 REF.		
L	0.73	----	1.03
b	0.25	----	0.45
e	0.65 BSC		

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