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Actual Size
(3,10 mm x 4,50 mm)

TPS2112
TPS2113

SLVS446 – DECEMBER 2002

AUTOSWITCHING POWER MUX

FEATURES

- **Two-Input, One-Output Power Multiplexer With Low $r_{DS(on)}$ Switches:**
  - **84 mΩ Typ (TPS2113)**
  - **120 mΩ Typ (TPS2112)**
- **Reverse and Cross-Conduction Blocking**
- **Wide Operating Voltage Range . . . .2.8 V to 5.5 V**
- **Low Standby Current . . . . 0.5-μA Typ**
- **Low Operating Current . . . . 55-μA Typ**
- **Adjustable Current Limit**
- **Controlled Output Voltage Transition Times, Limits Inrush Current and Minimizes Output Voltage Hold-Up Capacitance**
- **CMOS and TTL Compatible Control Inputs**
- **Auto-Switching Operating Mode**
- **Thermal Shutdown**
- **Available in a TSSOP-8 Package**

APPLICATIONS

- **PCs**
- **PDAs**
- **Digital Cameras**
- **Modems**
- **Cell phones**
- **Digital Radios**
- **MP3 Players**

PW PACKAGE
(TOP VIEW)

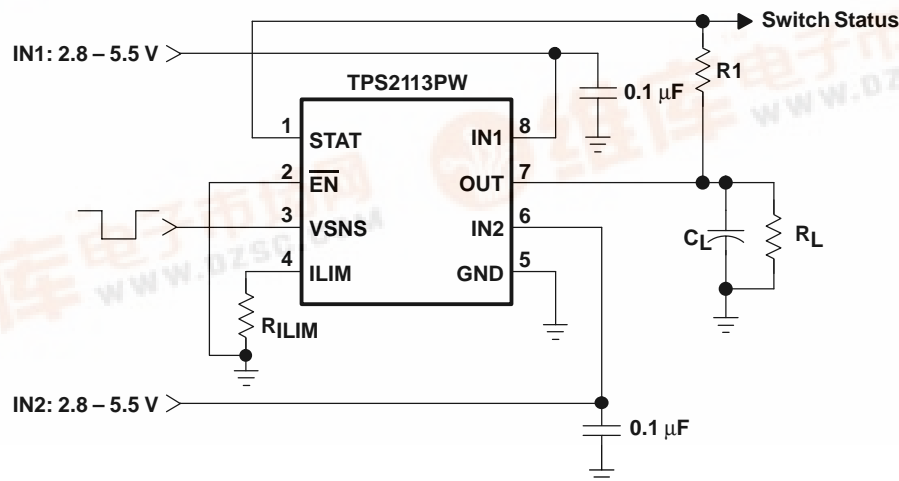|		
STAT	1	8 IN1
EN	2	7 OUT
VSNS	3	6 IN2
ILIM	4	5 GND
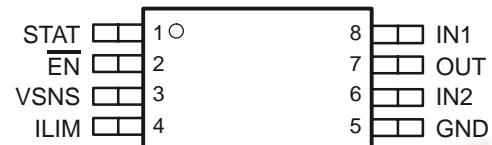
DESCRIPTION

The TPS211x family of power multiplexers enables seamless transition between two power supplies, such as a battery and a wall adapter, each operating at 2.8–5.5 V and delivering up to 1 A. The TPS211x family includes extensive protection circuitry, including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

TYPICAL APPLICATION

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty.

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TPS2112
TPS2113

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

FEATURE		TPS2110	TPS2111	TPS2112	TPS2113	TPS2114	TPS2115
Current Limit Adjustment Range		0.31–0.75A	0.63–1.25A	0.31–0.75A	0.63–1.25A	0.31–0.75A	0.63–1.25A
Switching modes	Manual	Yes	Yes	No	No	Yes	Yes
	Automatic	Yes	Yes	Yes	Yes	Yes	Yes
Switch Status Output		No	No	Yes	Yes	Yes	Yes
Package		TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8

ORDERING INFORMATION

T_A	PACKAGE	ORDERING NUMBER[1]	MARKINGS
−40°C to 85°C	TSSOP-8 (PW)	TPS2112PW	2112
		TPS2113PW	2113

[1] The PW package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2112PWR) to indicate tape and reel.

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T_A = 25°C	$T_A \leq 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
TSSOP-8 (PW)	3.87 mW/°C	386.84 mW	212.76 mW	154.73 mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

		TPS2112, TPS2113
Input voltage range at pins IN1, IN2, $\overline{EN}$, VSNS, ILIM[2]		−0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$, $V_{O(STAT)}$[2]		−0.3 V to 6 V
Output sink current, $I_{O(STAT)}$		5 mA
Continuous output current, I_O	TPS2112	0.9 A
	TPS2113	1.5 A
Continuous total power dissipation		See Dissipation Rating Table
Operating virtual junction temperature range, T_J		−40°C to 125°C
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		260°C

[1] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltages are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Input voltage at IN1, $V_{I(IN1)}$	$V_{I(IN2)} \geq 2.8$ V	1.5	5.5	V
	$V_{I(IN2)} < 2.8$ V	2.8	5.5	
Input voltage at IN2, $V_{I(IN2)}$	$V_{I(IN1)} \geq 2.8$ V	1.5	5.5	V
	$V_{I(IN1)} < 2.8$ V	2.8	5.5	
Input voltage, $V_{I(\overline{EN})}$, $V_{I(VSNS)}$		0	5.5	V
Current limit adjustment range, $I_{O(OUT)}$	TPS2112	0.31	0.75	A
	TPS2113	0.63	1.25	
Operating virtual junction temperature, T_J		−40	125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model		2	kV
CDM		500	V

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5$ V, $R_{ILIM} = 400$ Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TPS2112			TPS2113			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
POWER SWITCH										
$r_{DS(on)}$[1]	Drain-source on-state resistance (INx–OUT)	$T_J = 25°C$, $I_L = 500$ mA	$V_{I(IN1)} = V_{I(IN2)} = 5.0$ V		120	140		84	110	mΩ
			$V_{I(IN1)} = V_{I(IN2)} = 3.3$ V		120	140		84	110	
			$V_{I(IN1)} = V_{I(IN2)} = 2.8$ V		120	140		84	110	
		$T_J = 125°C$, $I_L = 500$ mA	$V_{I(IN1)} = V_{I(IN2)} = 5.0$ V			220			150	mΩ
			$V_{I(IN1)} = V_{I(IN2)} = 3.3$ V			220			150	
			$V_{I(IN1)} = V_{I(IN2)} = 2.8$ V			220			150	

[1] The TPS211x can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this specific case, the lower supply voltage has no effect on the IN1 and IN2 switch on-resistances.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUTS ($\overline{EN}$)					
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
Input current	$\overline{EN}$ = High, sink current			1	μA
	$\overline{EN}$ = Low, source current	0.5	1.4	5	
SUPPLY AND LEAKAGE CURRENTS					
Supply current from IN1 (operating)	$V_{I(VSNS)} = 1.5$ V, $\overline{EN}$ = Low (IN1 active), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A		55	90	μA
	$V_{I(VSNS)} = 1.5$ V, $\overline{EN}$ = Low (IN1 active), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A		1	12	
	$V_{I(VSNS)} = 0$ V, $\overline{EN}$ = Low (IN2 active), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A			75	
	$V_{I(VSNS)} = 0$ V, $\overline{EN}$ = Low (IN2 active), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A			1	
Supply current from IN2 (operating)	$V_{I(VSNS)} = 1.5$ V, $\overline{EN}$ = Low (IN1 active), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A			1	μA
	$V_{I(VSNS)} = 1.5$ V, $\overline{EN}$ =Low (IN1 active), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A			75	
	$V_{I(VSNS)} = 0$ V, $\overline{EN}$ = Low (IN2 active), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A		1	12	
	$V_{I(VSNS)} = 0$ V, $\overline{EN}$ = Low (IN2 active), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A		55	90	
Quiescent current from IN1 (STANDBY)	$\overline{EN}$ = High (inactive), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A		0.5	2	μA
	$\overline{EN}$ = High (inactive), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A			1	
Quiescent current from IN2 (STANDBY)	$\overline{EN}$ = High (inactive), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A			1	μA
	$\overline{EN}$ = High (inactive), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A		0.5	2	
Forward leakage current from IN1 (measured from OUT to GND)	$\overline{EN}$ = High (inactive), $V_{I(IN1)} = 5.5$ V, IN2 open, $V_{O(OUT)} = 0$ V (shorted), $T_J = 25°C$		0.1	5	μA
Forward leakage current from IN2 (measured from OUT to GND)	$\overline{EN}$ = High (inactive), $V_{I(IN2)} = 5.5$ V, IN1 open, $V_{O(OUT)} = 0$ V (shorted), $T_J = 25°C$		0.1	5	μA
Reverse leakage current to INx (measured from INx to GND)	$\overline{EN}$ = High (inactive), $V_{I(INx)} = 0$ V, $V_{O(OUT)} = 5.5$ V, $T_J = 25°C$		0.3	5	μA
STAT OUTPUT					
Leakage current	$V_{O(STAT)} = 5.5$ V		0.01	1	μA
Saturation voltage	$I_{I(STAT)} = 2$ mA, IN1 switch is on		0.13	0.4	V
Deglitch time (falling edge only)			150		μs

TPS2112
TPS2113

SLVS446 – DECEMBER 2002

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ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5$ V, $R_{ILIM} = 400$ Ω (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT CIRCUIT							
Current limit accuracy	TPS2112	$R_{ILIM} = 400$ Ω		0.51	0.63	0.80	A
		$R_{ILIM} = 700$ Ω		0.30	0.36	0.50	
	TPS2113	$R_{ILIM} = 400$ Ω		0.95	1.25	1.56	
		$R_{ILIM} = 700$ Ω		0.47	0.71	0.99	
t_d	Current limit settling time[1]		Time for short–circuit output current to settle within 10% of its steady state value.		1		ms
	Input current at ILIM		$V_{I(ILIM)} = 0$ V, $I_{O(OUT)} = 0$ A	−15		0	μA

[1] Not tested in production.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSNS COMPARATOR					
VSNS threshold voltage	$V_{I(VSNS)}$ ↑	0.78	0.8	0.82	V
	$V_{I(VSNS)}$ ↓	0.735	0.755	0.775	
VSNS comparator hysteresis[1]			30	60	mV
Deglitch of VSNS comparator (both ↑↓)[1]		90	150	220	μs
Input current	0 V $\leq V_{I(VSNS)} \leq 5.5$ V	−1		1	μA
UVLO					
IN1 and IN2 UVLO	Falling edge	1.15	1.25		V
	Rising edge		1.30	1.35	
IN1 and IN2 UVLO hysteresis[1]		30	57	65	mV
Internal V_{DD} UVLO (the higher of IN1 and IN2)	Falling edge	2.4	2.53		V
	Rising edge		2.58	2.8	
Internal V_{DD} UVLO hysteresis[1]		30	50	75	mV
UVLO deglitch for IN1, IN2[1]	Falling edge		110		μs

[1] Not tested in production.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REVERSE CONDUCTION BLOCKING						
$\Delta V_{O(I\_block)}$	Minimum output-to-input voltage difference to block switching	$\overline{EN}$ = high, $V_{I(IN1)} = 3.3$ V and $V_{I(IN2)} = V_{I(VSNS)} = 0$ V. Connect OUT to a 5 V supply through a series 1-kΩ resistor. Let $\overline{EN}$ = low. Slowly decrease the supply voltage until OUT connects to IN1.	80	100	120	mV

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Thermal shutdown threshold[1]	TPS211x is in current limit.	135			°C
Recovery from thermal shutdown[1]	TPS211x is in current limit.	125			
Hysteresis[1]			10		
IN2–IN1 COMPARATORS					
Hysteresis of IN2–IN1 comparator			0.1	0.2	V
Deglitch of IN2–IN1 comparator, (both ↑↓)[1]		90	150	220	μs

[1] Not tested in production.

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5$ V, $R_{ILIM} = 400$ Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TPS2112			TPS2113			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
POWER SWITCH										
t_r	Output rise time from an enable[1]	$V_{I(IN1)} = V_{I(IN2)} = 5$ V, $V_{I(VSNS)} = 1.5$ V	$T_J = 25°C$, $C_L = 1$ µF, $I_L = 500$ mA, See Figure 1(a)	0.5	1.0	1.5	1	1.8	3	ms
t_f	Output fall time from a disable[1]	$V_{I(IN1)} = V_{I(IN2)} = 5$ V, $V_{I(VSNS)} = 1.5$ V	$T_J = 25°C$, $C_L = 1$ µF, $I_L = 500$ mA, See Figure 1(a)	0.35	0.5	0.7	0.5	1	2	ms
t_t	Transition time[1]	IN1 to IN2 transition, $V_{I(IN1)} = 3.3$ V, $V_{I(\overline{IN2})} = 5$ V, $V_{I(\overline{EN})} = 0$ V	$T_J = 125°C$, $C_L = 10$ µF, $I_L = 500$ mA [Measure transition time as 10–90% rise time or from 3.4 V to 4.8 V on $V_{O(OUT)}$], See Figure 1(b)		40	60		40	60	µs
t_{PLH1}	Turn-on propagation delay from enable[1]	$V_{I(IN1)} = V_{I(IN2)} = 5$ V Measured from enable to 10% of $V_{O(OUT)}$, $V_{I(VSNS)} = 1.5$ V	$T_J = 25°C$, $C_L = 10$ µF, $I_L = 500$ mA, See Figure 1(a)		0.5			1		ms
t_{PHL1}	Turn-off propagation delay from a disable[1]	$V_{I(IN1)} = V_{I(IN2)} = 5$ V, Measured from disable to 90% of $V_{O(OUT)}$, $V_{I(VSNS)} = 1.5$ V	$T_J = 25°C$, $C_L = 10$ µF, $I_L = 500$ mA, See Figure 1(a)		3			5		ms
t_{PLH2}	Switch-over rising propagation delay[1]	Logic 1 to Logic 0 transition on VSNS , $V_{I(IN1)} = 1.5$ V, $V_{I(\overline{IN2})} = 5$ V, $V_{I(\overline{EN})} = 0$ V, Measured from VSNS to 10% of $V_{O(OUT)}$	$T_J = 25°C$, $C_L = 10$ µF, $I_L = 500$ mA, See Figure 1(c)		0.17	1		0.17	1	ms
t_{PHL2}	Switch-over falling propagation delay[1]	Logic 0 to Logic 1 transition on VSNS $V_{I(IN1)} = 1.5$V, $V_{I(\overline{IN2})} = 5$V, $V_{I(\overline{EN})} = 0$ V, Measured from VSNS to 90% of $V_{O(OUT)}$	$T_J = 25°C$, $C_L = 10$ µF, $I_L = 500$ mA, See Figure 1(c)	2	3	10	2	5	10	ms

[1] Not tested in production.

TPS2112
TPS2113

SLVS446 – DECEMBER 2002

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TRUTH TABLE

$\overline{\text{EN}}$	$V_{I(VSNS)} > 0.8V$	$V_{I(IN2)} > V_{I(IN1)}$	STAT	OUT[1]
0	Yes	X	0	IN1
	No	No	0	IN1
	No	Yes	Hi-Z	IN2
1	X	X	0	Hi-Z

[1]The under-voltage lockout circuit causes the output OUT to go Hi-Z if the selected power supply does not exceed the IN1/IN2 UVLO, or if neither of the supplies exceeds the internal V_{DD} UVLO.

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	2	I	$\overline{\text{EN}}$ is a TTL and CMOS compatible input with a 1-μA pull-up. The truth table shown above illustrates the functionality of $\overline{\text{EN}}$.
GND	5	I	Ground
IN1	8	I	Primary power switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
IN2	6	I	Secondary power switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
ILIM	4	I	A resistor R_{ILIM} from ILIM to GND sets the current limit I_L to 250/R_{ILIM} and 500/R_{ILIM} for the TPS2112 and TPS2113, respectively.
OUT	7	O	Power switch output
STAT	1	O	STAT is an open-drain output that is Hi-Z if the IN2 switch is ON. STAT pulls low if the IN1 switch is ON or if OUT is Hi-Z (i.e., $\overline{\text{EN}}$ is equal to logic 0)
VSNS	3	I	An internal power FET connects OUT to IN1 if the VSNS voltage is greater than 0.8 V. Otherwise, the FET connects OUT to the higher of IN1 and IN2. The truth table shown above illustrates the functionality of VSNS.

FUNCTIONAL BLOCK DIAGRAM

TPS2112
TPS2113

SLVS446 – DECEMBER 2002
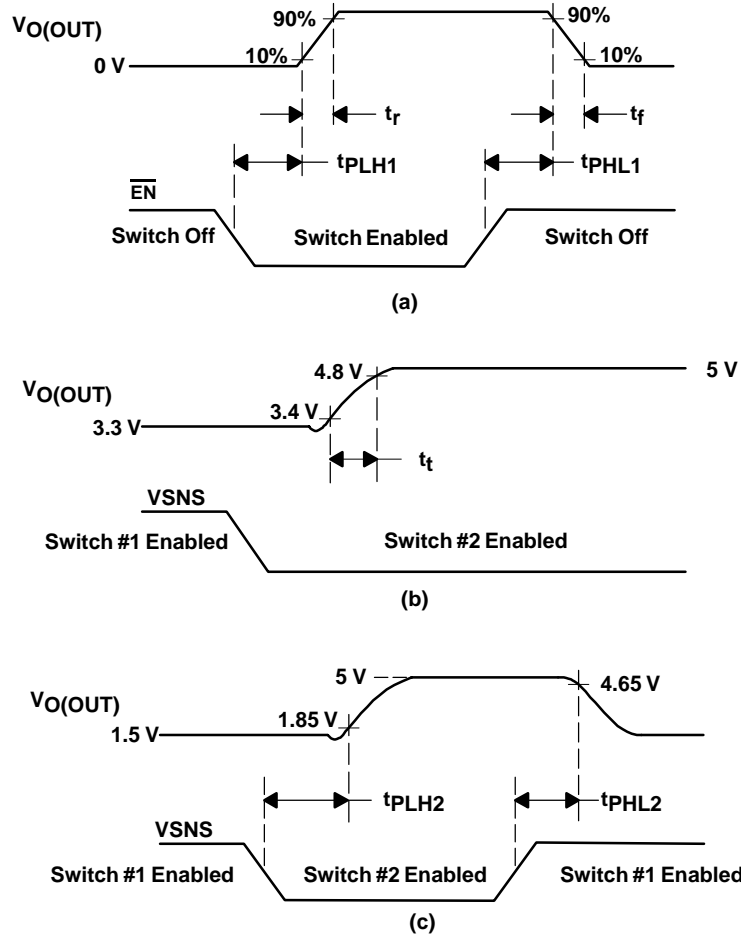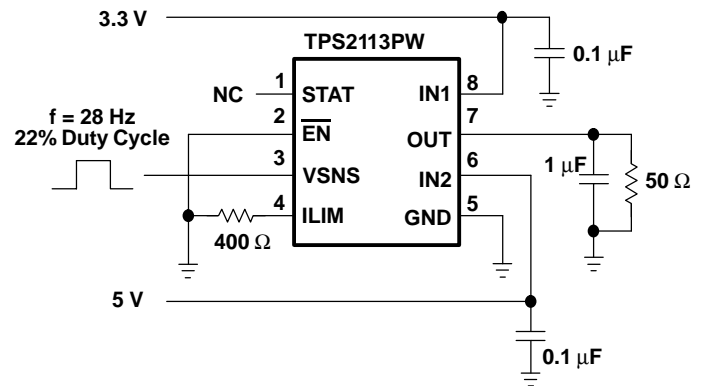
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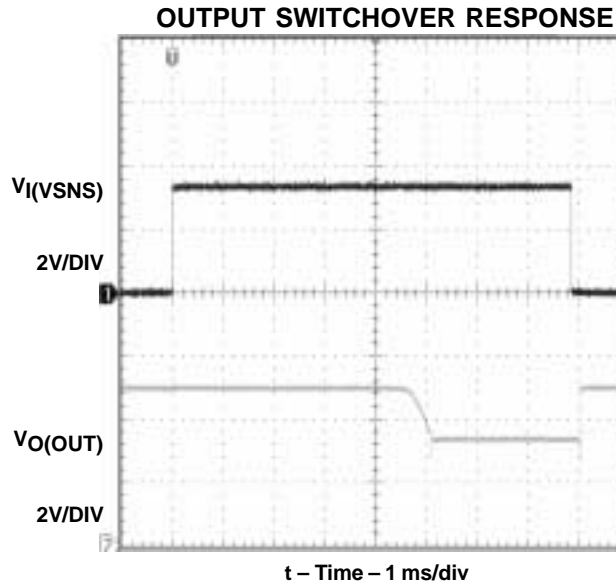www.ti.com
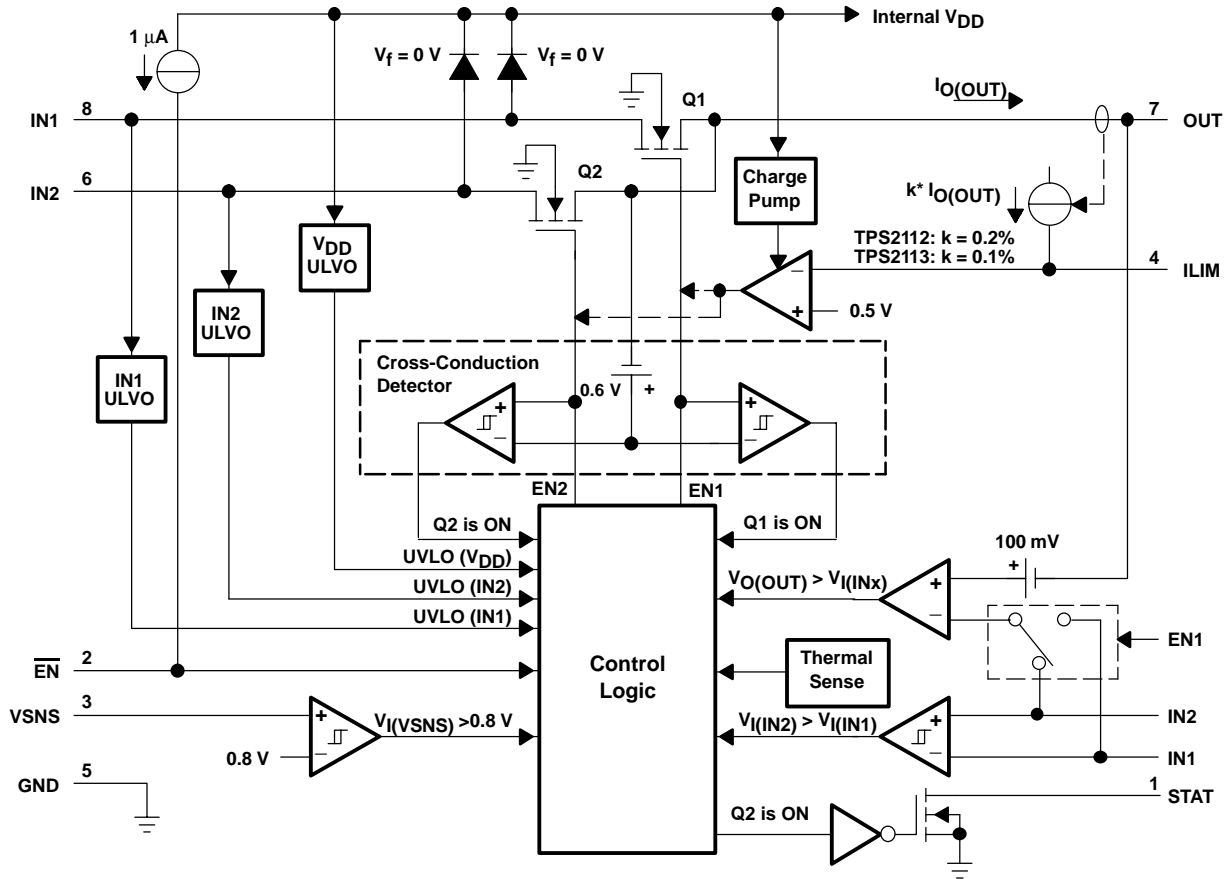
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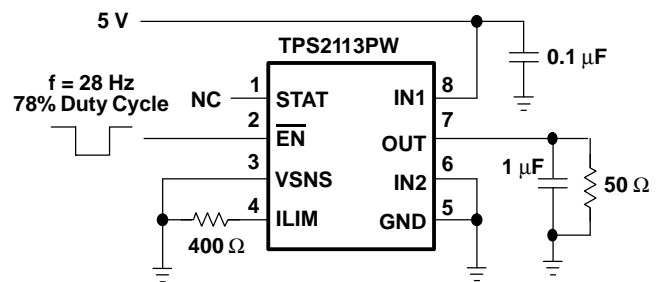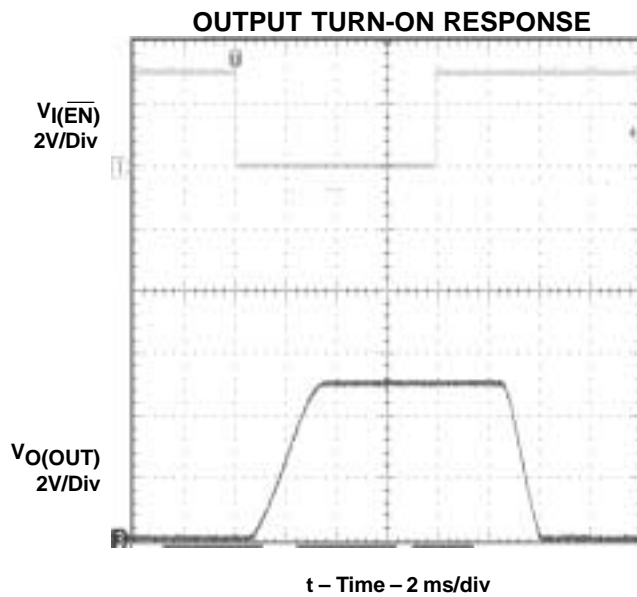

Figure 1. Propagation Delays and Transition Timing Waveforms

TYPICAL CHARACTERISTICS

OUTPUT SWITCHOVER RESPONSE

t – Time – 1 ms/div

Output Switchover Response Test Circuit

Figure 2

OUTPUT TURN-ON RESPONSE

t – Time – 2 ms/div

Output Turn-On Response Test Circuit

Figure 3

TYPICAL CHARACTERISTICS

OUTPUT SWITCHOVER VOLTAGE DROOP

$V_{I(VSNS)}$
2V/Div

$C_L = 1 \mu F$

$V_{O(OUT)}$
2V/Div

$C_L = 0 \mu F$

t – Time – 40 μs/div
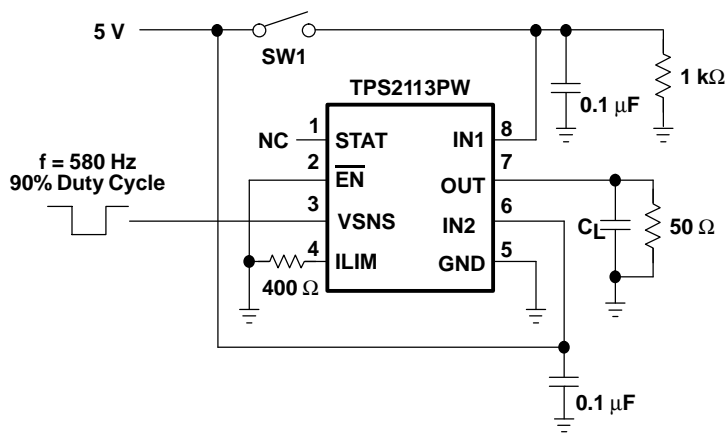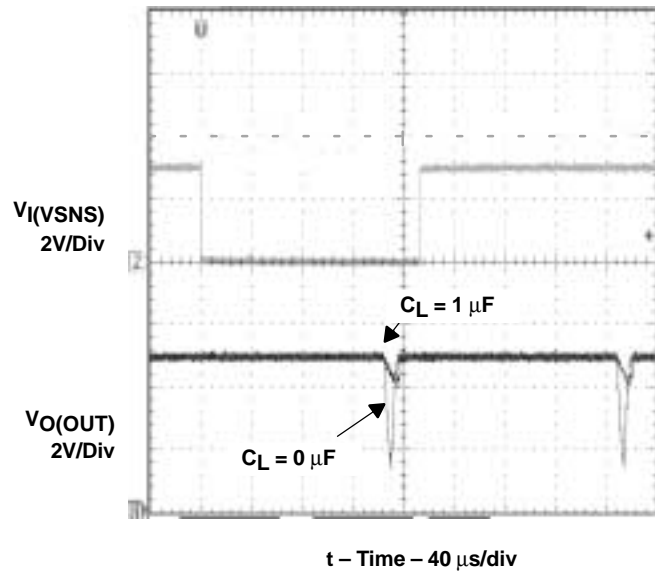
Output Switchover Voltage Droop Test Circuit

Figure 4

NOTE: To initialize the TPS2113 for this test, set input VSNS equal to 0 V, turn on the 5 V supply, and then turn on switch SW1.

TYPICAL CHARACTERISTICS

OUTPUT SWITCHOVER VOLTAGE DROOP
vs
LOAD CAPACITANCE
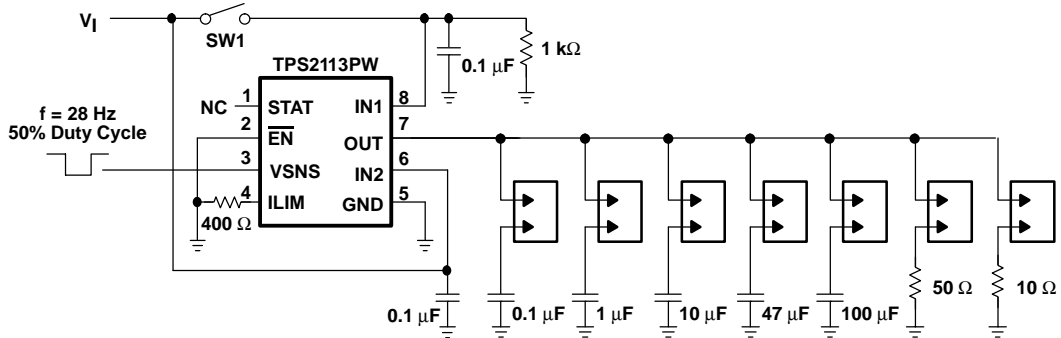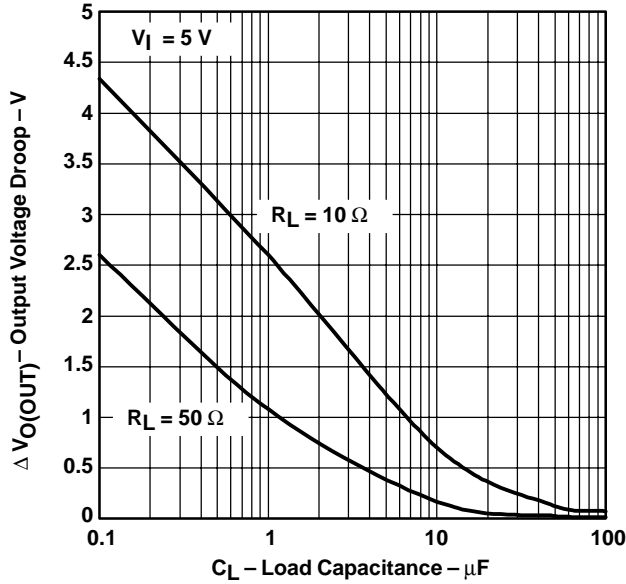
Output Switchover Voltage Droop Test Circuit

Figure 5

NOTE: To initialize the TPS2113 for this test, set input VSNS equal to 0 V, turn on the supply V_i, and then turn on switch SW1.

TPS2112
TPS2113

SLVS446 – DECEMBER 2002

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TYPICAL CHARACTERISTICS

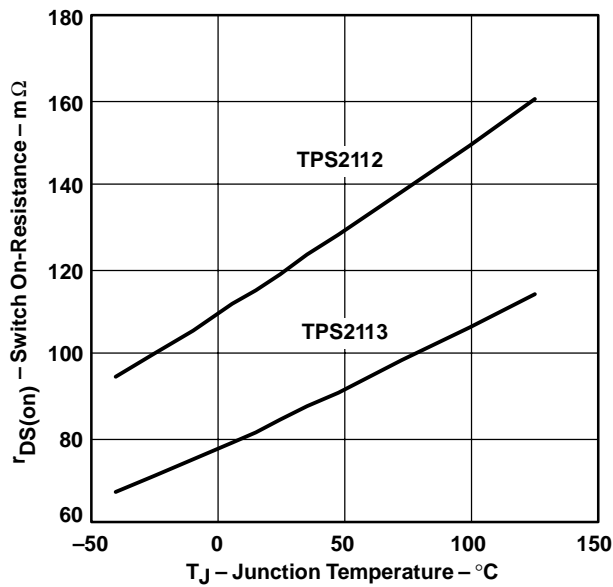### INRUSH CURRENT
vs
LOAD CAPACITANCE
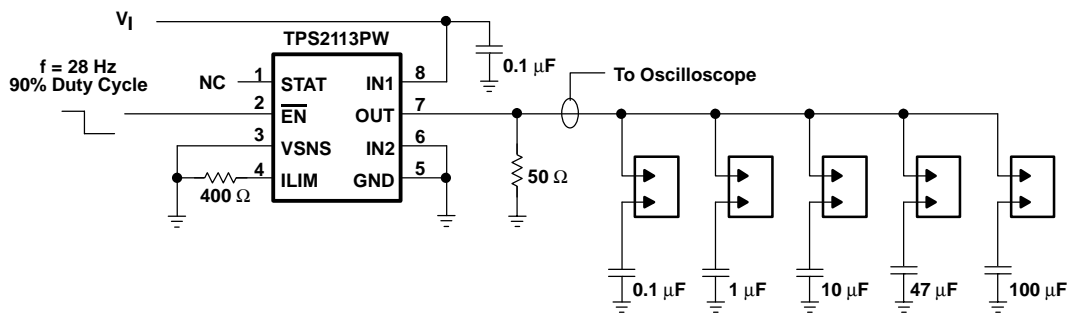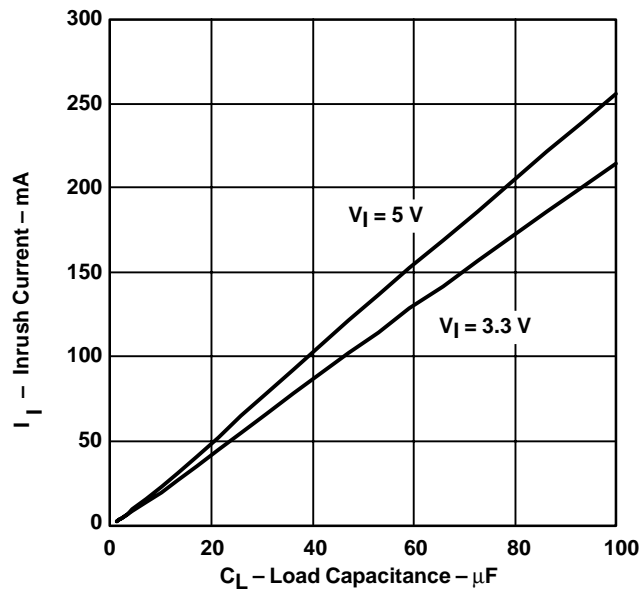
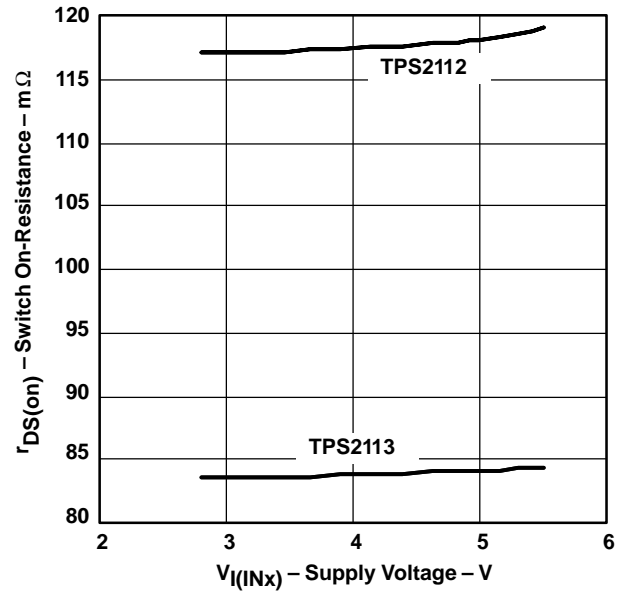Output Capacitor Inrush Current Test Circuit

Figure 6

TYPICAL CHARACTERISTICS

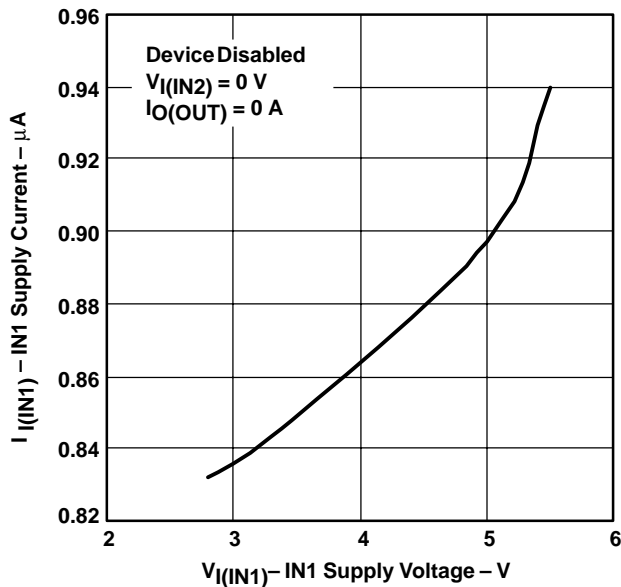**SWITCH ON-RESISTANCE**
vs
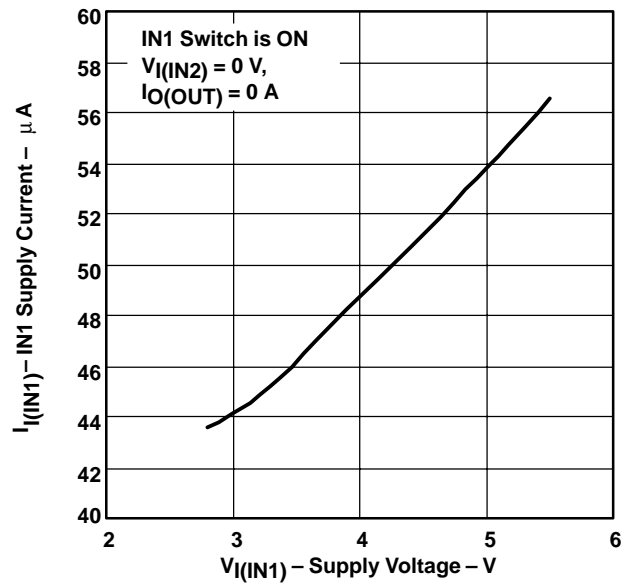**JUNCTION TEMPERATURE**

Figure 7

SWITCH ON-RESISTANCE
vs
SUPPLY VOLTAGE

Figure 8

IN1 SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 9

IN1 SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 10

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TPS2113

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
JUNCTION TEMPERATURE

Figure 11
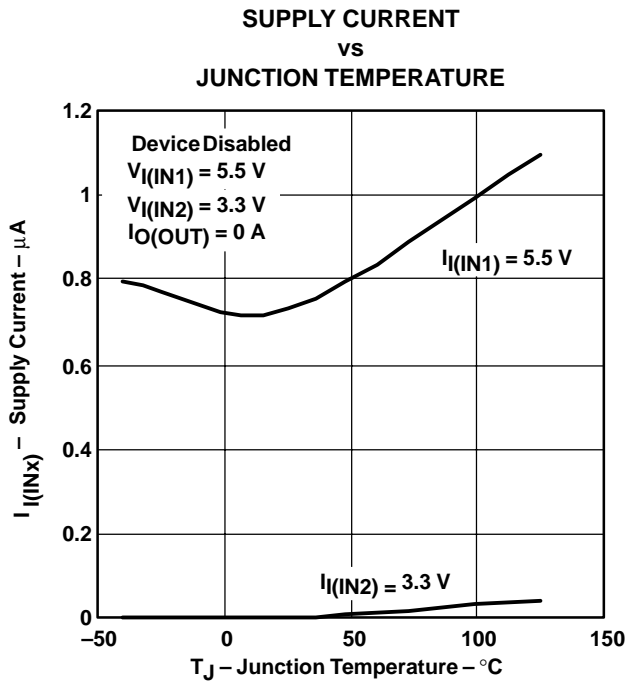
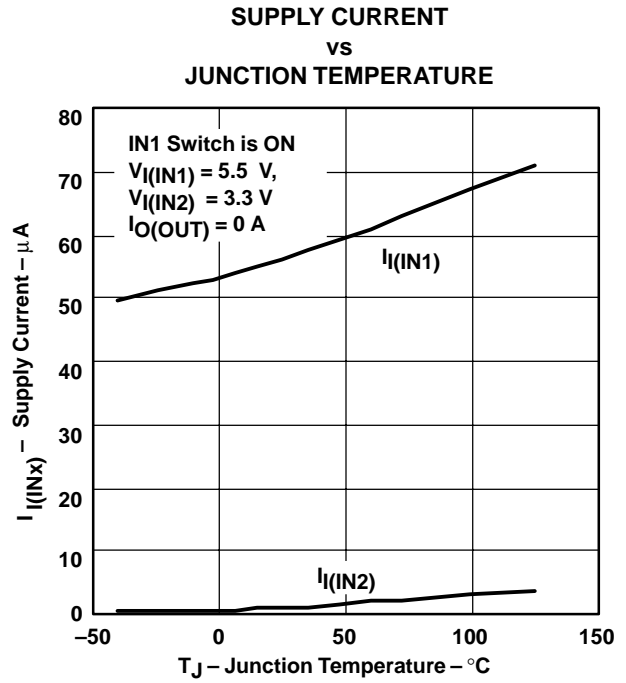**SUPPLY CURRENT**
vs
**JUNCTION TEMPERATURE**

Figure 12

APPLICATION INFORMATION﹘

Some applications have two energy sources, one of which should be used in preference to another. Figure 13 shows a circuit that will connect IN1 to OUT until the voltage at IN1 falls below a user-specified threshold. Once the voltage on IN1 falls below this threshold, the TPS2112/3 will select the higher of the two supplies. This usually means that the TPS2112/3 will swap to IN2.
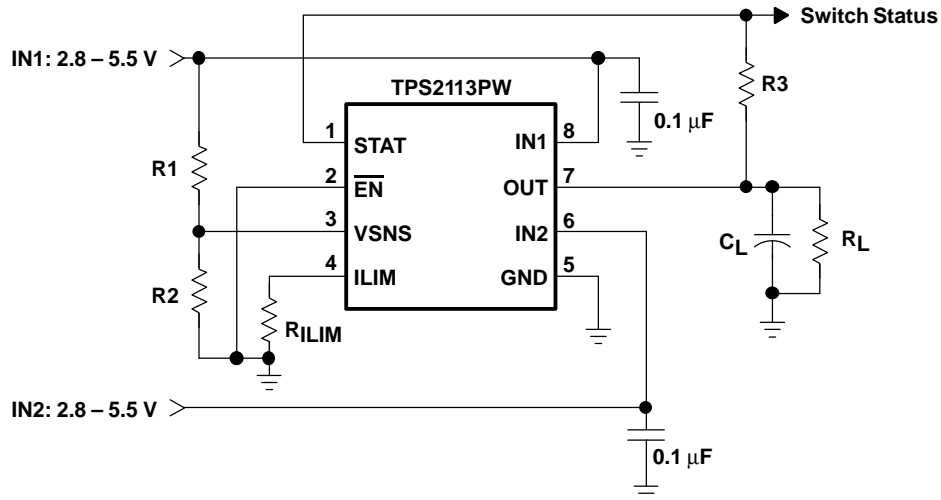
Figure 13. Auto-Selecting for a Dual Power Supply Application

In Figure 14, the multiplexer selects between two power supplies based upon the $\overline{EN}$ logic signal. OUT connects to IN1 if $\overline{EN}$ is logic 1, otherwise OUT connects to IN2. The logic thresholds for the $\overline{EN}$ terminal are compatible with both TTL and CMOS logic.
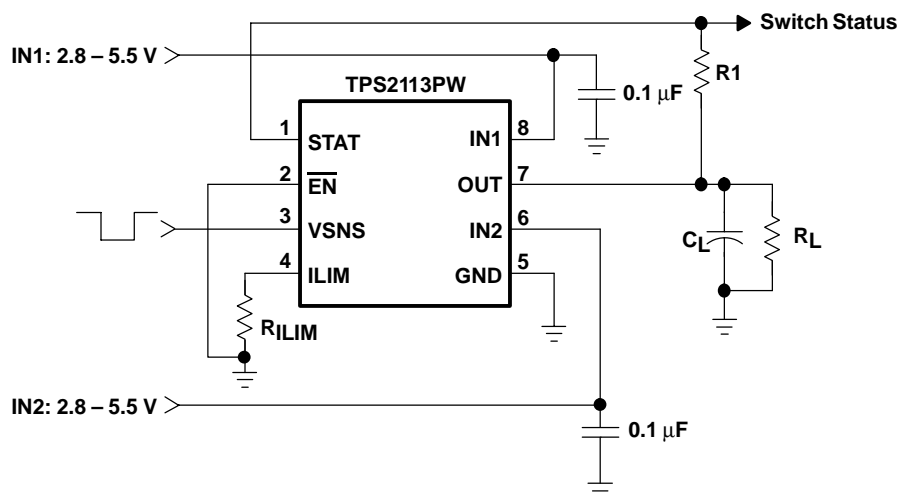
Figure 14. Manually Switching Power Sources

TPS2112
TPS2113

SLVS446 – DECEMBER 2002

TEXAS
INSTRUMENTS
www.ti.com

DETAILED DESCRIPTION

AUTO-SWITCHING MODE

The TPS2112/3 only supports the auto-switching mode. In this mode, OUT connects to IN1 if $V_{I(VSNS)}$ is greater than 0.8 V, otherwise OUT connects to the higher of IN1 and IN2.

The VSNS terminal includes hysteresis equal to 3.75–7.5% of the threshold selected for transition from the primary supply to the higher of the two supplies. This hysteresis helps avoid repeated switching from one supply to the other due to resistive drops.

N-CHANNEL MOSFETs

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turn-on of a FET switch if the output voltage is greater than the input voltage.

CROSS-CONDUCTION BLOCKING

The switching circuitry ensures that both power switches will never conduct at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turn-on threshold voltage.

REVERSE-CONDUCTION BLOCKING

When the TPS211x switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS211x will not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, it will remain connected regardless of output voltage.

CHARGE PUMP

The higher of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

CURRENT LIMITING

A resistor R_{ILIM} from ILIM to GND sets the current limit to 250/ R_{ILIM} and 500/R_{ILIM} for the TPS2112 and TPS2113, respectively. Setting resistor R_{ILIM} equal to zero is not recommended as that disables current limiting.

OUTPUT VOLTAGE SLEW-RATE CONTROL

The TPS2112/3 slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see *Truth Table*).). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can glitch the voltage bus and cause a system to hang up or reset. It can also cause reliability issues—like pit the connector power contacts, when hot plugging a load like a PCI card. The TPS2112/3 slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.
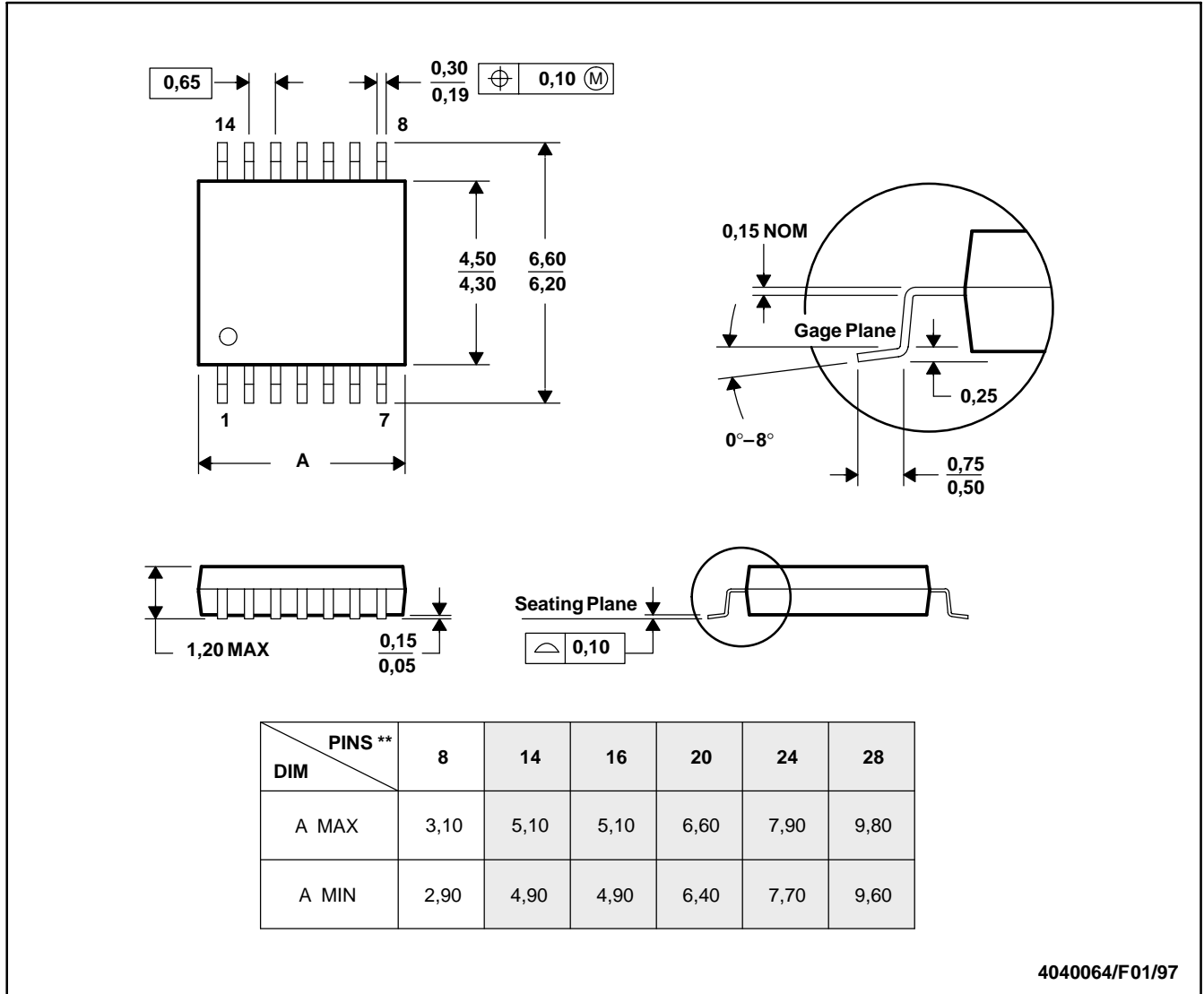
MECHANICAL DATA

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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