



Data sheet acquired from Harris Semiconductor
SCHS186

September 1997

CD74HC393, CD74HCT393

High Speed CMOS Logic Dual 4 -Stage Binary Counter

Features

- Fully Static Operation
- Buffered Inputs
- Common Reset
- Negative-Edge Clocking
- Typical $f_{MAX} = 60$ MHz at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^{\circ}C$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^{\circ}C$ to $125^{\circ}C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at

$V_{CC} = 5V$

- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

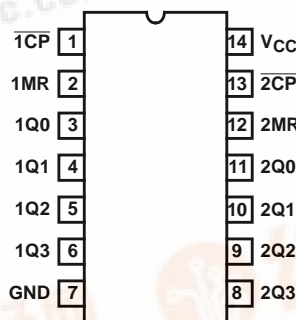
The Harris CD74HC393 and CD74HCT393 are 4-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each clock pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

Ordering Information

| PART NUMBER | TEMP. RANGE ($^{\circ}C$) | PACKAGE | PKG. NO. |
|-------------|-----------------------------|------------|----------|
| CD74HC393E | -55 to 125 | 14 Ld PDIP | E14.3 |
| CD74HCT393E | -55 to 125 | 14 Ld PDIP | E14.3 |

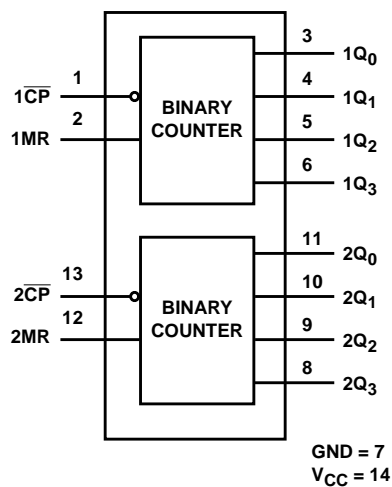
Pinout

CD74HC393, CD74HCT393
(PDIP, SOIC)
TOP VIEW



CD74HC393, CD74HCT393

Functional Diagram



TRUTH TABLE

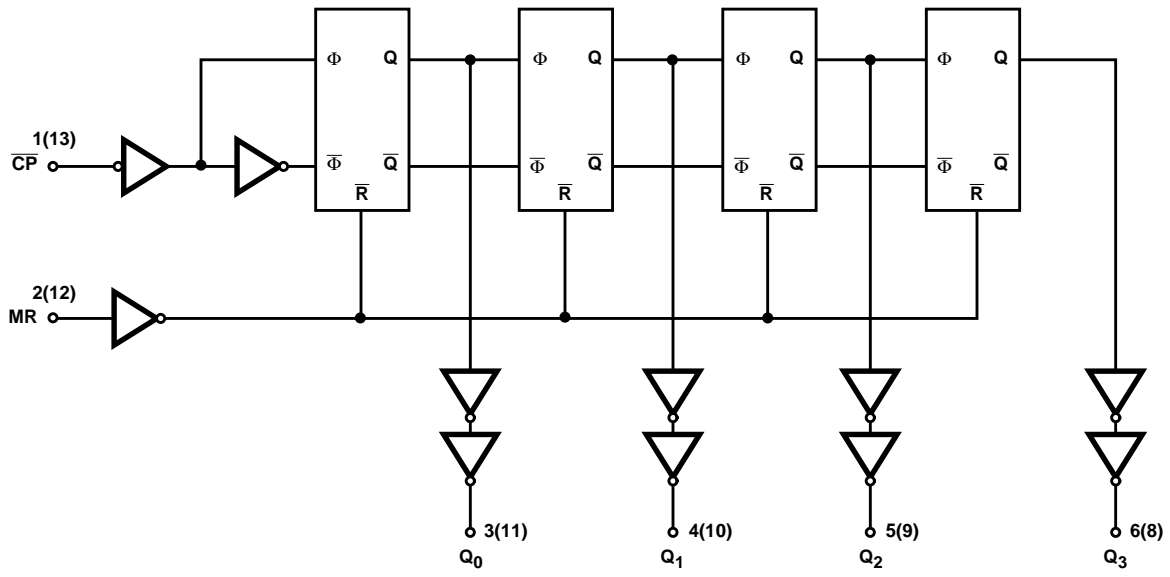
| CP COUNT | OUTPUTS | | | |
|----------|----------------|----------------|----------------|----------------|
| | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |
| 10 | L | H | L | H |
| 11 | H | H | L | H |
| 12 | L | L | H | H |
| 13 | H | L | H | H |
| 14 | L | H | H | H |
| 15 | H | H | H | H |

| CP COUNT | MR | OUTPUT |
|----------|----|-----------|
| ↑ | L | No Change |
| ↓ | L | Count |
| X | H | L L L L |

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care,
 ↑ = Transition from Low to High Level, ↓ = Transition from High to Low.

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Logic Diagram



CD74HC393, CD74HCT393

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} | $\pm 50mA$ |

Thermal Information

| | |
|--|---|
| Thermal Resistance (Typical, Note 3) | θ_{JA} ($^{\circ}C/W$) |
| PDIP Package | 90 |
| SOIC Package | 175 |
| Maximum Junction Temperature | $150^{\circ}C$ |
| Maximum Storage Temperature Range | $-65^{\circ}C$ to $150^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | $300^{\circ}C$ (SOIC - Lead Tips Only) |

Operating Conditions

| | |
|---|----------------------------------|
| Temperature Range (T_A) | $-55^{\circ}C$ to $125^{\circ}C$ |
| Supply Voltage Range, V_{CC} | |
| HC Types | $.2V$ to $6V$ |
| HCT Types | $4.5V$ to $5.5V$ |
| DC Input or Output Voltage, V_I , V_O | $0V$ to V_{CC} |
| Input Rise and Fall Time | |
| $2V$ | $1000ns$ (Max) |
| $4.5V$ | $500ns$ (Max) |
| $6V$ | $400ns$ (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25 $^{\circ}C$ | | | -40 $^{\circ}C$ TO 85 $^{\circ}C$ | | -55 $^{\circ}C$ TO 125 $^{\circ}C$ | | UNITS |
|---|----------|----------------------|------------|--------------|----------------|-----|-----------|-----------------------------------|---------|------------------------------------|---------|---------|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA |
| Quiescent Device Current | I_{CC} | V_{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA |

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DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} and GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI _{CC} | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|-------------------|------------|
| n \overline{CP} | 0.4 |
| nMR | 1 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Prerequisite for Switching Specifications

| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|-------------------------|------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | |
| Maximum Clock Frequency | f _{MAX} | 2 | 6 | - | - | 5 | - | 4 | - | ns |
| | | 4.5 | 30 | - | - | 24 | - | 20 | - | ns |
| | | 6 | 35 | - | - | 28 | - | 24 | - | ns |
| Clock Pulse Width | t _W | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| Reset Recovery Time | t _{REC} | 2 | 5 | - | - | 5 | - | 5 | - | ns |
| | | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| | | 6 | 5 | - | - | 5 | - | 5 | - | ns |

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Prerequisite for Switching Specifications (Continued)

| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|-------------------------|------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Reset Pulse Width | t _W | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| HCT TYPES | | | | | | | | | | |
| Maximum Clock Frequency | f _{MAX} | 4.5 | 27 | - | - | 22 | - | 18 | - | MHz |
| Clock Pulse Width | t _W | 4.5 | 19 | - | - | 24 | - | 29 | - | ns |
| Reset Recovery Time | t _{REC} | 4.5 | 5 | - | - | 5 | - | 5 | - | ns |
| Reset Pulse Width | t _W | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |

Switching Specifications Input t_r, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|--|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| Propagation Delay Time (Figure 1) Q _n to Q _n + 1 | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 45 | - | 55 | - | 70 | ns |
| | | | 4.5 | - | - | 9 | - | 11 | - | 14 | ns |
| | | C _L = 15pF | 5 | - | 4 | - | - | - | - | - | ns |
| | | | 6 | - | - | 8 | - | 9 | - | 12 | ns |
| nCP̄ to nQ ₀ | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 150 | - | 190 | - | 225 | ns |
| | | | 4.5 | - | - | 30 | - | 38 | - | 59 | ns |
| | | C _L = 15pF | 5 | - | 12 | - | - | - | - | - | ns |
| | | | 6 | - | - | 26 | - | 33 | - | 50 | ns |
| nCP̄ to nQ ₁ | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 190 | - | 245 | - | 295 | ns |
| | | | 4.5 | - | - | 38 | - | 49 | - | 59 | ns |
| | | | 6 | - | - | 33 | - | 42 | - | 50 | ns |
| nCP̄ to nQ ₂ | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 240 | - | 300 | - | 360 | ns |
| | | | 4.5 | - | - | 48 | - | 60 | - | 72 | ns |
| | | | 6 | - | - | 41 | - | 51 | - | 61 | ns |
| nCP̄ to nQ ₃ | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 285 | - | 355 | - | 430 | ns |
| | | | 4.5 | - | - | 57 | - | 71 | - | 86 | ns |
| | | | 6 | - | - | 48 | - | 60 | - | 73 | ns |
| MR to Q _n | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 135 | - | 170 | - | 205 | ns |
| | | | 4.5 | - | - | 27 | - | 34 | - | 41 | ns |
| | | C _L = 15pF | 5 | - | 11 | - | - | - | - | - | ns |
| | | | 6 | - | - | 23 | - | 29 | - | 35 | ns |
| Output Transition Time (Figure 1) | t _{TLH} , t _{THL} | C _L = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | C _{IN} | C _L = 50pF | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 4, 5) | C _{PD} | C _L = 15pF | 5 | - | 20 | - | - | - | - | - | pF |

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Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|--------------------|---------------------|-----------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HCT TYPES | | | | | | | | | | | |
| Propagation Delay Time (Figure 1) | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 12 | - | 15 | - | 18 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 4 | - | - | - | - | - | ns |
| Q_n to Q_{n+1} | | | | | | | | | | | |
| $n\overline{CP}$ to nQ_0 | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 32 | - | 40 | - | 48 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 13 | - | - | - | - | - | ns |
| $n\overline{CP}$ to nQ_1 | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 44 | - | 55 | - | 66 | ns |
| $n\overline{CP}$ to nQ_2 | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 50 | - | 63 | - | 75 | ns |
| $n\overline{CP}$ to nQ_3 | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 62 | - | 78 | - | 93 | ns |
| MR to Q_n | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 32 | - | 40 | - | 48 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 13 | - | - | - | - | - | ns |
| Output Transition | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Input Capacitance | C_{IN} | $C_L = 15\text{pF}$ | - | - | - | 10 | - | 10 | - | 10 | pF |
| Power Dissipation Capacitance (Notes 4, 5) | C_{PD} | $C_L = 15\text{pF}$ | 5 | - | 21 | - | - | - | - | - | pF |

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per stage.
5. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

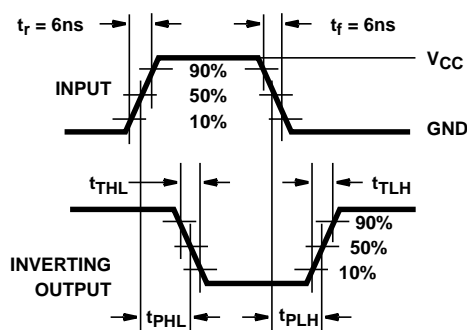


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

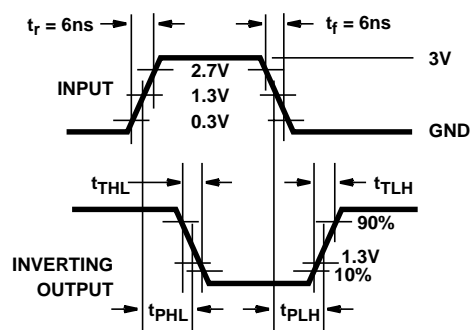


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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