



Data sheet acquired from Harris Semiconductor  
SCHS189

January 1998

# CD74HC540, CD74HCT540, CD74HC541, CD74HCT541

## High Speed CMOS Logic Octal Buffer and Line Drivers, Three-State

### Features

- CD74HC540, CD74HCT540 ..... Inverting
- CD74HC541, CD74HCT541 ..... Non-Inverting
- Buffered Inputs
- Three-State Outputs
- Bus Line Driving Capability
- Typical Propagation Delay = 9ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
  - Standard Outputs ..... 10 LSTTL Loads
  - Bus Driver Outputs ..... 15 LSTTL Loads
- Wide Operating Temperature Range ...  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD74HC540 and CD74HCT540 are Inverting Octal Buffers and Line Drivers with Three-State Outputs and the capability to drive 15 LSTTL loads. The Harris CD74HC541 and CD74HCT541 are Non-Inverting Octal Buffers and Line Drivers with Three-State Outputs that can drive 15 LSTTL loads. The Output Enables ( $\overline{OE1}$  and  $\overline{OE2}$ ) control the Three-State Outputs. If either  $\overline{OE1}$  or  $\overline{OE2}$  is HIGH the outputs will be in the high impedance state. For data output  $\overline{OE1}$  and  $\overline{OE2}$  both must be LOW.

### Ordering Information

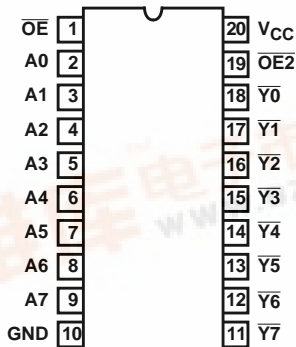
PART NUMBER	TEMP. RANGE ( $^\circ C$ )	PACKAGE	PKG. NO.
CD74HC540E	-55 to 125	20 Ld PDIP	E20.3
CD74HCT540E	-55 to 125	20 Ld PDIP	E20.3
CD74HC541E	-55 to 125	20 Ld PDIP	E20.3
CD74HCT541E	-55 to 125	20 Ld PDIP	E20.3
CD74HC540M	-55 to 125	20 Ld SOIC	M20.3
CD74HCT540M	-55 to 125	20 Ld SOIC	M20.3
CD74HC541M	-55 to 125	20 Ld SOIC	M20.3
CD74HCT541M	-55 to 125	20 Ld SOIC	M20.3

#### NOTES:

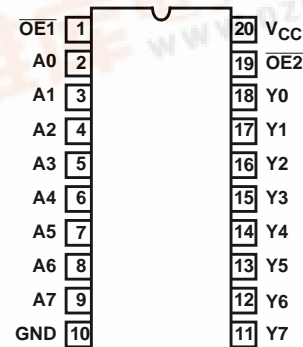
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinouts

CD74HC540, CD74HCT540  
(PDIP, SOIC)  
TOP VIEW

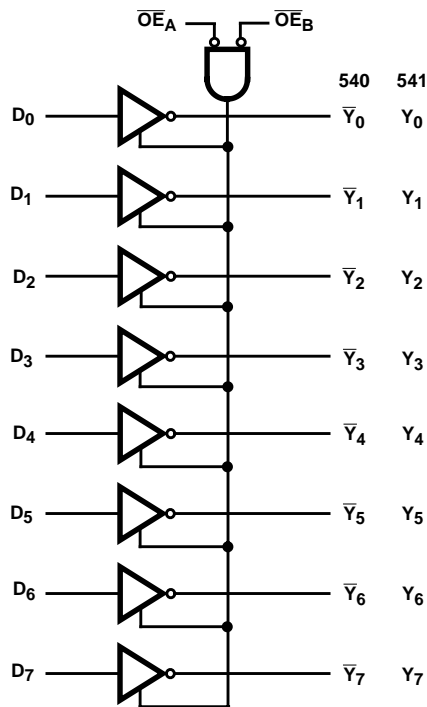


CD74HC541, CD74HCT541  
(PDIP, SOIC)  
TOP VIEW



**CD74HC540, CD74HCT540, CD74HC541, CD74HCT541**

**Functional Diagram**



**TRUTH TABLE**

INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	$A_n$	540	541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

**NOTE:**

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Z = High Impedance

## CD74HC540, CD74HCT540, CD74HC541, CD74HCT541

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 35mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	125
SOIC Package .....	120
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range, $T_A$ .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$

## CD74HC540, CD74HCT540, CD74HC541, CD74HCT541

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
Three-State Leakage Current	I <sub>OZ</sub>	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	6	-	-	±0.5	-	±5.0	-	±10	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Three-State Leakage Current	I <sub>OZ</sub>	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	-	-	±0.5	-	±5.0	-	±10	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE: For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOADS	
	HCT540	HCT541
A0 - A7	1	0.4
OE2	0.75	0.75
OE1	1.15	1.15

NOTE: Unit load is ΔI<sub>CC</sub> limit specific in DC Electrical Specifications Table, e.g., 360μA max. at 25°C.

**CD74HC540, CD74HCT540, CD74HC541, CD74HCT541**

**Switching Specifications**  $C_L = 50\text{pF}$ , Input  $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay Data to Outputs (540)	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	110	-	140	-	165	ns
			4.5	-	-	22	-	28	-	33	ns
		$C_L = 15\text{pF}$	5	-	9	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	19	-	24	-	28	ns
Data to Outputs (541)	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	2	-	-	115	-	145	-	175	ns
			4.5	-	-	23	-	29	-	35	ns
		$C_L = 15\text{pF}$	5	-	9	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	20	-	25	-	30	ns
Output Enable and Disable to Outputs (540)	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
		$C_L = 15\text{pF}$	5	-	13	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	27	-	34	-	41	ns
Output Enable and Disable to Outputs (541)	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	23	-	29	-	35	ns
Output Transition Time	$t_{THL}, t_{TLH}$	$C_L = 50\text{pF}$	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			6	-	-	10	-	13	-	15	ns
Input Capacitance	$C_I$	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	$C_O$	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 4, 5) (540)	$C_{PD}$	$C_L = 15\text{pF}$	5	-	50	-	-	-	-	-	pF
Power Dissipation Capacitance (Notes 4, 5) (541)	$C_{PD}$	$C_L = 15\text{pF}$	5	-	48	-	-	-	-	-	pF
<b>HCT TYPES</b>											
Propagation Delay Data to Outputs (540)	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	24	-	30	-	36	ns
		$C_L = 15\text{pF}$	5	-	9	-	-	-	-	-	ns
Data to Outputs (541)	$t_{PHL}, t_{PLH}$	$C_L = 50\text{pF}$	4.5	-	-	28	-	35	-	42	ns
		$C_L = 15\text{pF}$	5	-	11	-	-	-	-	-	ns
Output Enable and Disable to Outputs (540, 541)	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	12	-	15	-	18	ns
Input Capacitance	$C_I$	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF

## CD74HC540, CD74HCT540, CD74HC541, CD74HCT541

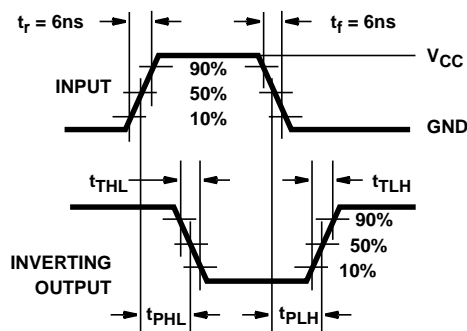
### Switching Specifications $C_L = 50\text{pF}$ , Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Three-State Output Capacitance	$C_O$	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 4, 5) (540, 541)	$C_{PD}$	$C_L = 15\text{pF}$	5	-	55	-	-	-	-	-	pF

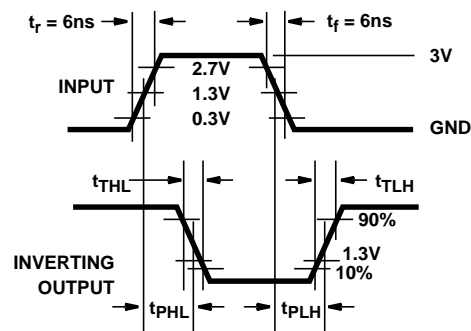
**NOTES:**

4.  $C_{PD}$  is used to determine the dynamic power consumption, per channel.
5.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

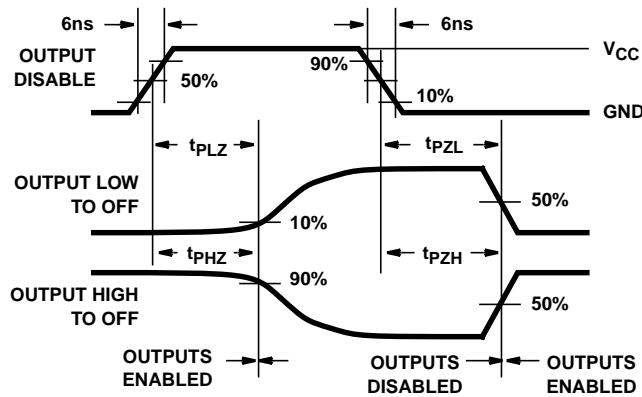
### Test Circuits and Waveforms



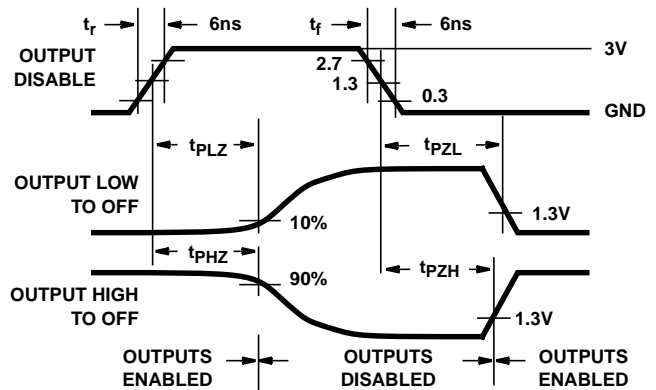
**FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

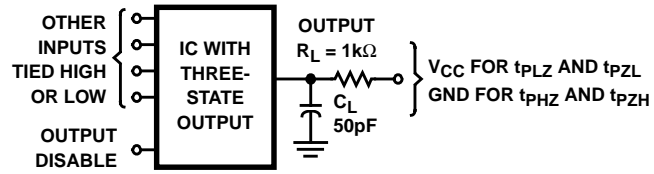


**FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM**



**FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM**

**Test Circuits and Waveforms** (Continued)



NOTE: Open drain waveforms  $t_{pLZ}$  and  $t_{pZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

**FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT**

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

**CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.**

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.