



February 2005

# LM5034 High Voltage Dual Interleaved Current Mode Controller with Active Clamp

## General Description

The LM5034 dual current mode PWM controller contains all the features needed to control either two independent forward/active clamp dc/dc converters or a single high current converter comprised of two interleaved power stages. The two controller channels operate 180° out of phase thereby reducing input ripple current. The LM5034 includes a startup regulator that operates over a wide input range up to 100V and compound (bipolar + CMOS) gate drivers that provide a robust 2.5A peak sink current. The adjustable dead-time of the active clamp gate drivers and adjustable maximum PWM duty cycle reduce stress on the primary side MOSFET switches. Additional features include programmable line under-voltage lockout, cycle-by-cycle current limit, hiccup mode fault operation with adjustable restart delay, PWM slope compensation, soft-start, and a 2 MHz capable oscillator with synchronization capability.

## Features

- Two independent PWM current mode controllers
- Integrated high voltage startup regulator
- Compound 2.5A main output gate drivers
- Single resistor oscillator setting to 2 MHz
- Synchronizable oscillator
- Active clamp gate driver for P-channel MOSFETs
- Adjustable gate drive overlap time
- Programmable maximum duty cycle
- Maximum duty cycle fold-back at high line voltage
- Adjustable timer for hiccup mode current limiting
- Integrated slope compensation
- Adjustable line under-voltage lockout
- Independently adjustable soft-start (each regulator)
- Direct interface with opto-coupler transistor
- Thermal shutdown

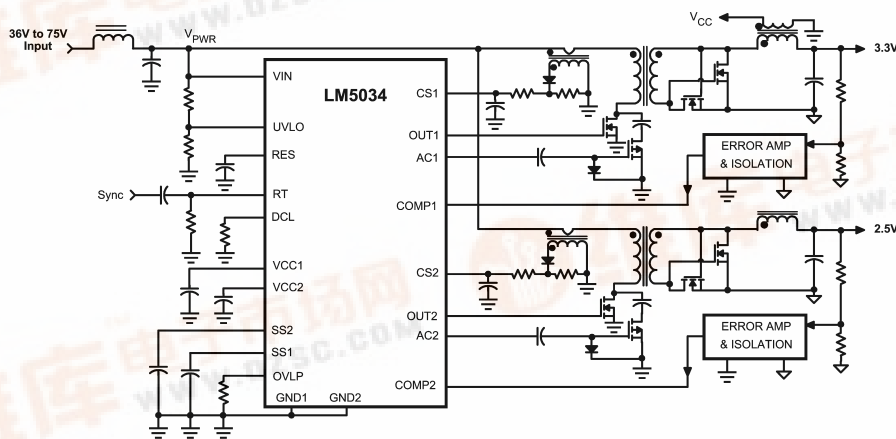
## Applications

- Telecommunication Power Converters
- Industrial Power Converters
- +42V Automotive Systems

## Packages

- TSSOP-20

## Typical Application Circuit



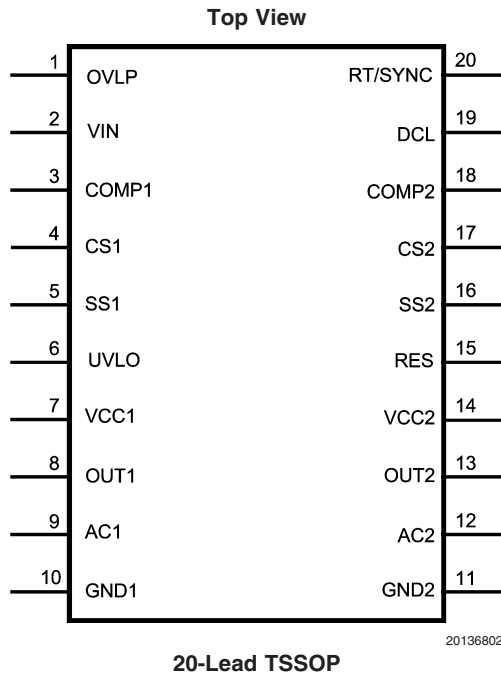
Dual Interleaved Regulators with Independent Outputs

20136801

LM5034 High Voltage Dual Interleaved Current Mode Controller with Active Clamp



## Connection Diagram



## Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM5034MTC	TSSOP-20	MTC-20	73 Units per Rail
LM5034MTCX	TSSOP-20	MTC-20	2500 Units on Tape and Reel

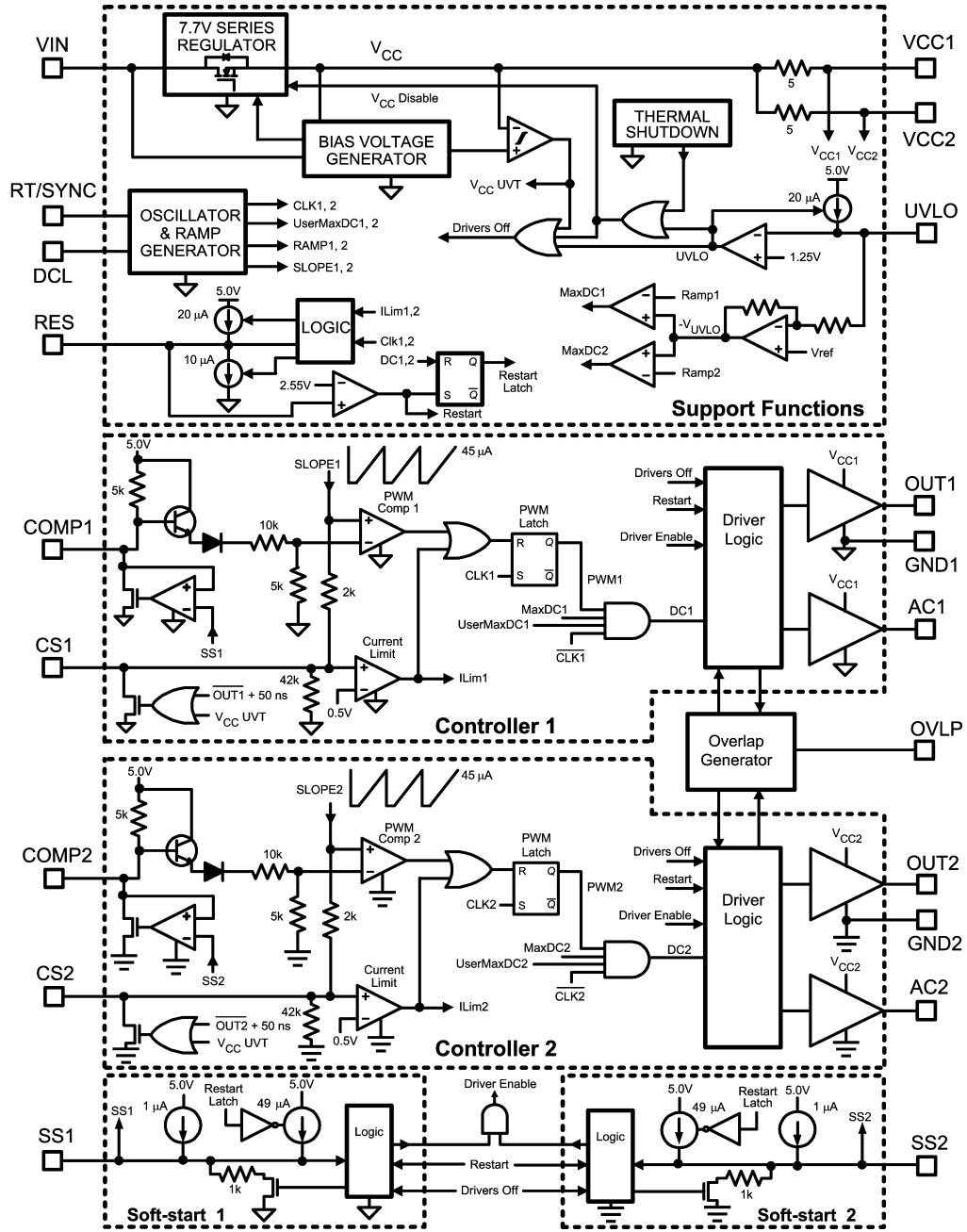
## Pin Description

PIN	NAME	DESCRIPTION	APPLICATIONS INFORMATION
1	OVLP	Active Clamp Overlap Adjust	An external resistor (10 k $\Omega$ to 100 k $\Omega$ ) sets the overlap time of the active clamp outputs relative to the main outputs for both Controller 1 and Controller 2. The overlap time results in deadtime between each main switch and its active clamp switch.
2	VIN	Input Supply	Input to the startup regulator. The operating input range is 13V to 100V with transient capability to 105V.
3	COMP1	PWM Control, Controller 1	The COMP1 input provides voltage feedback to the PWM comparator inverting input of Controller 1 through a 3:1 divider. The OUT1 duty cycle increases as the COMP1 voltage increases. An internal 5K $\Omega$ pull-up resistor to +5.0V provides bias current to an opto-coupler transistor.
4	CS1	Current Sense Input, Controller 1	Input for current mode control and the current limit sensing. If the CS1 pin exceeds 0.5V the OUT1 pulse is terminated producing cycle-by-cycle current limiting. External resistance connected to CS1 will adjust (increase) PWM slope compensation. This pin's voltage must not exceed 1.25V.
5	SS1	Soft-start, Controller 1	An internal 50 $\mu$ A current source charges an external capacitor to set the soft-start rate. During a current limit restart sequence, the internal current source is reduced to 1 $\mu$ A to increase the delay before retry. Forcing SS1 below 0.5V shuts off Controller 1.

## Pin Description (Continued)

PIN	NAME	DESCRIPTION	APPLICATIONS INFORMATION
6	UVLO	VIN Under-Voltage Lockout	An external resistor divider sets the input voltage threshold to enable the LM5034. The UVLO comparator reference voltage is 1.25V. A switched 20 $\mu$ A current source provides adjustable UVLO hysteresis. The UVLO pin voltage also controls the maximum duty cycle as described in the Functional Description section.
7	VCC1	Start-up regulator output, Controller 1	Output of the 7.7V high voltage start-up regulator for Controller 1. The sum of the currents drawn from VCC1 and VCC2 should not exceed 19 mA.
8	OUT1	Main Gate Driver, Controller 1	Gate driver output to the primary side switch for Controller 1. OUT1 swings between VCC1 and GND1 at a frequency equal to half the oscillator frequency.
9	AC1	Active Clamp Driver, Controller 1	Gate driver output to the active clamp P-channel MOSFET for Controller 1. The AC1 pulse overlaps the leading and trailing edges of the OUT1 pulse by an interval set by the OVLP pin resistor. The overlap produces deadtime between the main switch transistor and the P-channel active clamp transistor.
10	GND1	Ground, Controller 1	Ground connection for Controller 1 including gate drivers, PWM controller, soft-start and support functions.
11	GND2	Ground, Controller 2	Ground connection for Controller 2 including gate drivers, PWM controller and soft-start.
12	AC2	Active Clamp Driver, Controller 2	Gate driver output to the active clamp P-channel MOSFET for Controller 2. The AC2 pulse overlaps the leading and trailing edges of the OUT2 pulse by an interval set by the OVLP pin resistor. The overlap produces deadtime between the main switch transistor and the P-channel active clamp transistor.
13	OUT2	Main Gate Driver, Controller 2	Gate driver output to the primary side switch for Controller 2. OUT2 swings between VCC2 and GND2 at a frequency equal to half the oscillator frequency.
14	VCC2	Start-up regulator output, Controller 2	Output of the 7.7V high voltage start-up regulator for Controller 2. The sum of the currents drawn from VCC1 and VCC2 should not exceed 19 mA.
15	RES	Hiccup mode restart adjust	An external capacitor sets the time delay before forced restart during a sustained period of cycle-by-cycle current limiting. The hiccup mode comparator threshold is 2.55V.
16	SS2	Soft-start, Controller 2	An internal 50 $\mu$ A current source charges an external capacitor to set the soft-start rate. During a current limit restart sequence, the internal current source is reduced to 1 $\mu$ A to increase the delay before retry. Forcing SS2 below 0.5V shuts off Controller 2.
17	CS2	Current Sense Input, Controller 2	Input for current mode control and the current limit sensing. If the CS2 pin exceeds 0.5V the OUT2 pulse is terminated producing cycle-by-cycle current limiting. External resistance connected to CS2 will adjust (increase) PWM slope compensation. This pin's voltage must not exceed 1.25V.
18	COMP2	PWM Control, Controller 2	The COMP2 input provides voltage feedback to the PWM comparator inverting input of Controller 2 through a 3:1 divider. The OUT2 duty cycle increases as the COMP2 voltage increases. An internal 5k $\Omega$ pull-up resistor to +5.0V provides bias current to the opto-coupler transistor.
19	DCL	Duty Cycle Limit	An external resistor sets the maximum allowed duty cycle at OUT1 and OUT2.
20	RT/SYNC	Oscillator Adjust and Synchronizing input	An external resistor sets the oscillator frequency. This pin also accepts ac-coupled synchronization pulses from an external source.

# Block Diagram



20136803

FIGURE 1. Detailed Block Diagram

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

VIN to GND	-0.3V to 105V
VCC to GND	-0.3V to 16V
RT/SYNC, RES and DCL to GND	-0.3V to 5.5V
CS Pins to GND	-0.3V to 1.25V
All other inputs to GND	-0.3V to 7V
ESD Rating (Note 5)	
Human Body Model	2kV

Storage Temperature Range	-55°C to 150°C
Junction Temperature	150°C
Lead Temperature (Soldering 4 sec), (Note 2)	260°C

## Operating Ratings (Note 1)

VIN Voltage	13.0V to 100V
External Voltage Applied to VCC1, VCC2	8V to 15V
Operating Junction Temperature	-40°C to +125°C

## Electrical Characteristics

Specifications with standard typeface are for  $T_J = 25^\circ\text{C}$ , and those with **boldface** type apply over full **Operating Junction Temperature range**. VIN = 48V, VCC1 = VCC2 = 10V externally applied,  $R_T = R_{DCL} = 42.2\text{k}\Omega$ ,  $R_{OVL P} = 70\text{k}\Omega$ , UVLO = 1.5V, unless otherwise stated (Note 3) and (Note 4).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Startup Regulator (VIN, VCC1, VCC2 Pins)</b>						
V <sub>CCReg</sub>	V <sub>CC</sub> voltage	VCC1 connected to VCC2, ext. supply disconnected.	<b>7.4</b>	7.7	<b>8</b>	V
I <sub>CC(Lim)</sub>	V <sub>CC</sub> current limit	Sum of currents out of VCC1 and VCC2 with VCC1 = VCC2 = 0V.	<b>19</b>	22		mA
V <sub>CC UVT</sub>	V <sub>CC</sub> Under-voltage threshold (V <sub>CC</sub> increasing)	VCC1 connected to VCC2, ext. supply disconnected, VIN = 11V.	<b>VCC - 300 mV</b>	VCC - 100 mV		V
	V <sub>CC</sub> decreasing		<b>5.5</b>	6.2	<b>6.9</b>	V
I <sub>IN</sub>	Startup regulator current	VIN = 90V, UVLO = 0V		500	<b>600</b>	μA
I <sub>CCIn</sub>	Supply current into VCC from external source	Output loads = open, V <sub>CC</sub> = 10V		4.3	<b>7</b>	mA
<b>UVLO</b>						
UVLO	Under-voltage threshold		<b>1.22</b>	1.25	<b>1.28</b>	V
I <sub>HYST</sub>	Hysteresis current		<b>16</b>	20	<b>24</b>	μA
<b>Current Sense Input (CS1, CS2 Pins)</b>						
CS	Current Limit Threshold		<b>0.45</b>	0.5	<b>0.55</b>	V
	CS delay to output	CS1 (CS2) taken from zero to 1.0V. Time for OUT1 (OUT2) to fall to 90% of VCC1 (VCC2). Output load = 0 pF.		40		ns
	Leading edge blanking time at CS1 (CS2)			50		ns
	CS1 (CS2) sink impedance (clocked)	Internal pull-down FET on.		30	<b>55</b>	Ω
R <sub>CS</sub>	Equivalent input resistance at CS	CS taken from 0.2V to 0.5V, internal FET off.		42		kΩ
<b>Current Limit Restart (RES Pin)</b>						
ResTh	Threshold		<b>2.4</b>	2.55	<b>2.7</b>	V
	Charge source current		<b>15</b>	20	<b>25</b>	μA
	Discharge sink current		<b>7.5</b>	10	<b>12.5</b>	μA
<b>Soft-start (SS1, SS2 Pins)</b>						
I <sub>SS</sub>	Current source (normal operation)		<b>35</b>	50	<b>65</b>	μA
	Current source during a current limit restart		<b>0.7</b>	1	<b>1.3</b>	μA
V <sub>SS</sub>	Open circuit voltage			5		V

## Electrical Characteristics (Continued)

Specifications with standard typeface are for  $T_J = 25^\circ\text{C}$ , and those with **boldface** type apply over full **Operating Junction Temperature range**.  $V_{IN} = 48\text{V}$ ,  $V_{CC1} = V_{CC2} = 10\text{V}$  externally applied,  $R_T = R_{DCL} = 42.2\text{k}\Omega$ ,  $R_{OVL P} = 70\text{k}\Omega$ ,  $UVLO = 1.5\text{V}$ , unless otherwise stated (Note 3) and (Note 4).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Oscillator (RT/SYNC Pin)</b>						
$F_{S1}$	Frequency 1 (at OUT1, OUT2)	$R_T = 42.2\text{ k}\Omega$	<b>183</b>	200	<b>217</b>	kHz
$F_{S2}$	Frequency 2 (at OUT1, OUT2)	$R_T = 13.7\text{ k}\Omega$	<b>530</b>	600	<b>670</b>	kHz
	DC voltage			2		V
	Input Sync threshold		<b>2.6</b>	3.3	<b>3.7</b>	V
<b>PWM Controller (COMP1, COMP2, Duty Cycle Limit Pins)</b>						
	Delay to output	COMP1 (COMP2) set to 2V. CS1 (CS2) stepped from 0 to 0.4V. Time for OUT1 (OUT2) to fall to 90% of VCC1 (VCC2). Output load = 0 pF.		50		ns
$V_{COMP}$	COMP1 (COMP2) open circuit voltage			5		V
$I_{COMP}$	COMP1 (COMP2) short circuit current	COMP1 (COMP2) = 0V	<b>0.6</b>	1	<b>1.4</b>	mA
	COMP1 (COMP2) to PWM1 (PWM2) gain			0.33		V/V
	Minimum duty cycle	SS1 (SS2) = 0V			<b>0</b>	%
	Maximum duty cycle 1	UVLO pin = 1.30V, $R_{DCL} = R_T$ , COMP1 (COMP2) = open		76		%
	Maximum duty cycle 2	UVLO pin = 3.75V, $R_{DCL} = R_T$ , COMP1 (COMP2) = open		20		%
	Maximum duty cycle 3	UVLO pin = 1.30V, $R_{DCL} = R_T/4$ , COMP1 (COMP2) = open		20		%
	Maximum duty cycle 4	UVLO pin = 2.50V, $R_{DCL} = R_T$ , COMP1 (COMP2) = open		50		%
	Maximum duty cycle 5	UVLO pin = 1.30V, $R_{DCL} = R_T/2$ , COMP1 (COMP2) = open		40		%
	Slope compensation	Delta increase at PWM comparator to CS1 (CS2)		90		mV
	Channel mismatch	CS1 (CS2) = 0.25V			<b>7</b>	%
	Soft-start to COMP offset	SS1 (SS2) = 0.8V		0		V
<b>Main Output Drivers (OUT1, OUT2)</b>						
	Output high voltage	$I_{OUT} = 50\text{mA}$ (source)	<b>VCC-1</b>	VCC-0.2		V
	Output low voltage	$I_{OUT} = 100\text{ mA}$ (sink)		0.3	<b>1</b>	V
	Rise time	$C_{LOAD} = 1\text{ nF}$		12		ns
	Fall time	$C_{LOAD} = 1\text{ nF}$		10		ns
	Peak source current			1.5		A
	Peak sink current			2.5		A

## Electrical Characteristics (Continued)

Specifications with standard typeface are for  $T_J = 25^\circ\text{C}$ , and those with **boldface** type apply over full **Operating Junction Temperature range**.  $V_{IN} = 48\text{V}$ ,  $V_{CC1} = V_{CC2} = 10\text{V}$  externally applied,  $R_T = R_{DCL} = 42.2\text{k}\Omega$ ,  $R_{OVL P} = 70\text{k}\Omega$ ,  $UVLO = 1.5\text{V}$ , unless otherwise stated (Note 3) and (Note 4).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Active Clamp Output Drivers (AC1, AC2)</b>						
	Output high voltage	$I_{OUT} = 10\text{mA}$ (source)	<b>VCC-0.5</b>	VCC-0.2		V
	Output low voltage	$I_{OUT} = 20\text{mA}$ (sink)		0.1	<b>0.5</b>	V
	Rise time	$C_{LOAD} = 1.0\text{nF}$		44		ns
	Fall time	$C_{LOAD} = 1.0\text{nF}$		22		ns
	Peak source current			0.1		A
	Peak sink current			0.25		A
	Overlap time	$R_{OVL P} = 70\text{k}\Omega$	<b>75</b>	100	<b>125</b>	ns
<b>Thermal Shutdown</b>						
$T_{SD}$	Shutdown temperature			165		$^\circ\text{C}$
	Hysteresis			20		$^\circ\text{C}$
<b>Thermal Resistance</b>						
$\theta_{JA}$	Junction to ambient, 0 LFPM Air Flow	TSSOP-20 package		120		$^\circ\text{C}/\text{W}$

**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

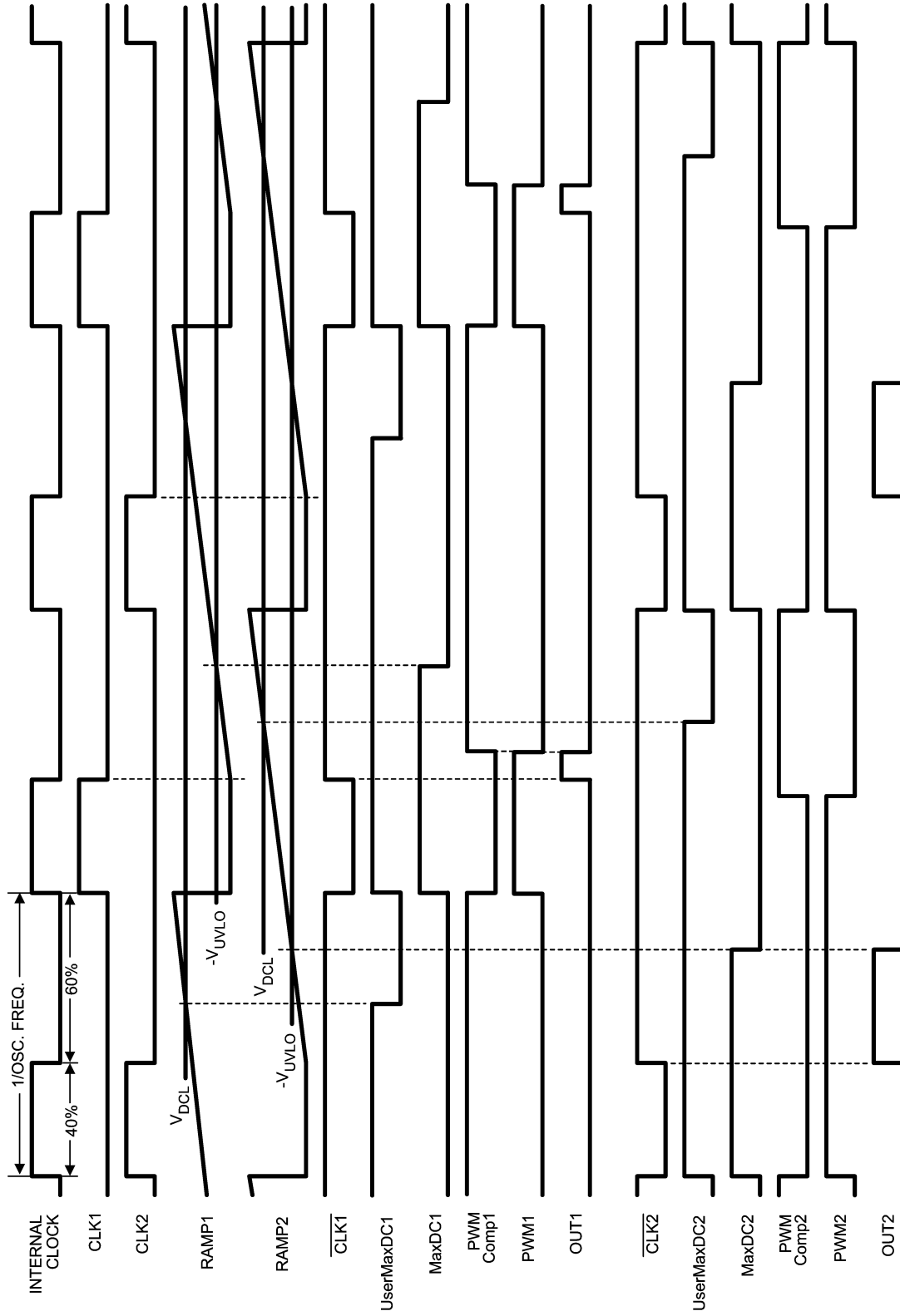
**Note 2:** For detailed information on soldering plastic TSSOP packages, refer to the Packaging Data Book available from National Semiconductor Corporation.

**Note 3:** All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production with  $T_A = 25^\circ\text{C}$ . All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

**Note 4:** Typical specifications represent the most likely parametric norm at  $25^\circ\text{C}$  operation

**Note 5:** The human body model is a  $100\text{pF}$  capacitor discharged through a  $1.5\text{k}\Omega$  resistor into each pin.

### Timing Diagram



20136804

FIGURE 2. Internal Timing Diagram



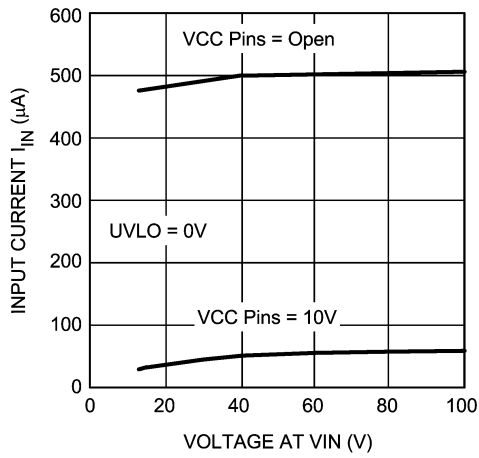
Timing Diagram (Continued)



20136805

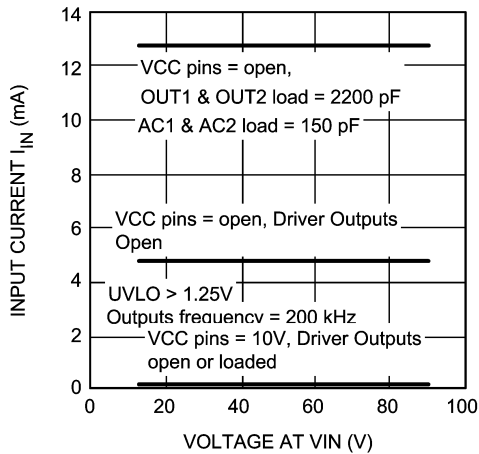
FIGURE 3. Startup Sequence

# Typical Performance Characteristics



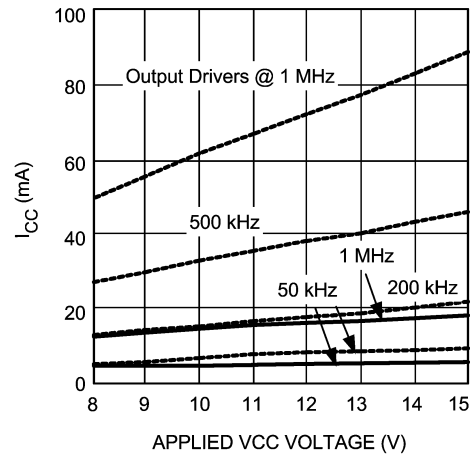
20136806

FIGURE 4.  $I_{IN}$  vs  $V_{IN}$



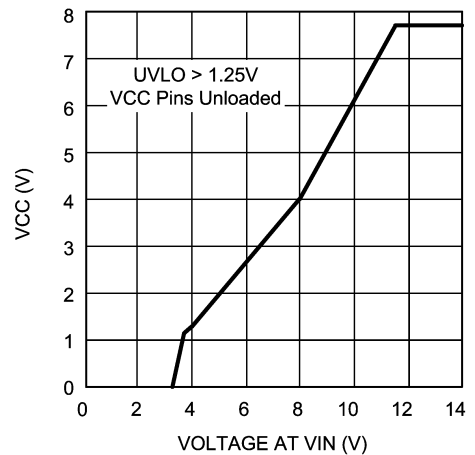
20136807

FIGURE 5.  $I_{IN}$  vs  $V_{IN}$



20136808

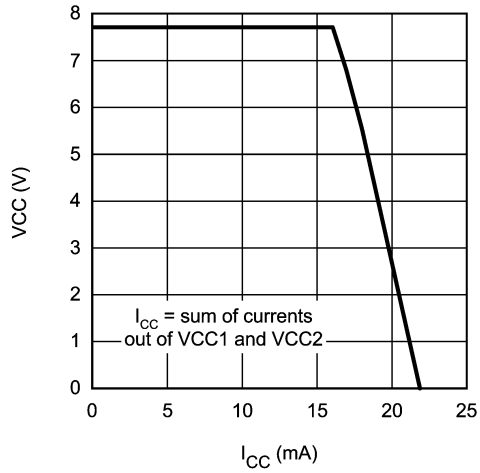
FIGURE 6.  $I_{CC}$  vs Externally Applied VCC



20136809

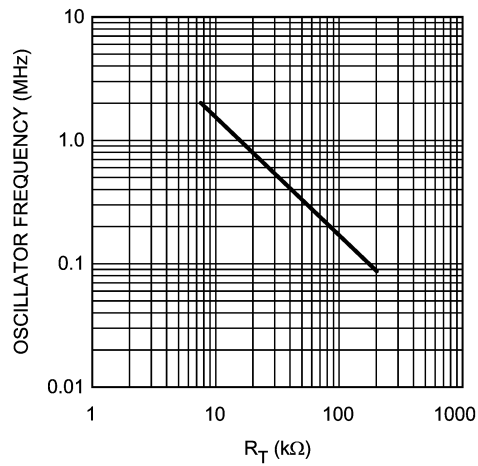
FIGURE 7. VCC vs  $V_{IN}$

### Typical Performance Characteristics (Continued)



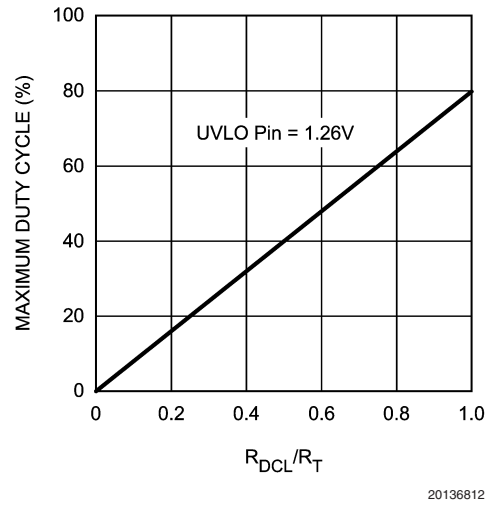
20136810

FIGURE 8. VCC vs  $I_{CC}$  (Externally Loaded)



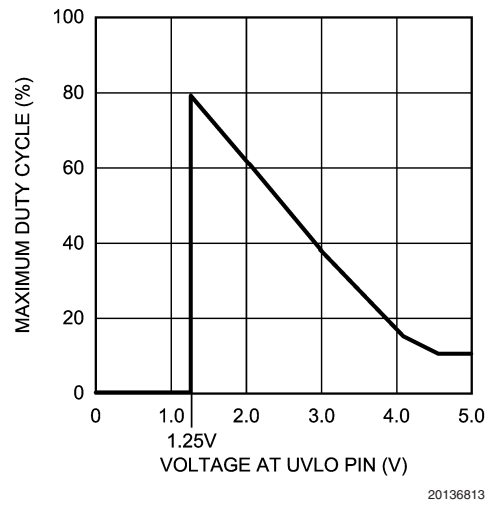
20136811

FIGURE 9. Oscillator Frequency vs  $R_T$  Resistor



20136812

FIGURE 10. User Defined Maximum Duty Cycle vs.  $R_{DCL}$  Resistor



20136813

FIGURE 11. Maximum Duty Cycle vs. UVLO Voltage

## Typical Performance Characteristics (Continued)

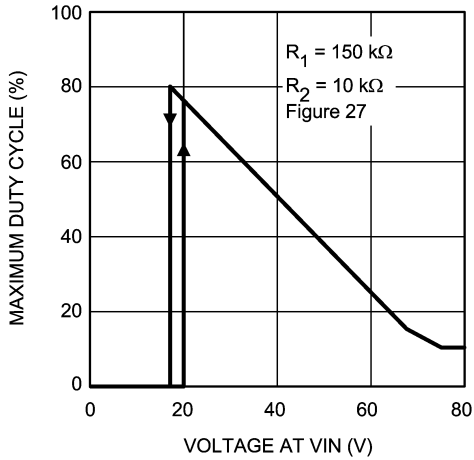


FIGURE 12. Maximum Duty Cycle vs. VIN (Figure 29)

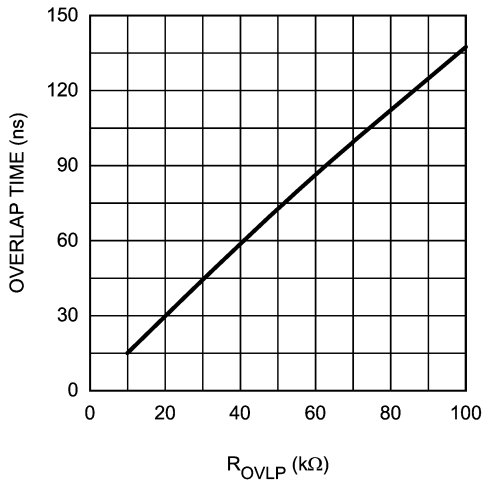


FIGURE 13. Active Clamp Overlap Time vs.  $R_{OVLP}$

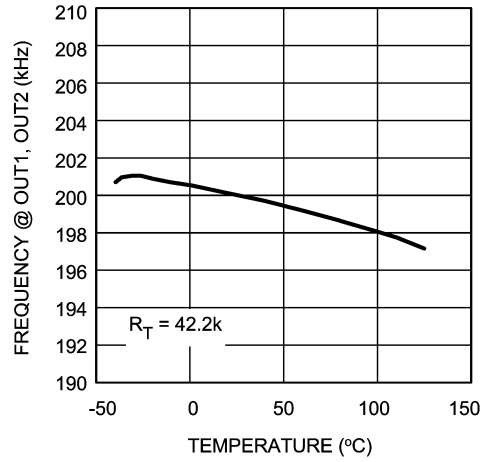


FIGURE 14. Frequency vs. Temperature

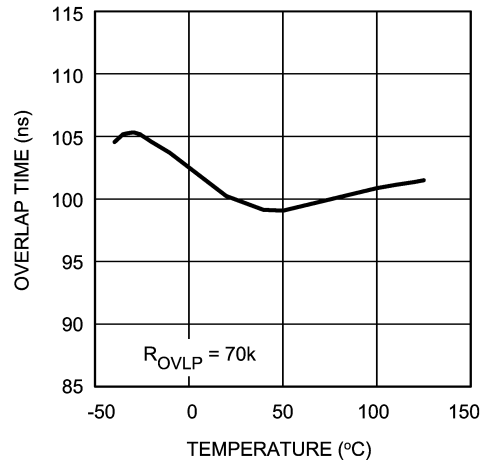


FIGURE 15. Overlap Time vs. Temperature

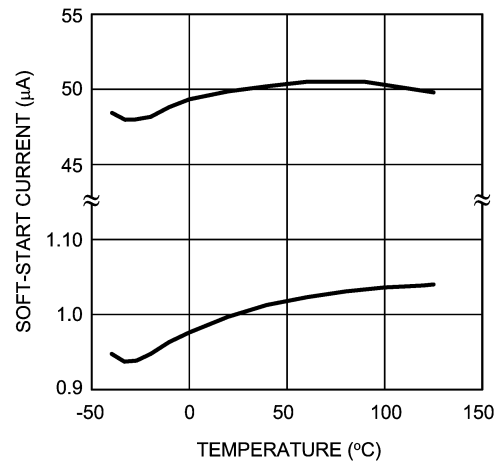
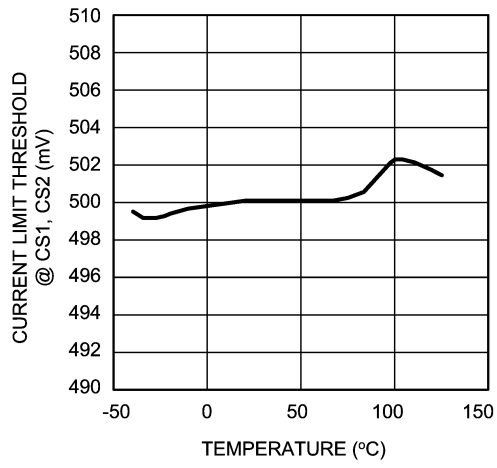


FIGURE 16. Soft-start Pin Current vs. Temperature

### Typical Performance Characteristics (Continued)



20136819

**FIGURE 17. Current Limit Threshold at CS1, CS2 vs. Temperature**



## Drivers Off, $V_{CC}$ Disable (Continued)

Off signal to disable the output drivers, connect the SS1, SS2, COMP1, COMP2 and RES pins to ground, and enable the 50  $\mu$ A Soft-start current sources.

If the  $V_{CC}$  voltage falls below the under-voltage threshold of 6.2V, the UVT comparator activates only the Drivers Off signal. The output drivers are disabled but the  $V_{CC}$  regulator is not disabled. Additionally, the CS1, CS2, SS1, SS2, COMP1, COMP2 and RES pins are internally grounded, and the 50  $\mu$ A Soft-start current sources are enabled.

## Oscillator

The oscillator frequency is set with an external resistor  $R_T$  connected between the RT/SYNC and GND1 pins. The resistor value is calculated from:

$$R_T = \frac{17100}{F_S} - 0.001(F_S - 400) \quad (1)$$

where  $F_S$  is the desired oscillator frequency in kHz (maximum of 2 MHz), and  $R_T$  is in k $\Omega$ . See Figure 9. The two gate driver outputs (OUT1 and OUT2) switch at half the oscillator frequency and 180° out of phase with each other. The voltage at the  $R_T$ /SYNC pin is internally regulated at 2.0V. The  $R_T$  resistor should be located as close as possible to the LM5034 with short direct connections to the pins.

The LM5034 can be synchronized to an external clock by applying a narrow clock pulse to the  $R_T$ /SYNC pin. See the Applications Information section for details on this procedure. The  $R_T$  resistor is always required, whether the oscillator is free running or externally synchronized.

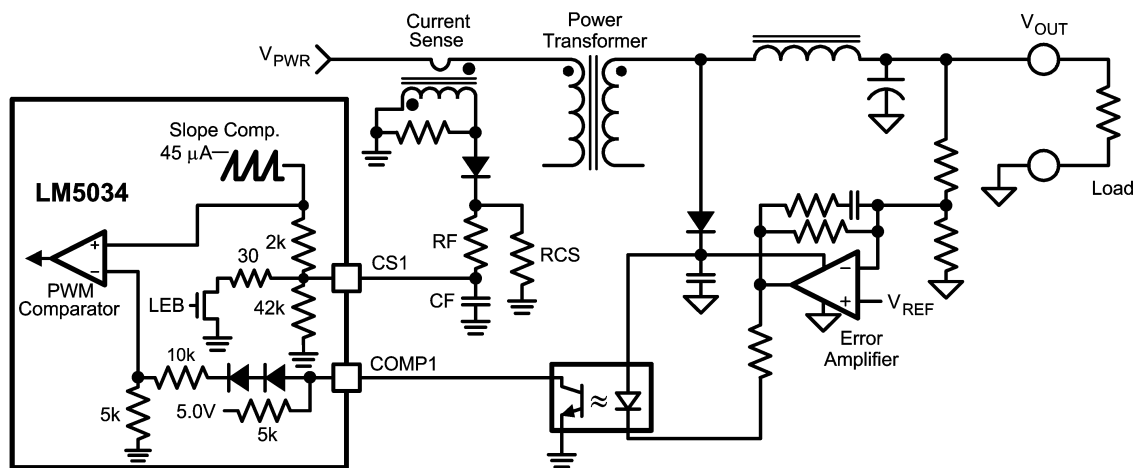
## PWM Comparator/Slope Compensation

The PWM comparator of each controller compares a slope compensated current ramp signal with the loop error voltage derived from the COMP pin. The COMP voltage is typically

controlled by an external error amplifier/optocoupler feedback circuit to regulate the converter output voltage. Internally, the voltage at the COMP pin passes through two level shifting diodes and a gain reducing 3:1 resistor divider (see Figure 19). The compensated current ramp signal is a combination of the current waveform at the CS pin, and an internally generated ramp derived from the internal clock. At duty cycles greater than 50% current mode control circuits are prone to subharmonic oscillation. By adding a small fixed ramp to the external current sense signal oscillations can be avoided. The internal ramp has an amplitude of 45  $\mu$ A and is sourced into an internal 2k $\Omega$  resistor, and a 42 k $\Omega$  resistor in parallel with the external impedance at the CS pin. The ramp current also flows through the external impedance connected to the CS pin and thus, the amount of slope compensation can be adjusted by varying the external circuit at the CS pin.

The output of the PWM comparator provides the pulse width information to the output drivers. This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The comparator's output duty cycle is 0% for  $V_{COMP} \leq 1.5V$ , and increases as  $V_{COMP}$  increases.

If either Soft-start pin is pulled low (internally or externally) the corresponding COMP pin is pulled down with it, forcing the output duty cycle to zero. When the Soft-start pin voltage increases, the COMP pin is allowed to increase. An internal 5 k $\Omega$  resistor connected from COMP to an internal 5.0V supply provides a pull-up for the COMP pin and bias current to the collector of the opto-coupler transistor.



20136822

FIGURE 19. Typical Feedback Network

## Cycle-by-Cycle Current Limit

Each CS pin is designed to accept a signal representative of its transformer primary current. If the voltage at CS exceeds 0.5V the current sense comparator terminates the present main output driver (OUT pin) pulse. If the high current fault persists, the controller operates with constant peak switch current in a cycle-by-cycle current limit mode, and a Hiccup Mode Current Limit Restart cycle begins (see below).

Each CS pin is internally connect to ground through a 30Ω resistor during the main output off time to discharge external filter capacitance. The discharge device remains on for an additional 50 ns after the main output driver switches high to blank leading edge transients in the current sensing circuit. Discharging the CS pin filter each cycle and blanking leading edge spikes reduces the filter requirement which improves the current sense response time.

The current sense comparators are fast and respond to short duration noise pulses. The external circuitry at each CS pin should include an R-C filter to suppress noise. Layout considerations are critical for the current sense filter and the sense resistor. Refer to the Applications Information section for PC board layout guidelines.

## Hiccup Mode Current Limit Restart

If cycle-by-cycle current limiting continues in either or both controllers for a sufficient period of time, the Current Limit Restart circuit disables both regulators and initiates a soft-start sequence after a programmable delay. The duration of cycle-by-cycle current limiting before turn-off occurs is programmed by the value of the external capacitor at the RES pin. The dwell time before output switching resumes is programmed by the value of the Soft-start capacitor(s). The circuit is detailed in *Figure 20* and the timing is shown in *Figure 21*. A description of this circuit's operation is as follows:

### a) No current limit detected:

The 10 μA discharge current source at RES is enabled pulling the RES pin to ground.

### b) Current limit repeatedly detected at both CS inputs:

The 20 μA current source at RES is enabled continuously to charge the RES pin capacitor as shown in *Figure 21*. The current limit comparators also terminate the PWM output

pulses to provide a cycle-by-cycle current limiting. When the voltage on the RES capacitor reaches the 2.55V restart comparator threshold, the comparator sets the Restart Latch which produces the following restart sequence:

- The SS1 and SS2 pin charging currents are reduced from 50μA to 1 μA,
- An internal MOSFET is turned on to discharge the RES pin capacitor.
- The internal MOSFETs at SS1 and SS2 are turned on to discharge the Soft-start capacitors.
- COMP1 and COMP2 follow SS1 and SS2 respectively and reduce the PWM duty cycles to zero
- When the voltages at the SS pins fall below 200mV, the internal MOSFETs at the SS pins are turned off allowing the SS pins to be charged by the 1μA current sources.
- When either SS pin reaches  $\approx 1.5V$  its PWM controller produces the first pulse of a soft-start sequence which resets the Restart Latch. The SS charging currents are increased to 50 μA and the soft-start sequence continues at the normal rate.

If the overload condition still exists, the voltage at RES begins to increase again and repeat the restart cycle as shown in *Figure 21*. If the overload condition has been cleared, the RES pin is held at ground by the 10 μA current source.

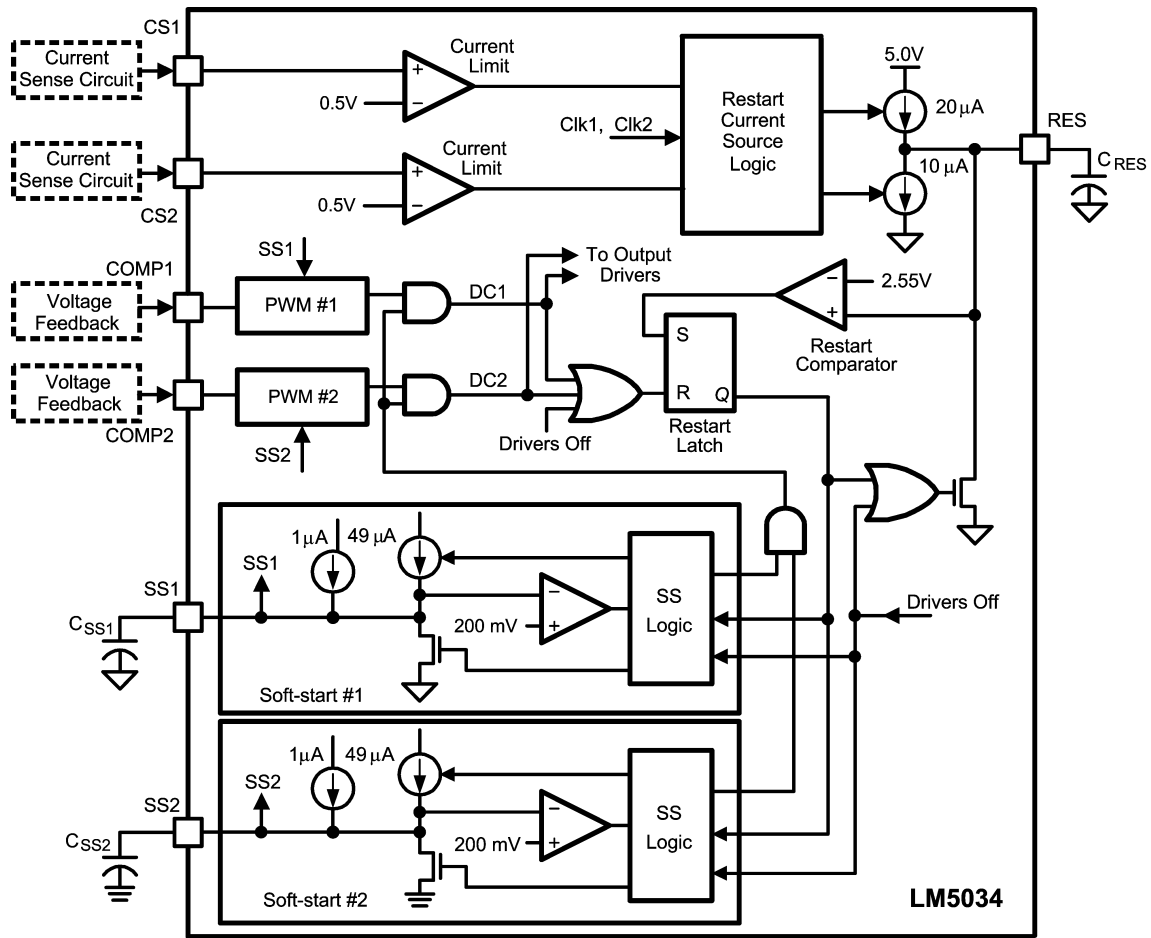
### c) Current limit repeatedly detected at one of the two CS inputs:

In this condition the RES pin capacitor is charged by the 20 μA current source once each clock cycle of the current limited regulator (CLK1 or CLK2), and discharged by the 10 μA current source once each clock cycle of the unaffected regulator. The voltage at the RES pin increases one fourth as fast as in case b) described above. The current limited regulator operates in a cycle-by-cycle current limit mode until the voltage at RES reaches the 2.55V threshold. When the Restart Comparator output switches high the Restart Latch is set, both SS pin capacitors are discharged to disable the regulator channels, and a restart sequence begins as described in case b) above.

To determine the value of the RES pin capacitor, see the Applications Information section.

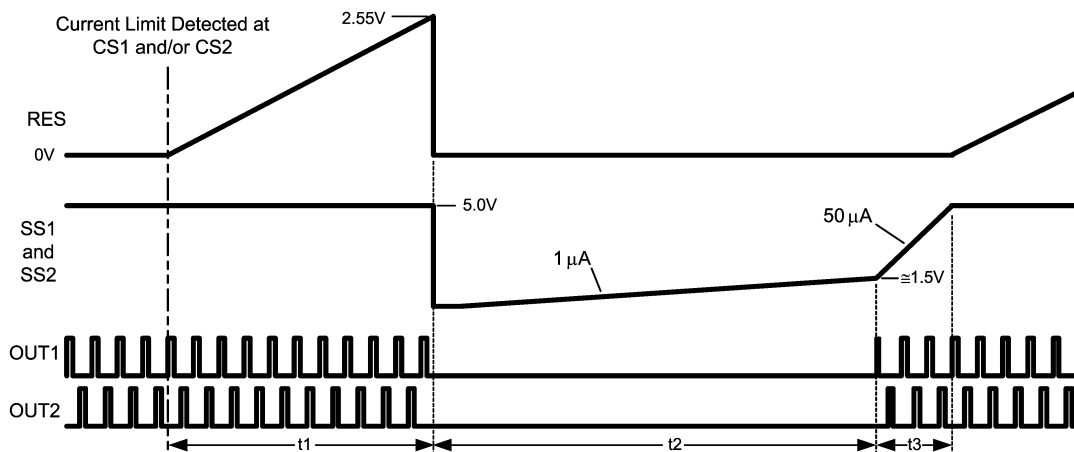


Hiccup Mode Current Limit Restart (Continued)



20136823

FIGURE 20. Current Limit Restart Circuit



20136824

FIGURE 21. Current Limit Restart Timing

## Soft-start

Each soft-start circuit allows the corresponding regulator to gradually reach a steady state operating point, thereby reducing startup current surges and output overshoot. Upon turn-on, both SS pins are internally held at ground. When VCC increases past its under-voltage threshold (UVT), the SS pins are released and internal 50  $\mu\text{A}$  current sources charge the external capacitors. The voltage at each COMP pin follows the SS pin, and when COMP reaches  $\approx 1.5\text{V}$ , the output pulses commence at a low duty cycle. The voltage at the SS pins continues to increase and saturates at  $\approx 5.0\text{V}$ . The voltage at each COMP pin increases to the value required for regulation where it is controlled by its voltage feedback loop (see *Figure 3*).

If the internal Drivers Off line is activated (see the Drivers Off paragraph), both SS pins are internally grounded. The SS pins pull the COMP pins to ground while the Driver Off signal disables the output drivers. When the event which activated the Drivers Off line is cleared and Vcc exceeds its under-voltage threshold, the SS pins are released. The internal 50  $\mu\text{A}$  current sources then charge the external soft-start capacitors allowing each regulator's output duty cycle to increase.

If the Current Limit Restart threshold is reached due to repeated over-current detections, both SS pins (and the COMP pins) are pulled to ground. The output drivers are disabled, and the 50  $\mu\text{A}$  SS pin current sources are reduced to 1  $\mu\text{A}$ . After a short propagation delay the SS pins and the COMP pins are released, and the external capacitors are charged up at a slow rate. When the COMP voltage reaches  $\approx 1.5\text{V}$ , the output drivers are enabled, and the current sources at the SS pins are increased to 50  $\mu\text{A}$ . The output duty cycle then increases to the value required for regulation.

To shutdown one regulator without affecting the other, ground the appropriate SS pin. This forces the COMP pin to ground, reducing the output duty cycle to zero for that regulator. Releasing the SS pin allows normal operation to resume.

## Output Duty Cycle

The output driver's duty cycle for each controller is normally controlled by comparing the voltage provided to the COMP input by the external voltage feedback circuit with the current information at the CS pin. However, the maximum duty cycle during transient or fault conditions may be intentionally limited by two other circuits, both of which are common to the two controller channels.

**User Defined Maximum Duty Cycle.** The maximum allowed duty cycle can be set with the  $R_{\text{DCL}}$  resistor connected from the DCL pin to GND1, according to the following equation:

$$\text{Maximum User Duty Cycle} = 80\% \times R_{\text{DCL}}/R_{\text{T}} \quad (2)$$

$R_{\text{T}}$  is the oscillator frequency programming resistor connected to the  $R_{\text{T}}/\text{SYNC}$  pin. The value of the  $R_{\text{DCL}}$  resistor must be calculated after the  $R_{\text{T}}$  resistor is selected. See *Figure 10*. Referring to the block diagrams of *Figure 1*, and *Figure 2*, the voltage at the DCL pin ( $V_{\text{DCL}}$ ) is compared to the Ramp1 and Ramp2 signals, creating the UserMaxDC1

and UserMaxDC2 timing signals. These signals are provided to the two 4-input AND gates to limit the PWM duty cycle of both channels.

**Line Voltage Maximum Duty Cycle.** The voltage at the UVLO pin, normally proportional to the voltage at  $V_{\text{PWR}}$ , further limits the maximum duty cycle at high input voltages. Referring to *Figure 11*, when the UVLO pin is below 1.25V, the outputs are disabled. At UVLO = 1.25V the maximum allowed duty cycle is 80% (or less if limited by the DCL resistor). As the UVLO pin voltage increases with  $V_{\text{PWR}}$ , the maximum duty cycle decreases, reaching a minimum of 10% at  $\approx 4.5\text{V}$ . Referring to *Figure 1* and *Figure 2*, the UVLO voltage, after passing through an inverting gain stage, is compared to the Ramp1 and Ramp2 signals generated by the oscillator. The output of these comparators are the MaxDC1 and MaxDC2 timing signals. These signals are provided to the two 4-input AND gates which limit the PWM pulses delivered to the output drivers.

**Resulting Output Duty Cycle.** The controller duty cycle is determined by the four signals into the 4-input AND gates in *Figure 1* (UserMaxDC, MaxDC, PWM and CLK). The output driver pulsewidth is equal to the least of these four pulses. Whichever input of the AND gate transitions high-to-low first terminates the output driver's on-time. For example, in *Figure 2*, the OUT1 driver's on-time is set by PWM Comparator #1. The on-time for OUT2 is limited by the UVLO pin voltage (determined by  $V_{\text{PWR}}$ ) even though the PWM Comparator #2 is seeking a higher duty cycle.

## Driver Outputs

OUT1, the primary switch driver for Controller 1 is designed to drive the gate of an N-channel MOSFET with 1.5A sourcing current and 2.5A sinking current. The corresponding active clamp driver, AC1, is designed to drive a P-channel MOSFET and is capable of sourcing 100 mA and sinking 250 mA. The peak output levels at OUT1 and AC1 are VCC1 and GND1. The ground return path for Controller 1 is GND1. The corresponding driver pins for Controller 2 are OUT2, AC2, VCC2 and GND2.

OUT1 and OUT2 are compound gate drivers with CMOS and Bipolar output transistors as shown in *Figure 22*. The parallel MOS and Bipolar devices provide a faster turn-off of the primary switch thereby reducing switching losses. The outputs switch at one-half the oscillator frequency with the rising edges at OUT1 and OUT2 180° out of phase with each other. The on-time of OUT1 and OUT2 is determined by their respective duty cycle control. The active clamp outputs are in phase with their respective main outputs, with their edge timing altered by the overlap control circuit as shown in *Figure 23*. The overlap time provides deadtime between the operation of the primary switch and the active clamp switch at both the rising and falling edges. The overlap times are the same at the rising and falling edges, independent of frequency and duty cycle. The overlap time is programmed by the resistor at the OVLP pin ( $R_{\text{OVLP}}$ ) according to the following equation (see *Figure 13* and *Figure 15*):

$$t_{\text{OVLP}} = (1.25 \times R_{\text{OVLP}}) + 5$$

where  $R_{\text{OVLP}}$  is in  $\text{k}\Omega$ , and  $t_{\text{OVLP}}$  is in ns. The range for  $R_{\text{OVLP}}$  is 10  $\text{k}\Omega$  to 100  $\text{k}\Omega$ . If the application requires zero overlap time, the OVLP pin should be left open.

## Driver Outputs (Continued)

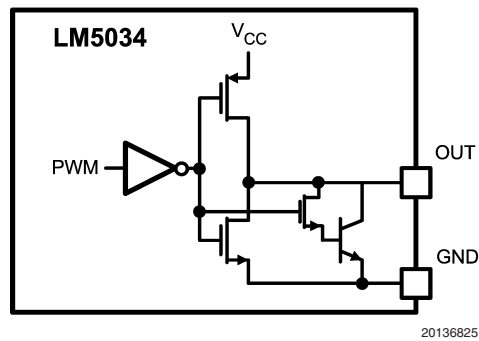


FIGURE 22. Compound Gate Driver

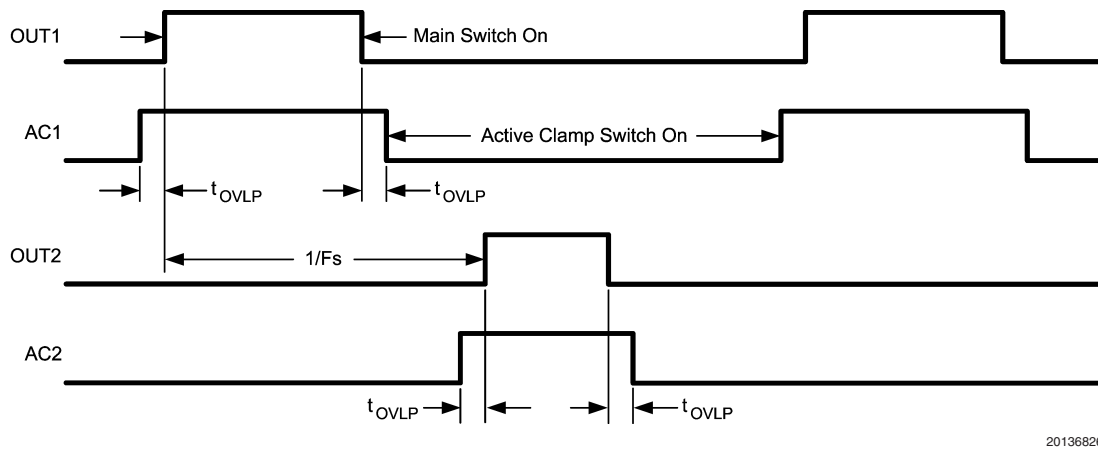


FIGURE 23. Output Overlap Timing

## Thermal Shutdown

The LM5034 should be operated so the junction temperature does not exceed 125°C. If a junction temperature transient reaches 165°C (typical), the Thermal Shutdown circuit activates the  $V_{CC}$  Disable and Drivers Off lines (see *Figure 18*). The  $V_{CC}$  regulator and the four output drivers are disabled,

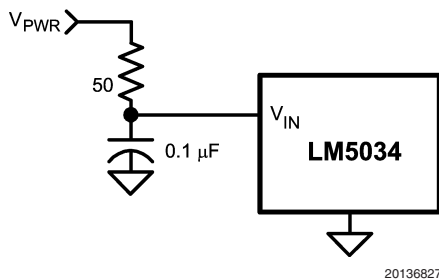
the SS1, SS2, and RES pins are grounded, and the soft-start current is set to 50  $\mu$ A. This puts the LM5034 in a low power state helping to prevent catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C), the  $V_{CC}$  regulator is enabled and a startup sequence is initiated (*Figure 3*).

## Applications Information

### VIN

The voltage applied to the VIN pin, normally the same as the system voltage applied to the power transformer's primary ( $V_{PWR}$ ), can vary in the range of 13 to 100V with transient capability to 105V. The current into VIN depends primarily on the output driver capacitive loads, the switching frequency, and any external loads on the VCC pins. If the power dissipation associated with the VIN current exceeds the package capability, an external voltage should be applied to the VCC pins (see *Figure 4* & *Figure 5*) to reduce power in the internal start-up regulator. It is recommended the circuit of *Figure 24* be used to suppress transients which may occur at the input supply, in particular where VIN is operated close to the maximum operating rating of the LM5034.

When all internal bias currents for the LM5034 and output driver currents are supplied through VIN and the internal  $V_{CC}$  regulator, the required input current ( $I_{IN}$ ) is shown in *Figure 4* & *Figure 5*. In most applications, upon turn-on,  $I_{IN}$  increases with  $V_{IN}$  as shown in *Figure 4* until the UVLO threshold is reached. After the outputs are enabled and the external VCC supply voltage is active, the current into VIN then drops to a nominal 120  $\mu$ A.

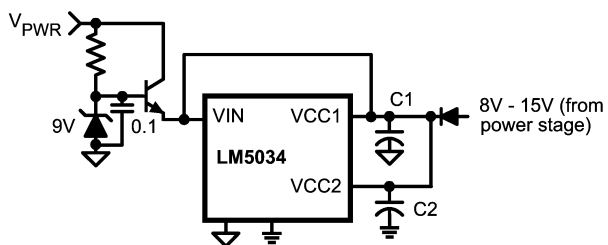


20136827

FIGURE 24. Input Transient Production

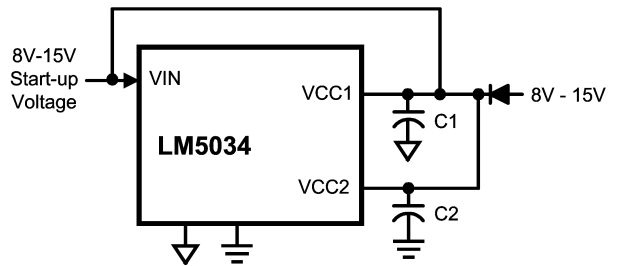
### FOR APPLICATIONS >100V

For applications where the system input voltage ( $V_{PWR}$ ) exceeds 100V, VIN can be powered from an external start-up regulator as shown in *Figure 25*, or from any other low voltage source as shown in *Figure 26*. Connecting VIN and the VCC together allows the LM5034 to be operated with VIN below 13V. The voltage at the VCC pins must not exceed 15V. The voltage source at the right side of *Figure 25* is typically derived from the power stage, and becomes active once the LM5034's outputs are active.



20136847

FIGURE 25. Start-up Regulator for  $V_{PWR} > 100V$



20136848

FIGURE 26. Bypassing the Internal Start-up Regulator

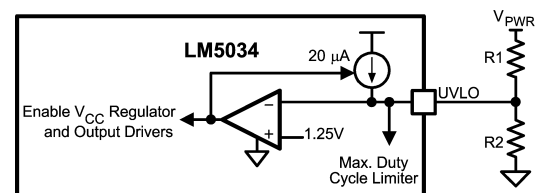
### UVLO

The under-voltage lockout threshold (UVLO) is internally set at 1.25V at the UVLO pin. With two external resistors as shown in *Figure 27*, the LM5034 is enabled when  $V_{PWR}$  exceeds the programmed threshold voltage. When  $V_{PWR}$  is above the threshold, the internal 20  $\mu$ A current source is enabled to raise the voltage at the UVLO pin, providing hysteresis. R1 and R2 are determined from the following equations:

$$R1 = V_{HYS} / 20 \mu A$$

$$R2 = \frac{1.25 \times R1}{V_{PWR} - 1.25}$$

where  $V_{HYS}$  is the desired UVLO hysteresis at  $V_{PWR}$ , and  $V_{PWR}$  in the second equation is the turn-on voltage. For example, if the LM5034 is to be enabled when  $V_{PWR}$  reaches 20V, and disabled when  $V_{PWR}$  is decreased to 17V, R1 calculates to 150 k $\Omega$ , and R2 calculates to 10 k $\Omega$ . The voltage at UVLO should not exceed 6V at any time.

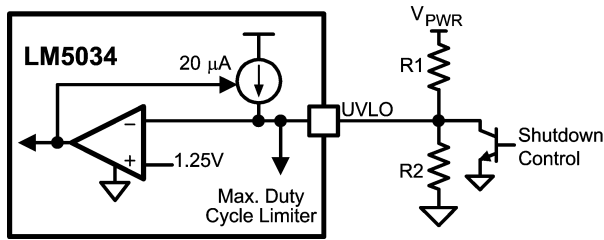


20136828

FIGURE 27. UVLO Circuit

The LM5034 can be remotely shutdown by taking the UVLO pin below 1.25V with an external open collector or open drain device, as shown in *Figure 28*. The outputs, and the  $V_{CC}$  regulator, are disabled, and the LM5034 enters a low power mode. To shut down one regulator without affecting the other, see the Soft-start section.

## Applications Information (Continued)



20136829

FIGURE 28. Shutdown Control

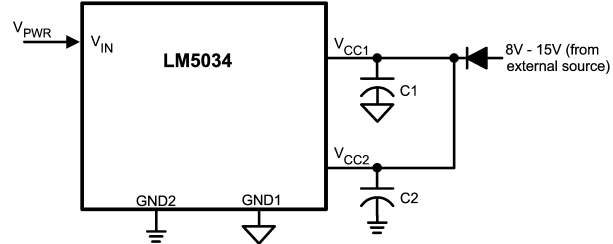
### VCC1, VCC2

The capacitors at each VCC pin provide not only regulator noise filtering and stability, but also prevents VCC from dropping to the lower under-voltage threshold level (UVT = 6.2V) when the output drivers source current surges to the external MOSFET gates. Additionally, the capacitors provide a necessary time delay during startup. The time delay allows the internal circuitry of the LM5034 and associated external circuitry to stabilize before V<sub>CC</sub> reaches the upper UVT threshold level (7.6V), at which time the outputs are enabled and the soft-start sequence begins. V<sub>CC</sub> is nominally regulated at 7.7V. The delay to the UVT level (Figure 3) is calculated from the following:

$$t_{VCC} = \frac{(C1 + C2) \times 7.6V}{I_{CC(Lim)}}$$

where C1 and C2 are the capacitors at VCC1 and VCC2, and I<sub>CC(Lim)</sub> is the V<sub>CC</sub> regulator's current limit. If the capacitors are 0.1 µF each, the nominal I<sub>CC(Lim)</sub> of 22 mA provides a delay of approximately 69 µs. The V<sub>CC</sub> capacitor values should range between 0.1 µF and 25 µF, and they should be the same value. Experimentation with the final design may be necessary to determine the optimum value for the V<sub>CC</sub> capacitors.

The average V<sub>CC</sub> regulator current required to drive the external MOSFETs is a function of the MOSFET gate capacitance and the switching frequency (see Figure 6). To ensure VCC does not droop below the lower UVT threshold, an external supply should be diode connected to both VCC pins to provide the required current, as shown in Figure 29. The applied V<sub>CC</sub> voltage must be between 8V and 15V. Providing the V<sub>CC</sub> voltage higher than the 7.7V regulation level with an external supply shuts off the internal regulator, reducing power dissipation within the IC. Internally there is a diode from the V<sub>CC</sub> regulator output to VIN. Typically the applied voltage is derived from an auxiliary winding on the power transformer, or on the output inductor.



20136830

FIGURE 29. External Power to V<sub>CC</sub>

### OSCILLATOR, SYNC INPUT

The oscillator frequency is generally selected in conjunction with the system magnetic components, and any other aspects of the system which may be affected by the frequency. The R<sub>T</sub> resistor at the RT/SYNC pin sets the frequency according to Equation 1. Each output (OUT1 and OUT2) switches at one-half the oscillator frequency. If the required frequency tolerance is critical in a particular application, the tolerance of the external resistor and the frequency tolerance specified in the Electrical Characteristics table must be considered when selecting the R<sub>T</sub> resistor.

If the LM5034 is to be synchronized to an external clock, that signal must be coupled into the RT/SYNC pin through a 100 pF capacitor. The external synchronizing frequency must be at least 4% higher than the free running frequency set by the R<sub>T</sub> resistor and no higher than twice the free running frequency. The RT/SYNC pin voltage is nominally regulated at 2.0V and the external pulse amplitude should lift the pin to between 3.8V and 5.0V on the low-to-high transition. The synchronization pulse width should be between 15 and 150 ns. The R<sub>T</sub> resistor is always required, whether the oscillator is free running or externally synchronized.

### VOLTAGE FEEDBACK, COMP1, COMP2

Each COMP pin is designed to accept a voltage feedback signal from the respective regulated output via an error amplifier and (typically) an opto-coupler. A typical configuration is shown in Figure 19. V<sub>OUT</sub> is compared to a reference by the error amplifier which has an appropriate frequency compensation network. The amplifier's output drives the opto-coupler, which in turn drives the COMP pin.

When the LM5034's two controller channels are configured to provide a single high current output, COMP1 and COMP2 are typically connected together, and to the feedback signal from the optocoupler.

### CURRENT SENSE, CS1, CS2

Each CS pin receives an input signal representative of its transformer's primary current, either from a current sense transformer or from a resistor in series with the source of the primary switch, as shown in Figure 30 and Figure 31. In both cases the sensed current creates a ramping voltage across R1, and the R<sub>F</sub>/C<sub>F</sub> filter suppresses noise and transients. R1, R<sub>F</sub> and C<sub>F</sub> should be as physically close to the LM5034 as possible, and the ground connection from the current sense transformer, or R1, should be a dedicated track to the appropriate GND pin. The current sense components must provide >0.5V at the CS pin when an over-current condition exists.

## Applications Information (Continued)

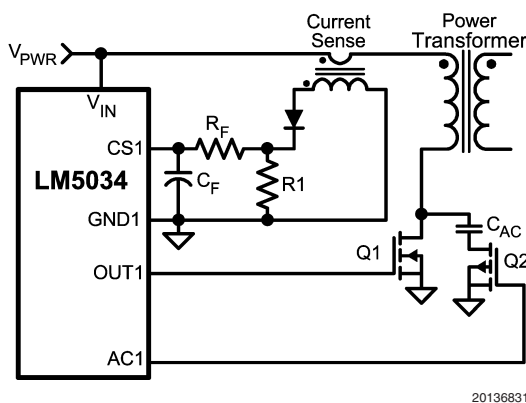


FIGURE 30. Current Sense Using a Current Sense Transformer

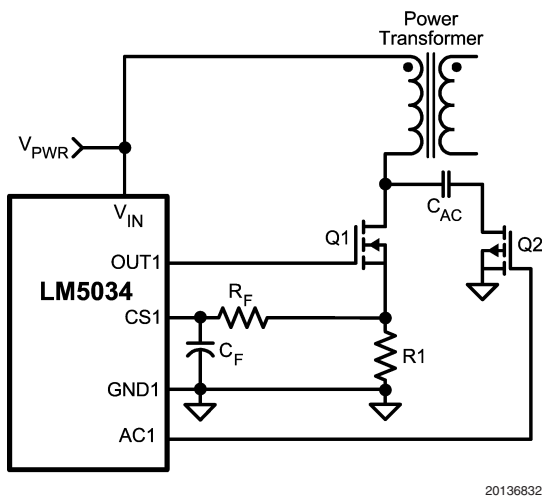


FIGURE 31. Current Sense Using a Source Sense Resistor (R1)

### HICCUP MODE CURRENT LIMIT RESTART

This circuit's operation is described in the Functional Description. Also see *Figure 20* and *Figure 21*. In the case of continuous current limit detection at both CS pins, the time required to reach the 2.55V RES pin threshold is:

$$t1 = \frac{C_{RES} \times 2.55V}{20 \mu A} = 1.275 \times 10^5 \times C_{RES}$$

For example, if  $C_{RES} = 0.1 \mu F$  the time  $t1$  in *Figure 21* is approximately 12.75 ms.

In the case of continuous current limit detection at one CS pin only, the time to reach the 2.55V threshold is increased by a factor of four, or:

$$t1 = 5.1 \times 10^5 \times C_{RES}$$

The time  $t2$  in *Figure 21* is set by the capacitor at each SS pin and the internal  $1 \mu A$  current source, and is equal to:

$$t2 = \frac{C_{SS} \times 1.5V}{1 \mu A} = 1.5 \times 10^6 \times C_{SS}$$

If  $C_{SS} = 0.1 \mu F$   $t2$  is  $\approx 150$  ms. Time  $t3$  is set by the internal  $50 \mu A$  current source, and is equal to:

$$t3 = \frac{C_{SS} \times 3.5V}{50 \mu A} = 7 \times 10^4 \times C_{SS}$$

The time  $t2$  provides a periodic dwell time for the converter in the event of a sustained overload or short circuit. This results in lower average input current and lower power dissipated within the circuit components. It is recommended that the ratio of  $t2/(t1 + t3)$  be in the range of 5 to 10 to make good use of this feature.

If the application requires no delay from the first detection of a current limit condition, so that  $t1$  is effectively zero, the RES pin can be left open (no external capacitor). If it is desired to disable the hiccup mode current limit operation then the RES pin should be connected to ground.

### SOFT-START

The capacitors at SS1 and SS2 determine the time required for each regulator's output duty cycle to increase from zero to its final value for regulation. The minimum acceptable time is dependent on the output capacitance and the response of each feedback loop to the COMP pin. If the Soft-start time is too quick, the output could significantly overshoot its intended voltage before the feedback loop has a chance to regulate the PWM controller.

After power is applied and  $V_{CC}$  has passed its upper UVT threshold ( $\approx 7.6V$ ), the voltage at each SS pin ramps up as its external capacitor is charged up by an internal  $50 \mu A$  current source (see *Figure 3*). The voltage at the COMP pins follow the SS pins. When both have reached  $\approx 1.5V$ , PWM pulses appear at the driver outputs with very low duty cycle. The voltage at each SS pin continues to increase to  $\approx 5.0V$ . The voltage at each COMP pin, and the PWM duty cycle, increase to the value required for regulation as determined by its feedback loop. The time  $t1$  in *Figure 3* is calculated from:

$$t1 = \frac{C_{SS} \times 1.5V}{50 \mu A} = 3 \times 10^4 \times C_{SS}$$

With a  $0.1 \mu F$  capacitor at SS,  $t1$  is  $\approx 3$  ms.

If the Hiccup Mode Current Limit Restart circuit activates due to repeated current limit detections at CS1 and/or CS2, both SS1 and SS2 are internally grounded (see the section on Hiccup Mode Current Limit Restart). After a short propagation delay, the SS pins are released and the external SS pin capacitors are charged by internal  $1 \mu A$  current sources. The slow charge rate provides a rest or dwell time for the converter power stage ( $t2$  in *Figure 21*), reducing the average input current and component temperature rise while in an overload condition. When the voltage at the SS and COMP pins reach  $\approx 1.5V$ , the first pulse out of either PWM comparator switches the internal SS pin current sources to  $50 \mu A$ . The voltages at the SS and COMP pins then increase more quickly, increasing the duty cycle at the output drivers. The rest time  $t2$  is the time required for SS to reach 1.5V:



## Applications Information (Continued)

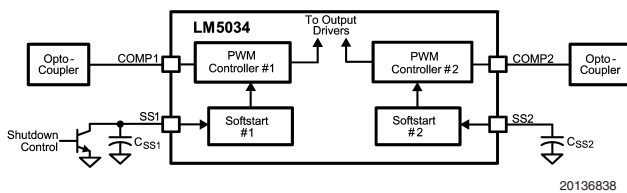
$$t_2 = \frac{C_{SS} \times 1.5V}{1 \mu A} = 1.5 \times 10^6 \times C_{SS}$$

With a 0.1  $\mu$ F capacitor at SS,  $t_2$  is  $\approx 150$  ms.

Experimentation with the startup sequence and over-current restart condition is usually necessary to determine the appropriate value for the SS capacitors.

To shutdown one regulator without affecting the other, ground the appropriate SS pin with an open collector or open drain device as shown in *Figure 32*. The SS pin forces the COMP pin to ground which reduces the PWM duty cycle to zero for that regulator. Releasing the SS pin allows normal operation to resume.

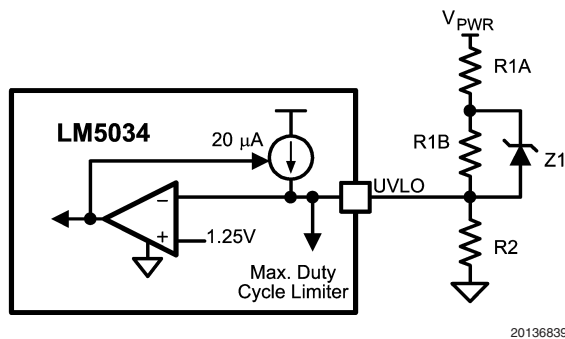
When the LM5034's two controller channels are configured to provide a single high current output, SS1 and SS2 are typically connected together, requiring a single capacitor for the two pins.



**FIGURE 32. Shutting Down One Regulator Channel**

### LINE VOLTAGE DEPENDENT MAXIMUM DUTY CYCLE

As  $V_{PWR}$  increases and the voltage at UVLO follows, the maximum allowed duty cycle decreases according to the graph of *Figure 11*. Using values from the example above ( $R_1 = 150$  k $\Omega$ ,  $R_2 = 10$  k $\Omega$  in *Figure 27*), the maximum duty cycle varies as shown in *Figure 12*. If it is desired to increase the slope of the ramp in *Figure 12*, *Figure 33* shows a suggested configuration. After the LM5034 is enabled, Z1 clamps the voltage across R1B, and UVLO increases with  $V_{PWR}$  at a rate determined by the ratio  $R_2/(R_1A + R_2)$ .



**FIGURE 33. Altering the Slope of Duty Cycle vs.  $V_{PWR}$**

### USER DEFINED MAX DUTY CYCLE

The maximum allowed duty cycle at OUT1 and OUT2 can be set with a resistor from DCL to GND1. See *Figure 10* and Equation 2. The default maximum duty cycle (80%) determined by the internal clock signals can be selected by setting  $R_{DCL} = R_T$ . The oscillator frequency setting resistor ( $R_T$ )

must be determined before  $R_{DCL}$  is selected. The DCL pin should not be left open.

### PRINTED CIRCUIT (PC) BOARD LAYOUT

The LM5034 Current Sense and PWM comparators are very fast, and respond to short duration noise pulses. The components at the CS, COMP, SS, DCL, UVLO, OVLP and the RT/SYNC pins should be as physically close as possible to the IC, thereby minimizing noise pickup in the PC board tracks.

Layout considerations are critical for the current sense filter. If current sense transformers are used, both leads of each transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of each transformer should be connected via a dedicated PC board track to its appropriate GND pin, rather than through the ground plane.

If the current sense circuits employ sense resistors in the drive transistor sources, low inductance resistors should be used. In this case, all the noise sensitive low current ground tracks should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point). The outputs of the LM5034 should have short direct paths to the power MOSFETs in order to minimize inductance in the PC board traces.

The two ground pins (GND1, GND2) must be connected together with a short direct connection to avoid jitter due to relative ground bounce in the operation of the two regulators.

If the internal dissipation of the LM5034 produces high junction temperatures during normal operation, the use of wide PC board traces can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

### APPLICATION CIRCUIT EXAMPLE

*Figure 38* shows an example of an LM5034 controlled 200W dual interleaved regulator which provides two independent regulated outputs or a single high current output. The input voltage range ( $V_{PWR}$ ) is 36V to 78V, and the output voltages are 3.3V and 2.5V in the dual output mode, or 3.3V in the single output mode. The output current capability is 30A from each output or 60A in the single output mode. Current sense transformers T1 and T2 provide information to the CS2 and CS1 pins for the current mode control, and error amplifiers U3 and U4 provide voltage feedback to COMP2 and COMP1 via optocoupler U2. Synchronous rectifiers Q5-Q12 minimize rectification losses in the secondaries. An auxiliary winding on inductor L2 provides power to the LM5034 VCC pins when the outputs are enabled. The UVLO levels are  $\approx 34.3$ V for increasing  $V_{PWR}$ , and  $\approx 32.3$ V for decreasing  $V_{PWR}$ . The circuit can be shut down by forcing the ON/OFF input (J2) below 1.25V. An external synchronizing frequency can be applied to the SYNC input (J3). Each regulator output is current limited at  $\approx 31.5$ A.

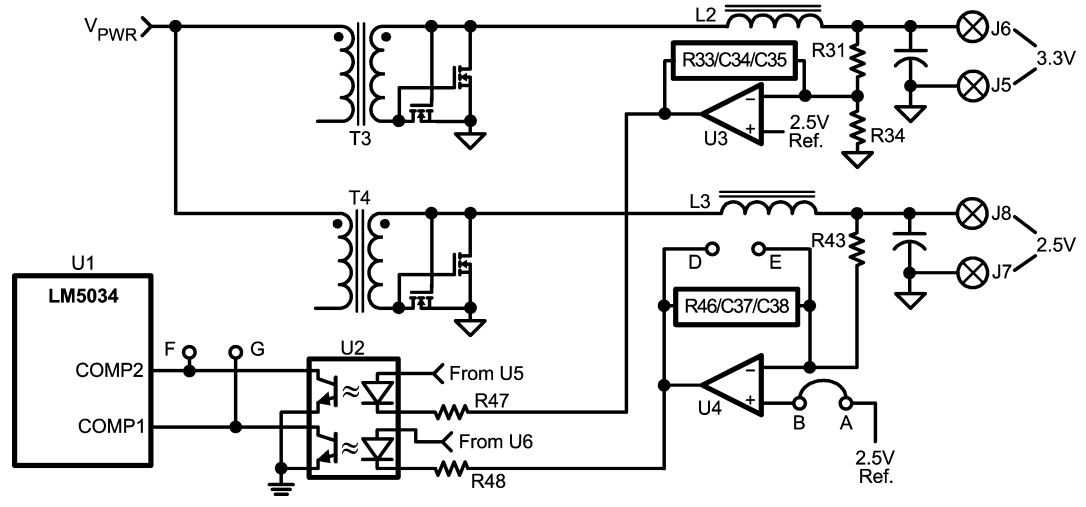
To configure the circuit for two independent outputs, jumper A-B is installed, and the other jumpers connections (C through G) are left open. U5 and U6 are the references for the two error amplifiers which control the LM5034's COMP pins via the optocouplers. See *Figure 34*.

To configure the circuit for a single high current output, jumpers B-C, D-E, and F-G are installed and A-B is removed. Output terminals J8 and J6 are connected together at the load, as well as the ground terminals J5 and J7. In this mode U4 is a follower to error amplifier U3, and the optocoupler

**Applications Information** (Continued)

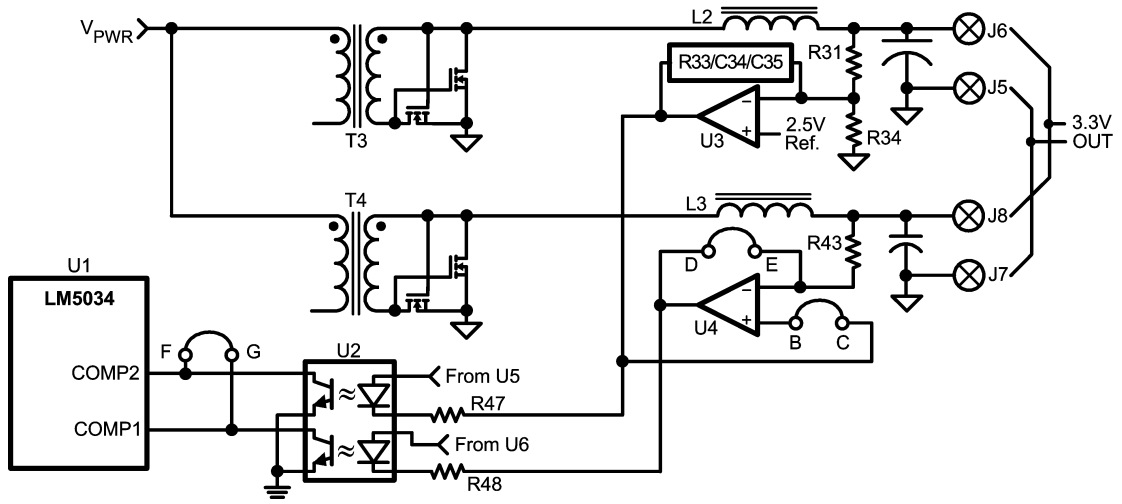
outputs are connected together to provide the same voltage

to COMP1 and COMP2. See *Figure 35*. Efficiency measurements for this circuit are shown in *Figure 36* and *Figure 37*.



20136840

**FIGURE 34. Circuit Configuration for Independent Outputs**

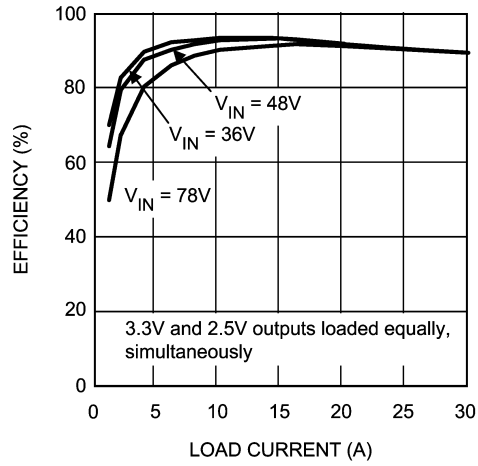


20136841

**FIGURE 35. Circuit Configuration for Single High Current Output**

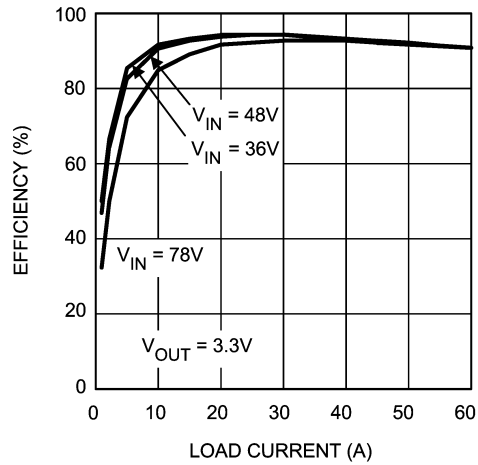


Applications Information (Continued)



20136842

FIGURE 36. Total Board Efficiency, Independent Outputs



20136843

FIGURE 37. Efficiency, Single Output



## Evaluation Board Schematic (Continued)

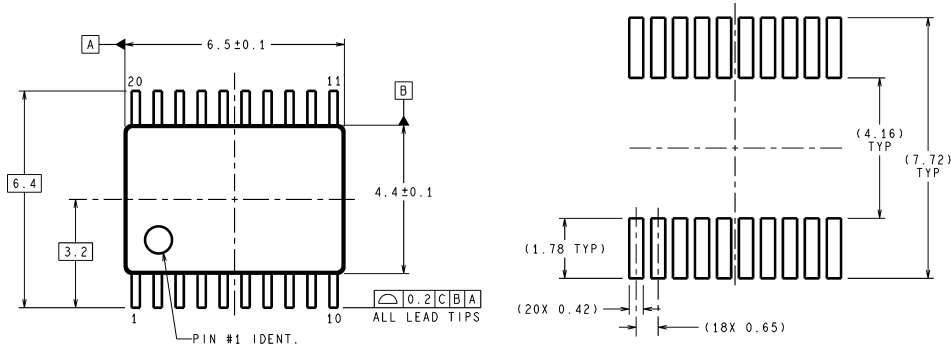
### Bill of Materials (Circuit of Figure 38)

Item	Description	Package	Value
C1-4	Capacitor	1812	2.2 $\mu$ F, 100V
C5, 50	Capacitor	1812	0.01 $\mu$ F, 1000V
C6, 17, 19	Capacitor	1206	0.1 $\mu$ F, 250V
C7, 10, 11, 35, 38	Capacitor	0805	0.01 $\mu$ F, 50V
C8, 16, 18, 24, 26, 27, 39, 40, 42	Capacitor	0805	0.1 $\mu$ F, 50V
C9	Capacitor	0805	100 pF
C12, 13	Capacitor	1210	10 $\mu$ F, 16V
C14, 15	Capacitor	0805	0.33 $\mu$ F
C20, 21	Capacitor	0805	1000 pF
C22, 23, 34, 37, 43, 44	Capacitor	0805	470 pF
C25, 41	Capacitor	0805	0.022 $\mu$ F
C28, 29, 45, 46	Capacitor	3018	330 $\mu$ F, 6.3V Tantalum
C30-32, 47-49	Capacitor	1812	47 $\mu$ F
C33, 36, 51, 52	Capacitor	0805	1500 pF
D1-D11	Dual Diode	SOT-23	75V, 200 mA
D12, 13	Dual Diode	SOT-23	100V, 200 mA
D14, 15	Schottky diode	SOD-323	30V, 100 mA
L1	Inductor, TDK SLF12575	12.5 x 12.5	5.6 $\mu$ H, 6A
L2, 3	Inductor w/ aux out, Coilcraft B0358-C	0.92 x 0.81	2 $\mu$ H, 30A
Q1, 3	N-MOSFET, Vishay Si7846DP	SO8	150V, 4A
Q2, 4	P-MOSFET, IRF6217	SO8	150V, 0.7A
Q5-12	N-MOSFET, Vishay Si7866DP	SO8	20V, 25A
R1	Resistor	1206	10 $\Omega$ , 1/8W
R2	Resistor	1206	49.9 $\Omega$
R3, 8	Resistor	0805	43.2k $\Omega$
R4	Resistor	0805	100k $\Omega$
R5	Resistor	0805	3.74k $\Omega$
R6, 10, 11, 25, 26, 32, 37, 38, 44	Resistor	0805	1.0k $\Omega$
R7	Resistor	0805	32.4k $\Omega$
R9, 45	Resistor	0805	Open
R12, 13	Resistor	0805	10k $\Omega$
R14, 17	Resistor	0805	1.5k $\Omega$
R15, 18	Resistor	0805	8.2 $\Omega$
R16, 19	Resistor	0805	301 $\Omega$
R20, 22, 49, 51	Resistor	2512	10 $\Omega$ , 1W
R21, 23, 24, 50, 52, 53	Resistor	0805	5.62 $\Omega$
R27, 39	Resistor	0805	49.9 $\Omega$
R28, 40	Resistor	0805	12.7k $\Omega$
R29, 41	Resistor	0805	20k $\Omega$
R30, 35, 36, 42	Resistor	0805	10 $\Omega$
R31, 43	Resistor	0805	24.9k $\Omega$
R33, 46	Resistor	0805	30.1k $\Omega$
R34	Resistor	0805	76.8k $\Omega$
R47, 48	Resistor	0805	1.21k $\Omega$

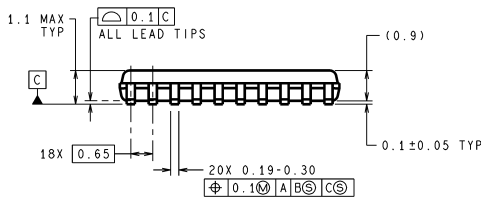
**Evaluation Board Schematic** (Continued)**Bill of Materials (Circuit of Figure 38)** (Continued)

Item	Description	Package	Value
T1, 2	Transformer, Pulse Eng. P8208T	0.33 x 0.28	100:1, 6A
T3, 4	Transformer, Coilcraft B0357-B	0.92 x 0.81	12:2, 30A
U1	PWM dual controller	TSSOP-20	LM5034MTC
U2	Dual Optocoupler	SO8	MOCD207M
U3, 4	Op Amp	SOT23-5	LM8261
U5, 6	Reference	SOT23	LM4040-4.1V

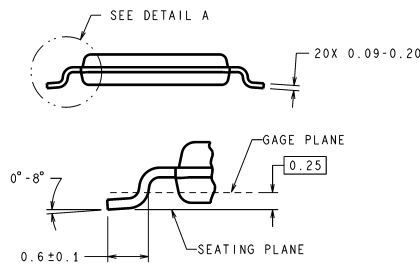
**Physical Dimensions** inches (millimeters)  
unless otherwise noted



**LAND PATTERN RECOMENDATION**



**DIMENSIONS ARE IN MILLIMETERS**



**DETAIL A**  
TYPICAL

MTC20 (Rev E)

**Molded TSSOP-20**  
**NS Package Number MTC20**

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at [www.national.com](http://www.national.com).

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**BANNED SUBSTANCE COMPLIANCE**

National Semiconductor manufactures products and uses packing materials that meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.



**National Semiconductor**  
**Americas Customer**  
**Support Center**  
Email: [new.feedback@nsc.com](mailto:new.feedback@nsc.com)  
Tel: 1-800-272-9959

**National Semiconductor**  
**Europe Customer Support Center**  
Fax: +49 (0) 180-530 85 86  
Email: [europe.support@nsc.com](mailto:europe.support@nsc.com)  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +44 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor**  
**Asia Pacific Customer**  
**Support Center**  
Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)

**National Semiconductor**  
**Japan Customer Support Center**  
Fax: 81-3-5639-7507  
Email: [jpn.feedback@nsc.com](mailto:jpn.feedback@nsc.com)  
Tel: 81-3-5639-7560