



74ACT74

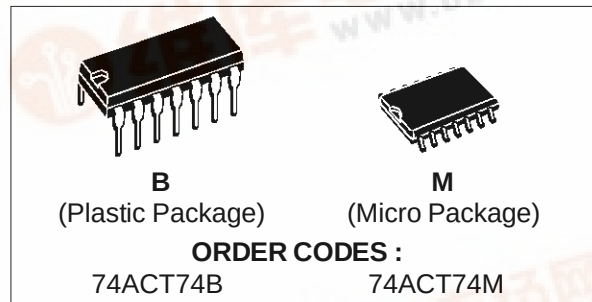
DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED:
 $f_{MAX} = 250 \text{ MHz (TYP.)}$ at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu A \text{ (MAX.)}$ at $T_A = 25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS
 $V_{IH} = 2V \text{ (MIN.)}$, $V_{IL} = 0.8V \text{ (MAX.)}$
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 4.5V \text{ to } 5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 74
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The ACT74 is an advanced high-speed CMOS OCTAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of



the clock pulse.

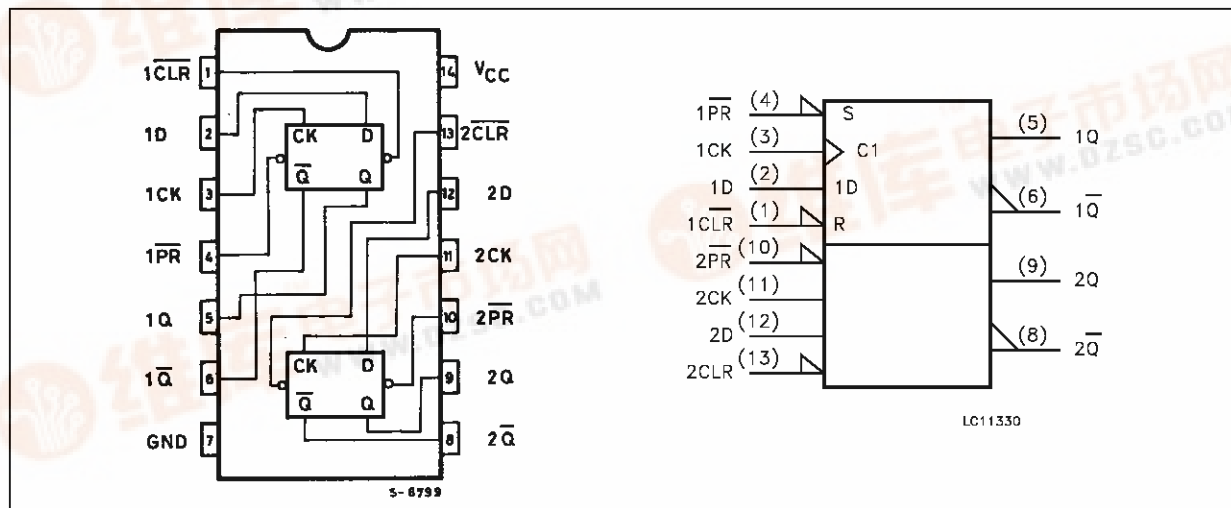
CLEAR and PRESET are independent of the clock and accomplished by a low setting on the appropriate input.

It is ideal for low power applications maintaining high speed operation similar to equivalent Bipolar Schottky TTL.

The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.

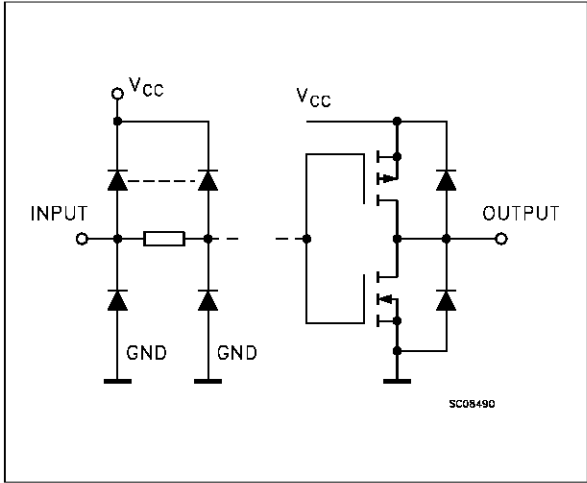
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



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INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

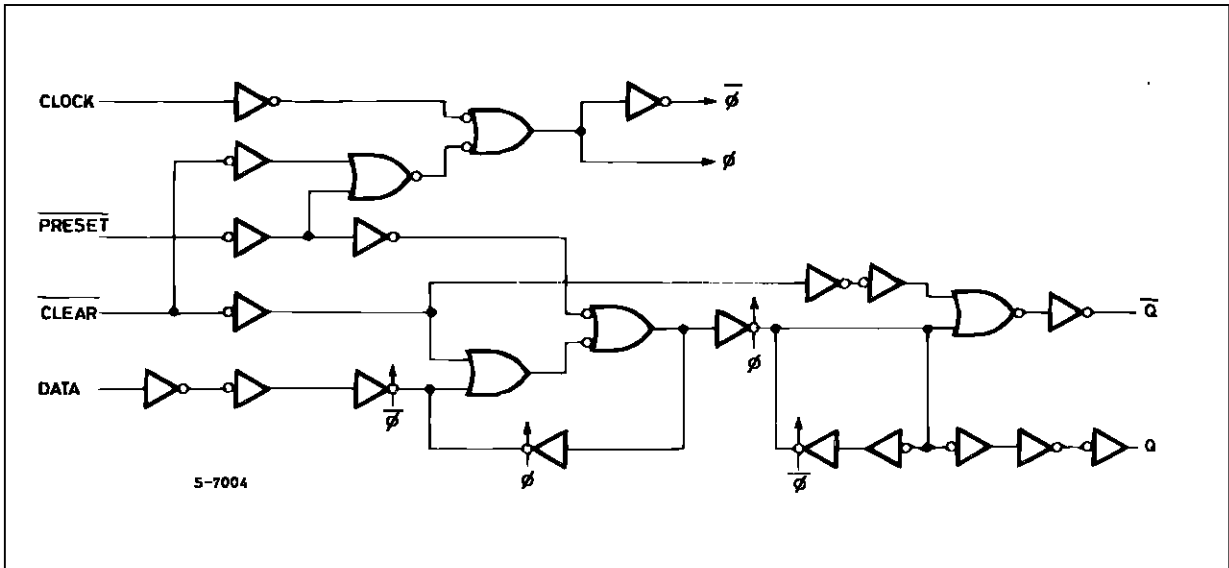
PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{1CLR}$, $\overline{2CLR}$	Asynchronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW-to-HIGH, Edge-Triggered)
4, 10	$\overline{1PR}$, $\overline{2PR}$	Asynchronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	$\overline{1Q}$, $\overline{2Q}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	VCC	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L		L	H	
H	H	H		H	L	
H	H	X		Q_n	$\overline{Q}_n$	NO CHANGE

X: Don't Care

LOGIC DIAGRAMS



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 200	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature (10 sec)	300	$^{\circ}\text{C}$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature:	-40 to +85	$^{\circ}\text{C}$
dt/dv	Input Rise and Fall Time $V_{CC} = 4.5$ to 5.5V (note 1)	8	ns/V

1) V_{IN} from 0.8 V to 2.0 V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C			
				Min.	Typ.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} - 0.1 V	2.0	1.5		2.0		V	
		5.5		2.0	1.5		2.0			
V _{IL}	Low Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} - 0.1 V		1.5	0.8		0.8	V	
		5.5			1.5	0.8		0.8		
V _{OH}	High Level Output Voltage	4.5	V _I ^(*) = V _{IH} or V _{IL}	I _O =-50 μA	4.4	4.49		4.4	V	
		5.5		I _O =-50 μA	5.4	5.49		5.4		
		4.5		I _O =-24 mA	3.86			3.76		
		5.5		I _O =-24 mA	4.86			4.76		
V _{OL}	Low Level Output Voltage	4.5	V _I ^(*) = V _{IH} or V _{IL}	I _O =50 μA		0.001	0.1	0.1	V	
		5.5		I _O =50 mA		0.001	0.1	0.1		
		4.5		I _O =24 mA			0.36	0.44		
		5.5		I _O =24 mA			0.36	0.44		
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND			±0.1		±1	μA	
I _{CC} T	Max I _{CC} /Input	5.5	V _I = V _{CC} -2.1 V		0.6			1.5	mA	
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40	μA	
I _{OLD}	Dynamic Output Current (note 1, 2)	5.5	V _{OLD} = 1.65 V max					75	mA	
I _{OHD}			V _{OHD} = 3.85 V min					-75	mA	

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50 Ω.

(*) All outputs loaded.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 3 \text{ ns}$)

Symbol	Parameter	Test Condition		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time CK to Q	5.0 ^(*)			5.0	10.0		11.0	ns
t _{PLH} t _{PHL}	Propagation Delay Time PR or CLR to Q or $\overline{Q}$	5.0 ^(*)			5.0	10.0		11.0	ns
t _w	CK Pulse Width, HIGH or LOW	5.0 ^(*)			1.5	5.0		6.0	ns
t _s	Setup Time Q to CK HIGH or LOW	5.0 ^(*)			0.5	3.0		3.5	ns
t _h	Hold Time Q to CK HIGH or LOW	5.0 ^(*)			-0.5	1.0		1.0	ns
t _{rem}	Removal Time $\overline{PR}$ or CLR to CK	5.0 ^(*)			-0.7	1.0		1.0	ns
f _{MAX}	Maximim Clock Frequency	5.0 ^(*)		100	250		85		MHz

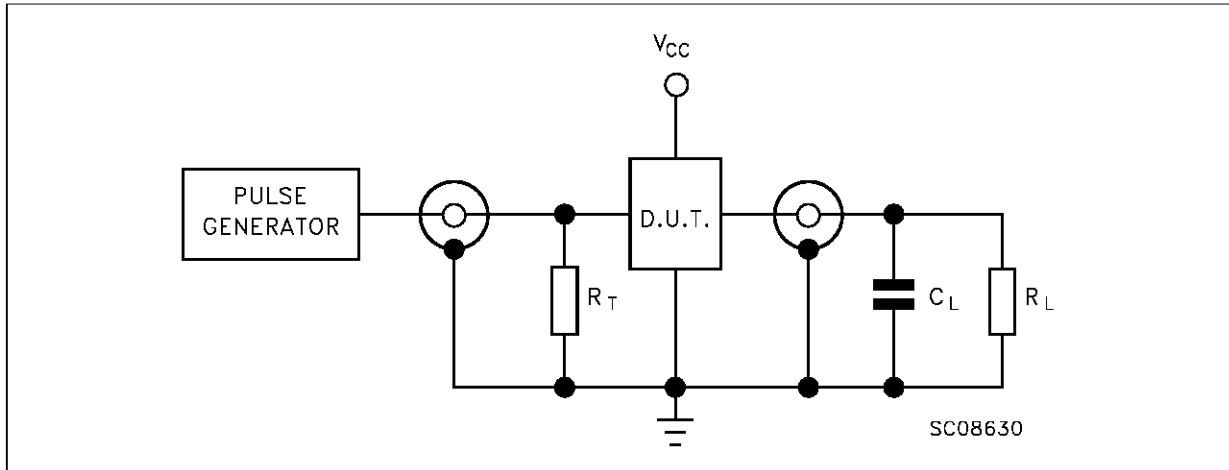
(*) Voltage range is $5V \pm 0.5V$ **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance	5.0			4				pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0			43				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/n$ (per circuit)

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TEST CIRCUIT

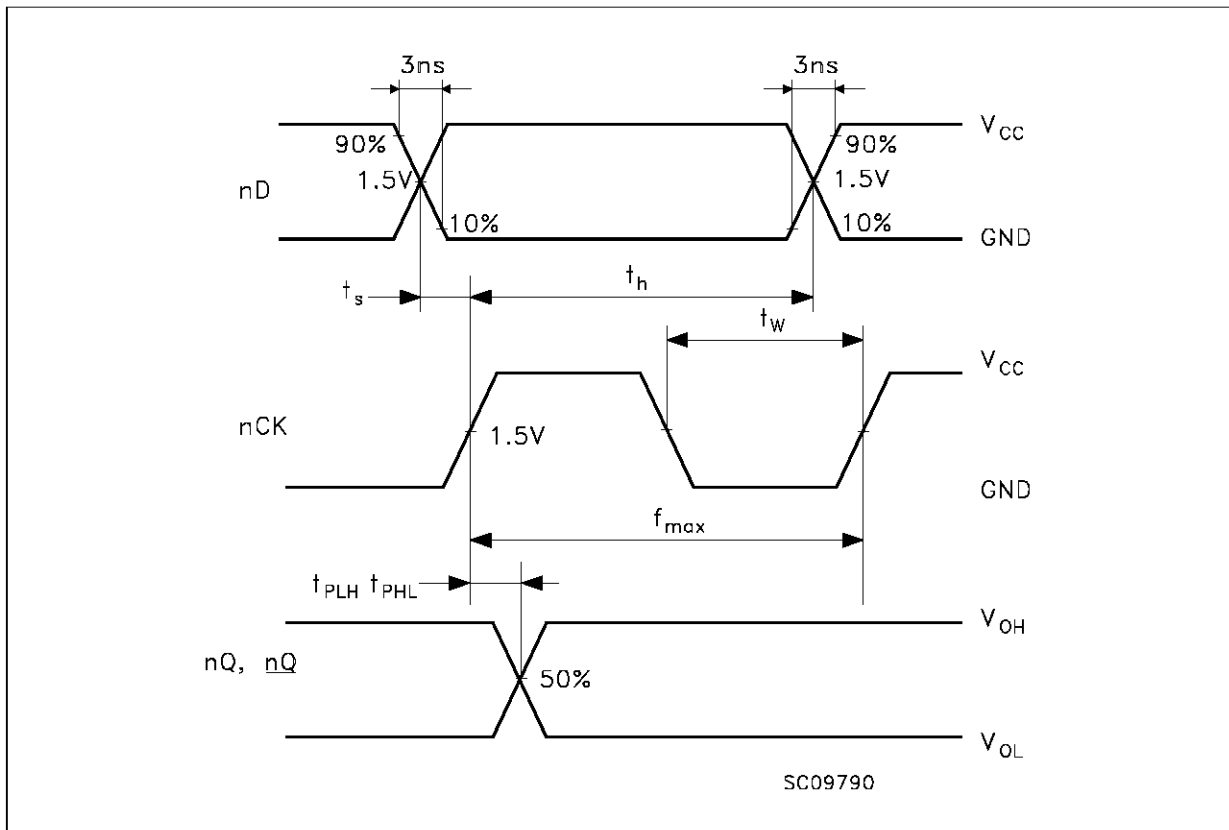


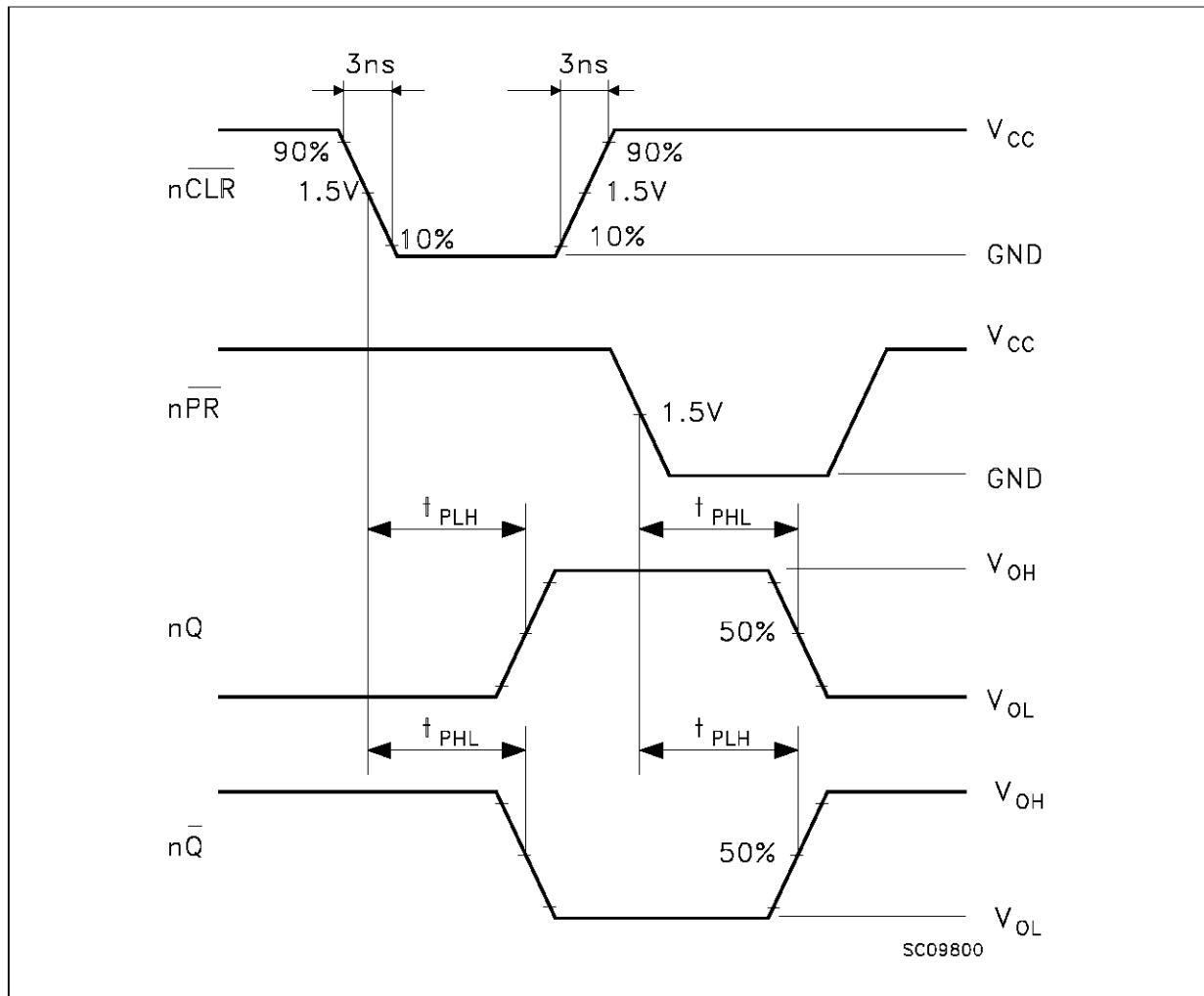
$C_L = 50$ pF or equivalent (includes jig and probe capacitance)

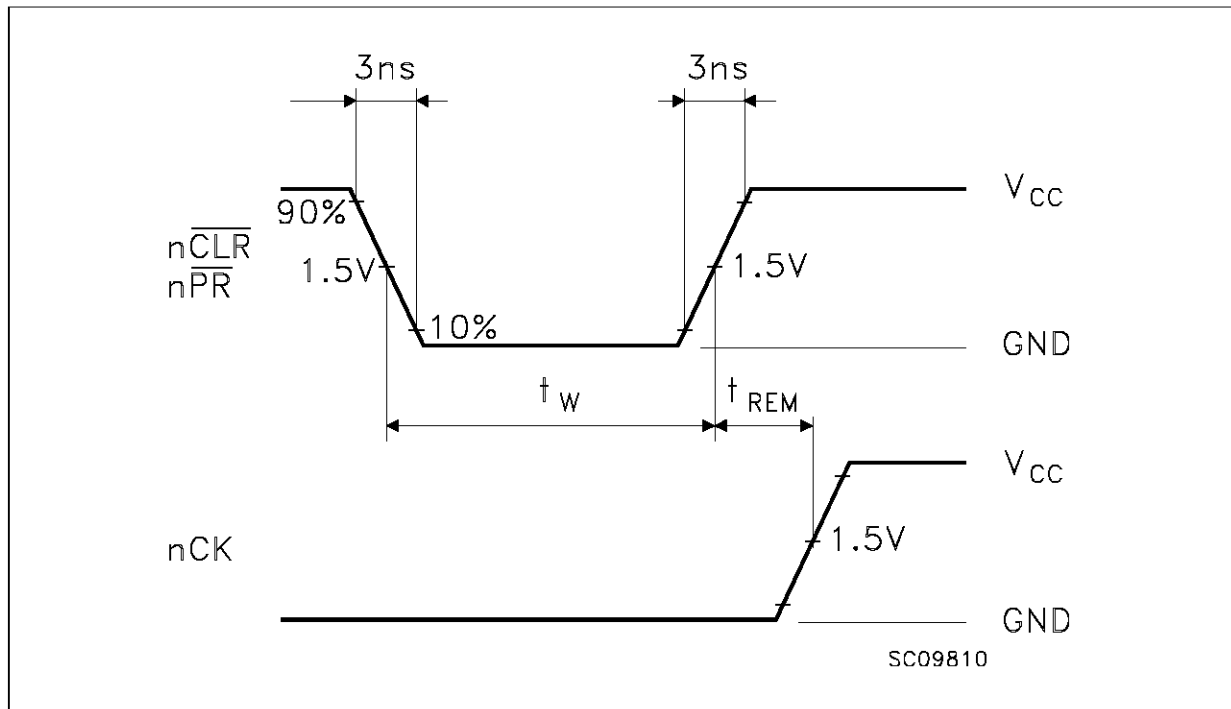
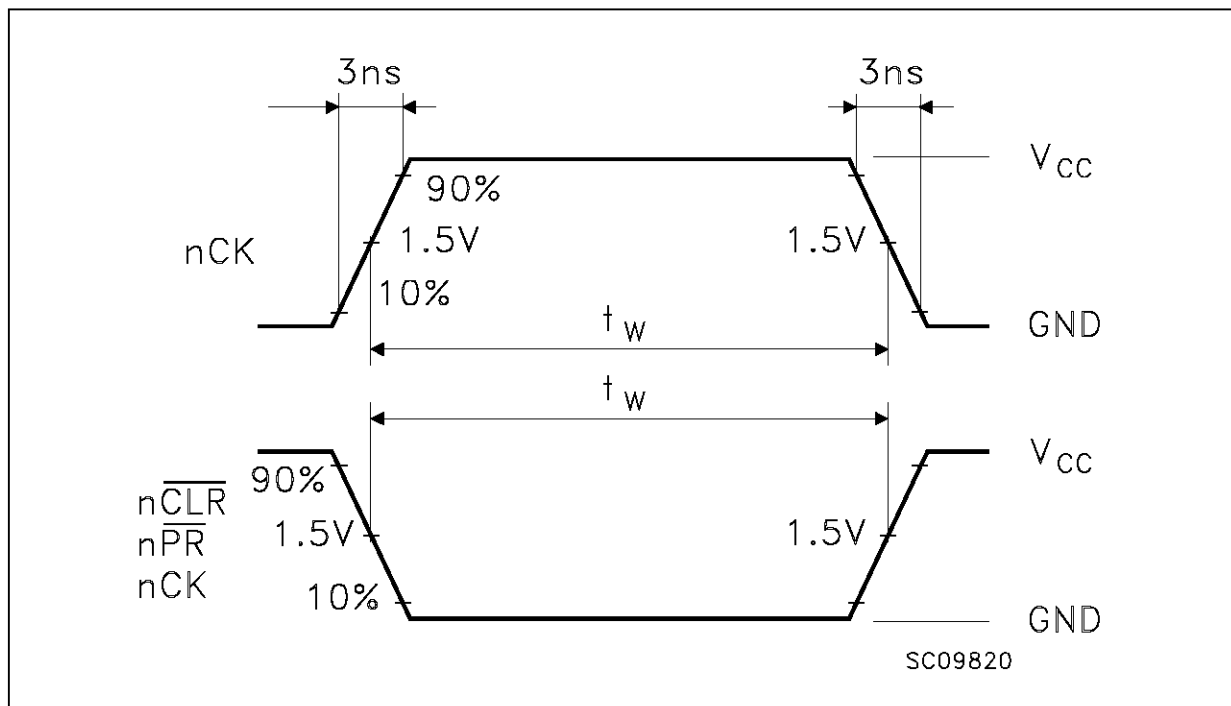
$R_L = R_1 = 500\Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES ($f=1$ MHz; 50% duty cycle)

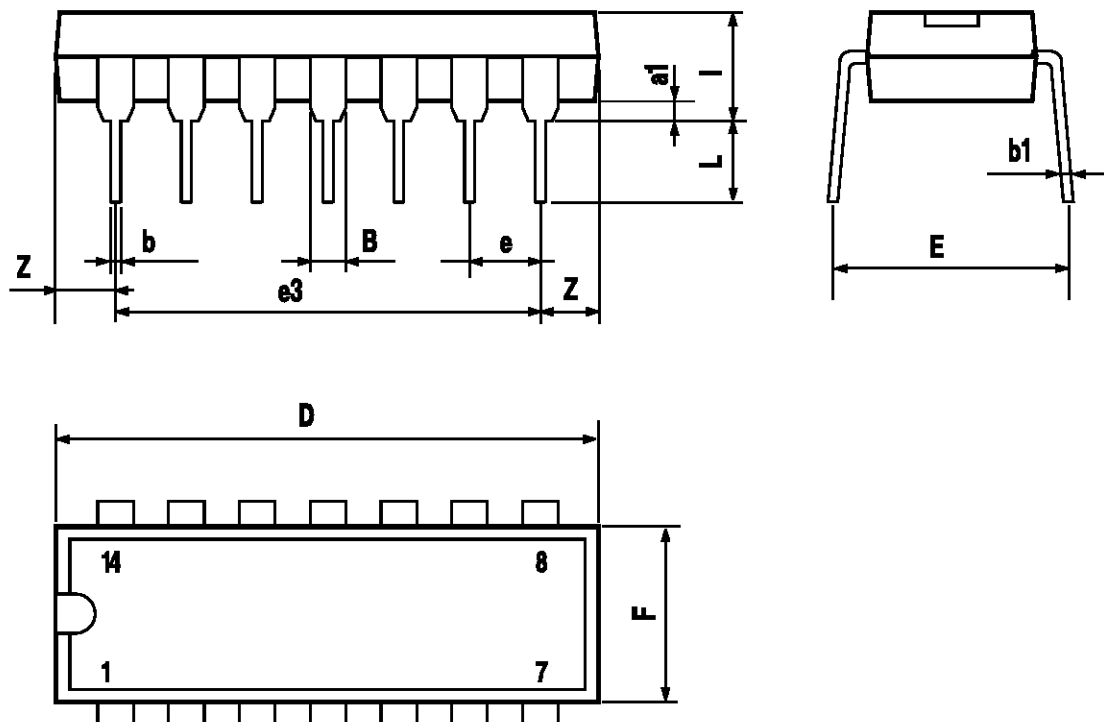


WAVEFORM 2: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)

WAVEFORM 3: RECOVERY TIMES ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 3: PULSE WIDTH**

Plastic DIP14 MECHANICAL DATA

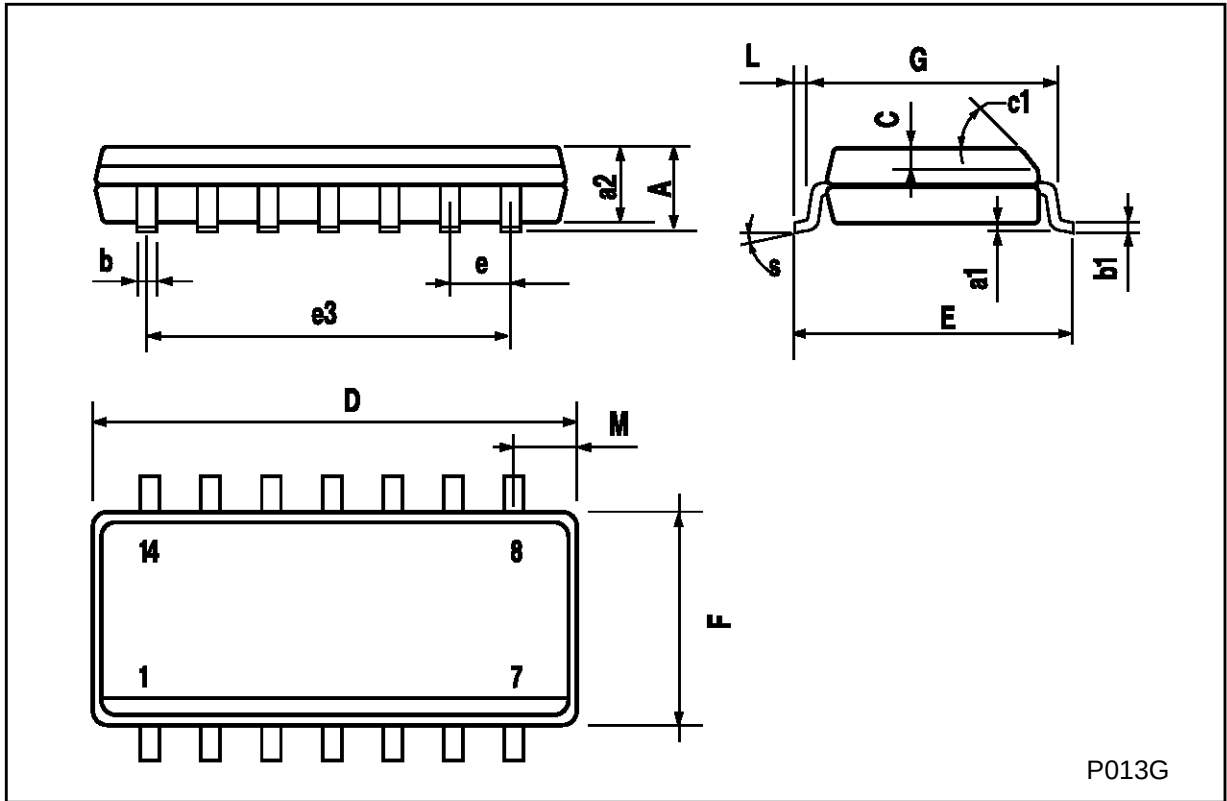
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

SO14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



P013G

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