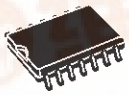
74LCX74

LOW VOLTAGE CMOS DUAL D-TYPE FLIP FLOP WITH 5V TOLERANT INPUTS

- 5V TOLERANT INPUTS
- HIGH SPEED:
  f_{MAX} = 150 MHz (MAX.) at V_{CC} = 3V
- POWER-DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24 mA (MIN)
- PCI BUS LEVELS GUARANTEED AT 24mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2.0V to 3.6V (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 74
- LATCH-UP PERFORMANCE EXCEEDS 500mA
- ESD PERFORMANCE:
  HBM >2000V; MM > 200V



M
(Micro Package)

T
(TSSOP Package)

ORDER CODES :

74LCX74M 74LCX74T

DESCRIPTION

The LCX74 is a low voltage CMOS DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for inputs.

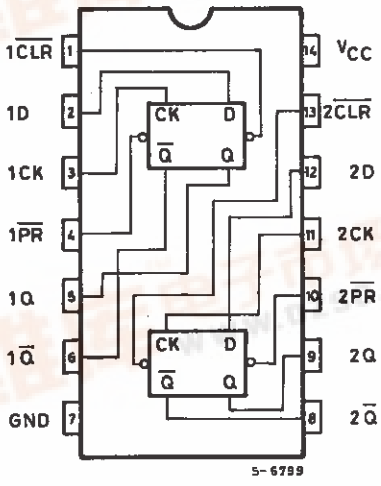
A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse.

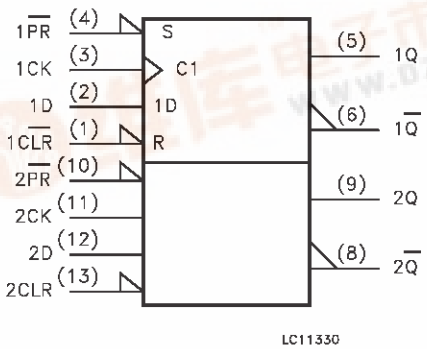
CLEAR and PRESET are independent of the clock and accomplished by a low setting on the appropriate input.

It has same speed performance at 3.3V than 5V, AC/ACT family, combined with a lower power consumption.

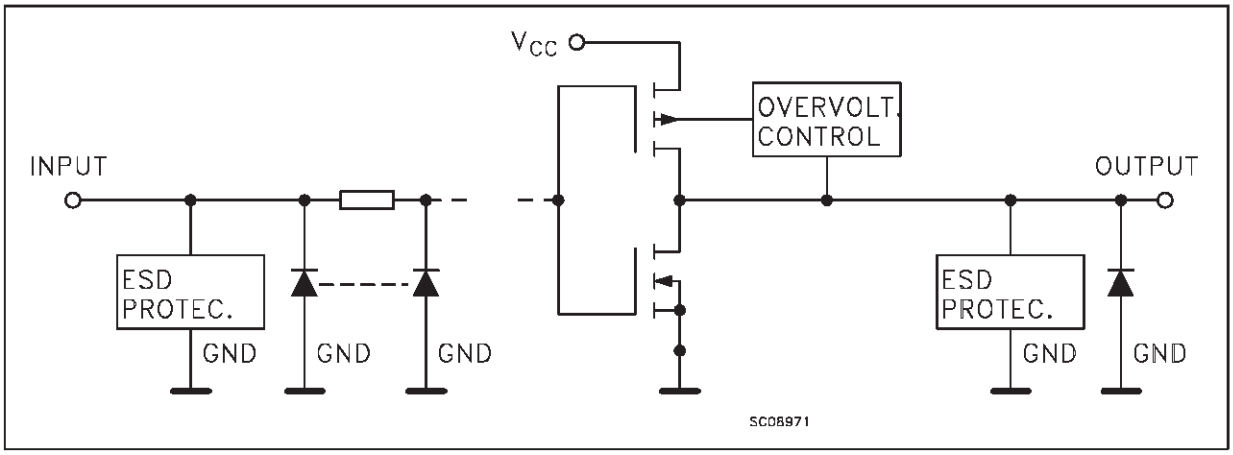
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

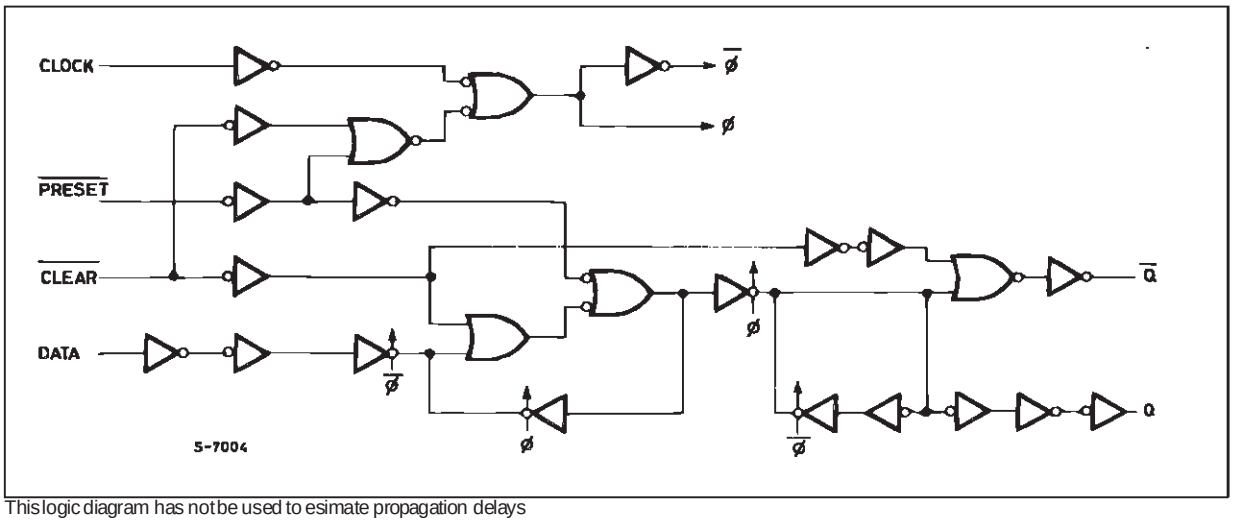
PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CLR}$, $2\overline{CLR}$	Asyncronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW-to-HIGH, Edge-Triggered)
4, 10	$1\overline{PR}$, $2\overline{PR}$	Asyncronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L	⌐	L	H	
H	H	H	⌐	H	L	
H	H	X	⌙	Q_n	$\overline{Q}_n$	NO CHANGE

X: Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to esimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage	-0.5 to + 7.0	V
V_O	DC Output Voltage (V_{CC}=0V)	-0.5 to + 7.0	V
V_O	DC Output Voltage (High or Low State) (note1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note2)	± 50	mA
I_O	DC Output Source/Sink Current	± 50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Supply Pin	± 100	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
1) I_O absolute maximum rating must be observed
2) $V_O < GND$, $V_O > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2.0 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (V_{CC}=0V)	0 to 5.5	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 3.0 to 3.6V)	± 24	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 2.7 to 3.0V)	± 12	mA
T_{op}	Operating Temperature:	-40 to +85	°C
dt/dv	Input Transition Rise or Fall Rate (V_{CC} = 3.0V) (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.5V to 3.6V
2) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value		Unit
		V_{CC} (V)			-40 to 85 °C		
					Min.	Max.	
V_{IH}	High Level Input Voltage	2.7 to 3.6			2.0		V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	2.7 to 3.6	V_I = V_{IH} or V_{IL}	I_O=-100 µA	V_{CC}-0.2		V
		2.7		I_O=-12 mA	2.2		
		3.0		I_O=-18 mA	2.4		
				I_O=-24 mA	2.2		
V_{OL}	Low Level Output Voltage	2.7 to 3.6	V_I = V_{IH} or V_{IL}	I_O=100 µA		0.2	V
		2.7		I_O=12 mA		0.4	
		3.0		I_O=16 mA		0.4	
		3.0		I_O=24 mA		0.55	
I_I	Input Leakage Current	2.7 to 3.6	V_I = 0 to 5.5 V			±5	µA
I_{off}	Power Off Leakage Current	0	V_I or V_O = 5.5V			100	µA
I_{CC}	Quiescent Supply Current	2.7 to 3.6	V_I = V_{CC} or GND			10	µA
			V_I or V_O = 3.6 to 5.5V			±10	
ΔI_{CC}	ICC incr. per input	2.7 to 3.6	V_{IH} = V_{CC} -0.6V			500	µA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1)	3.3	C_L = 50 pF V_{IL} = 0 V V_{IH} = 3.3V		0.8		V
V_{OLV}					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input $t_r = t_f$ = 2.5 ns)

Symbol	Parameter	Test Condition		Value		Unit
		V_{CC} (V)	Waveform	-40 to 85 °C		
				Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q or $\overline{Q}$	2.7	1	1.5	8.0	ns
		3.0 to 3.6		1.5	7.0	
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{PR}$ or $\overline{CLR}$ to Q or $\overline{Q}$	2.7	2	1.5	8.0	ns
		3.0 to 3.6		1.5	7.0	
t_s	Setup Time, HIGH or LOW level D to CK	2.7	1	2.5		ns
		3.0 to 3.6		2.5		
t_h	Hold Time, HIGH or LOW level D to CK	2.7	1	1.5		ns
		3.0 to 3.6		1.5		
t_w	CK Pulse Width, HIGH or LOW, $\overline{PR}$ or CLR Pulse Width, LOW	2.7	4	3.3		ns
		3.0 to 3.6		3.3		
t_{rec}	Recovery Time $\overline{PR}$ or $\overline{CLR}$ to CK	2.7	3	0		ns
		3.0 to 3.6		0		
f_{MAX}	Clock Pulse Frequency	3.0 to 3.6	1	150		MHz
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1, 2)	3.0 to 3.6			1.0	ns

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)

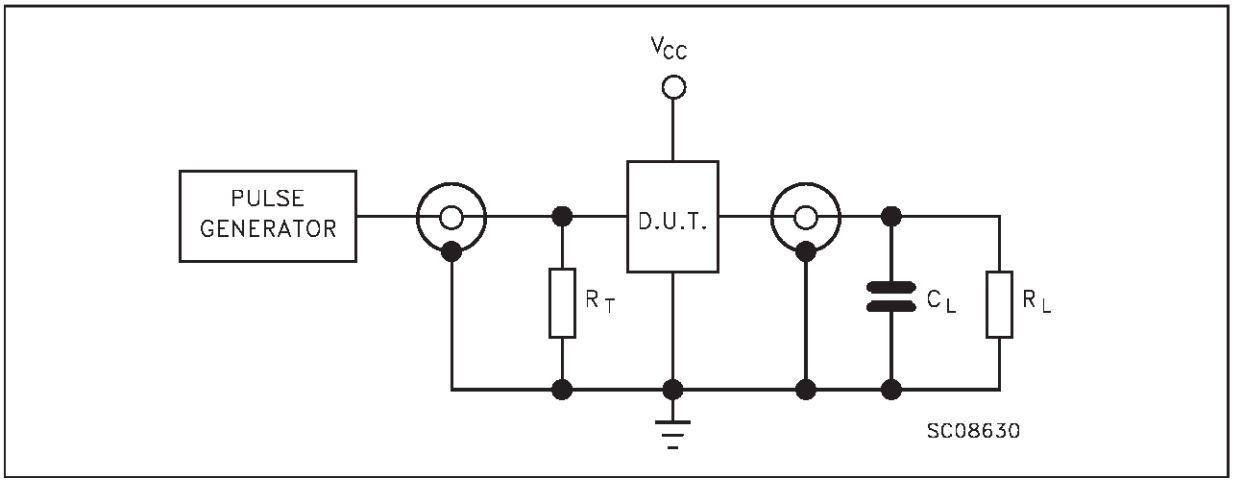
2) Parameter guaranteed by design

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance	3.3	V_{IN} = 0 to V_{CC}		6		pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	f_{IN} = 10MHz V_{IN} = 0 or V_{CC}		40		pF

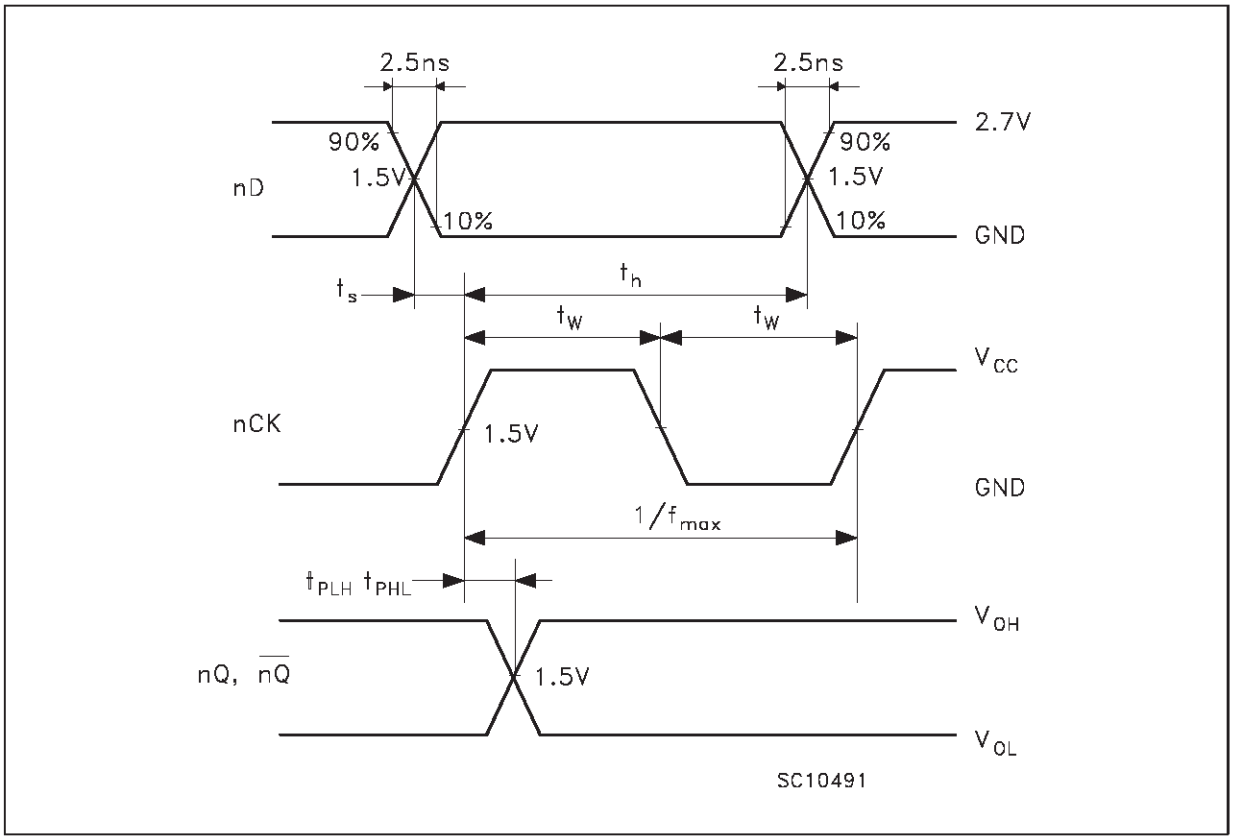
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/2$ (per Flip-Flop)

TEST CIRCUIT

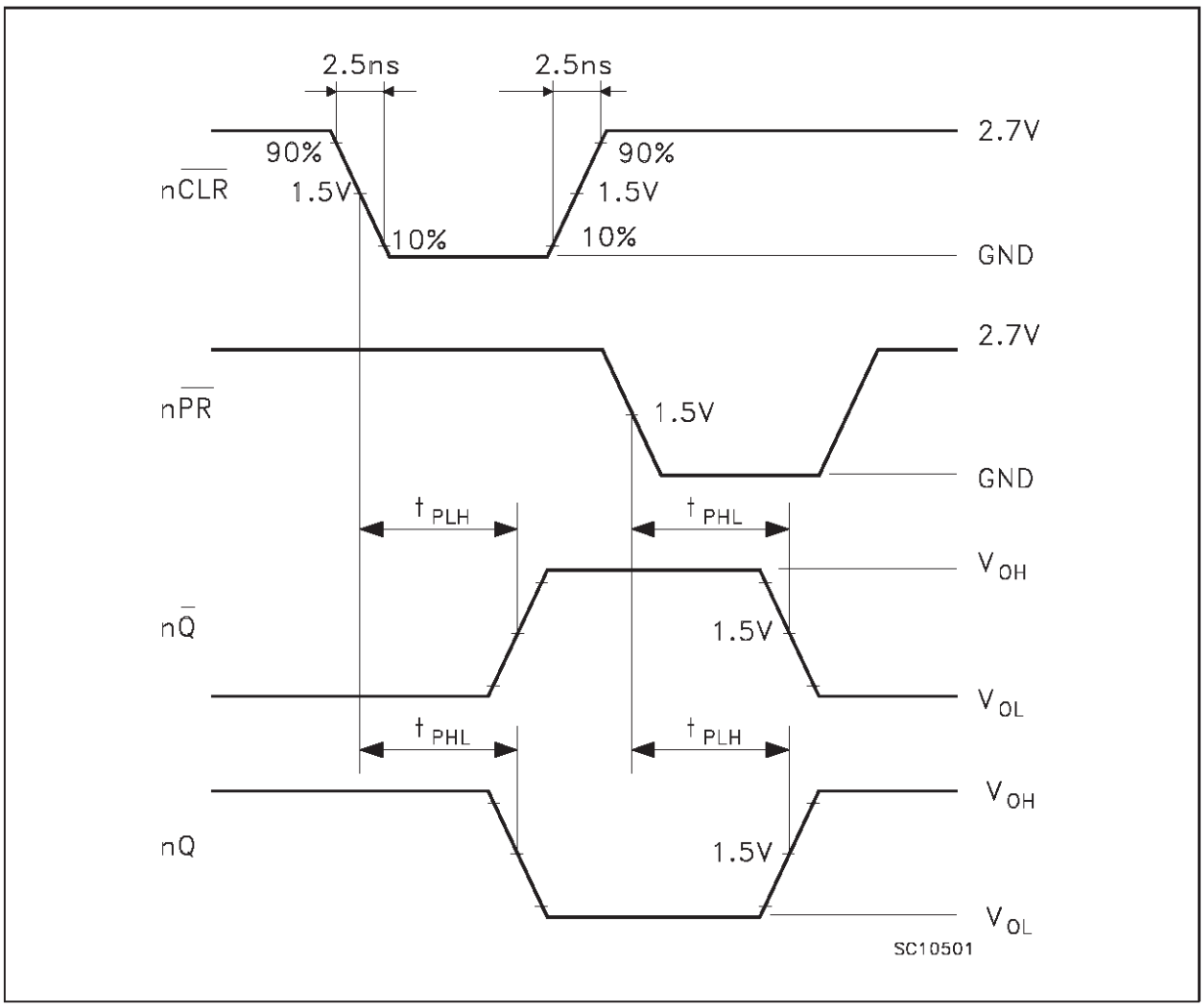


C_L = 50 pF or equivalent (includes jig and probe capacitance)
R_L = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

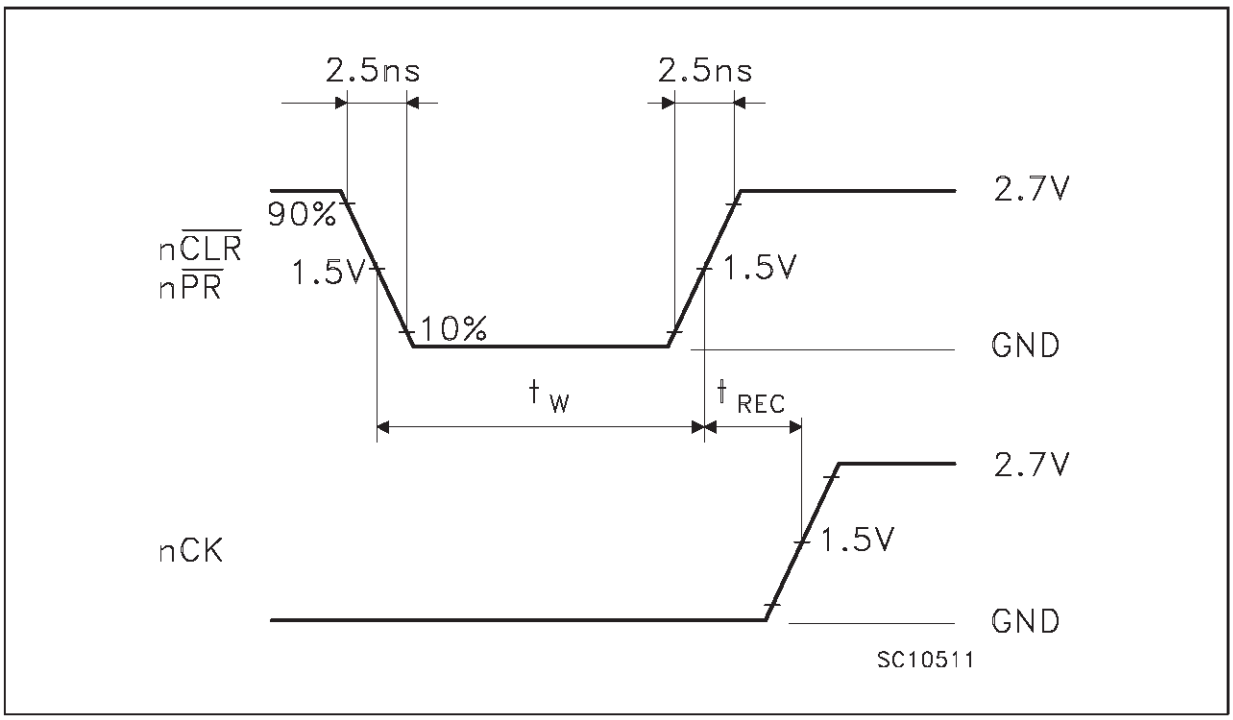
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



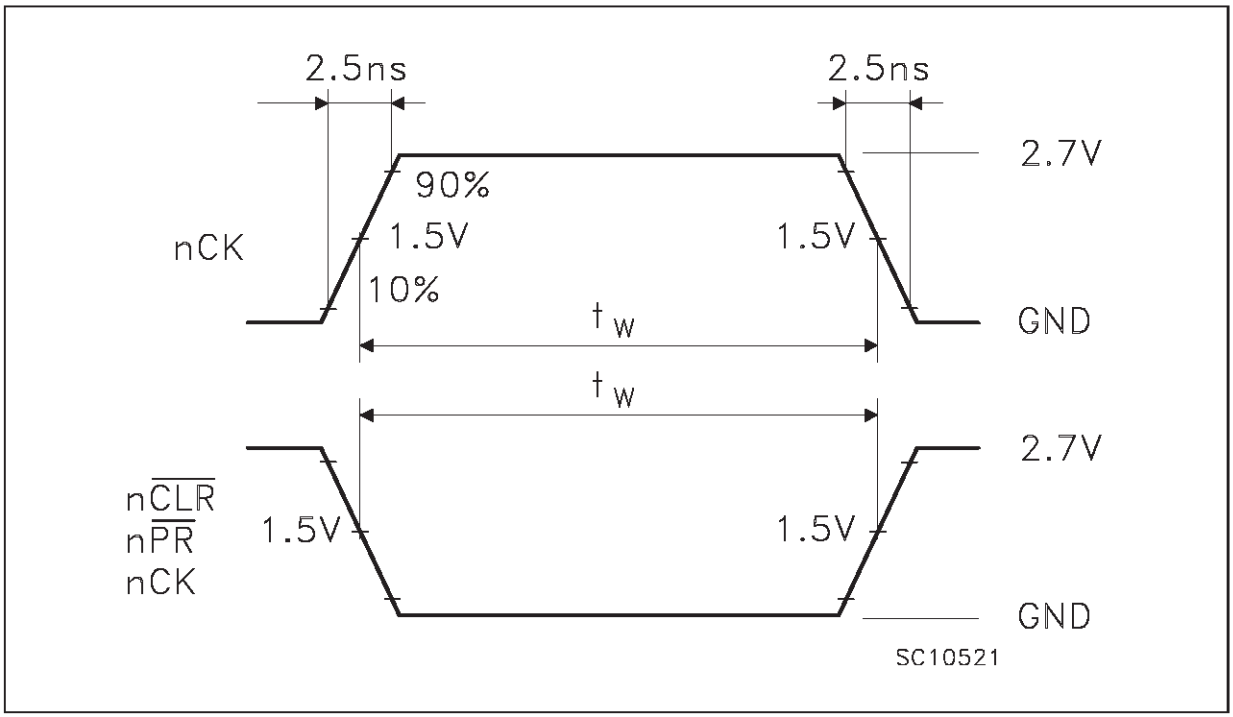
WAVEFORM 2: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



WAVEFORM 3: RECOVERY TIMES (f=1MHz; 50% duty cycle)

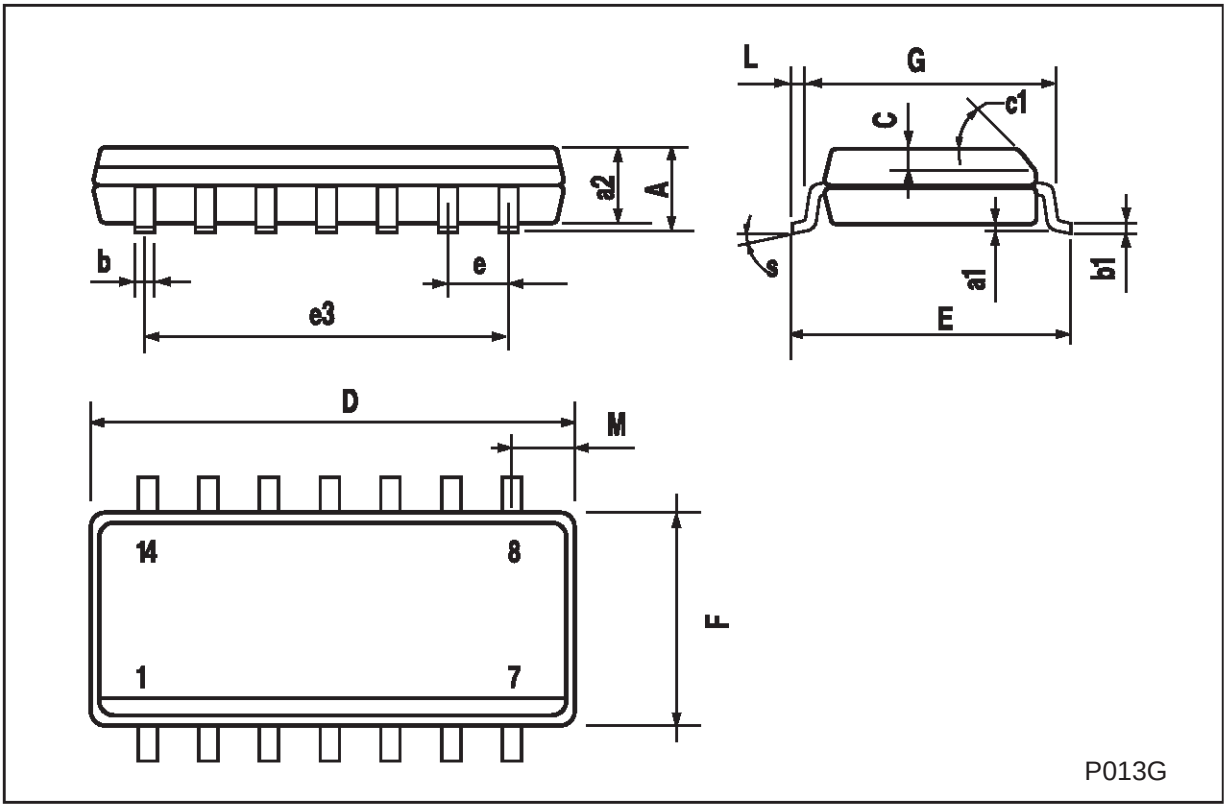


WAVEFORM 4: PULSE WIDTH



SO-14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



P013G

TSSOP14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0^o	4^o	8^o	0^o	4^o	8^o
L	0.50	0.60	0.70	0.020	0.024	0.028