



ESDA6V1B1

Application Specific Discretes
A.S.D.TM

TRANSILTM ARRAY
FOR ESD PROTECTION

MAIN APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- COMPUTER
- PRINTERS
- COMMUNICATION SYSTEMS
- GSM HANDSETS AND ACCESSORIES
- CAR RADIO

It is particularly recommended for parallel port protection where the line interface withstands only 2kV ESD surge

FEATURES

- 6 BIDIRECTIONAL TRANSILTM FUNCTIONS
- LOW LEAKAGE CURRENT : $I_R \text{ MAX} < 2 \mu\text{A}$
- 200 W PEAK PULSE POWER (8/20 μs)

DESCRIPTION

The ESDA6V1B1 is a monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against ESD.

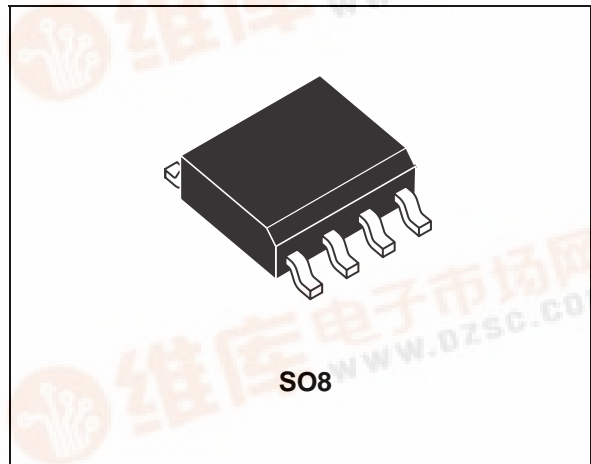
It clamps the voltage just above the logic level supply for positive and negative transients.

BENEFITS

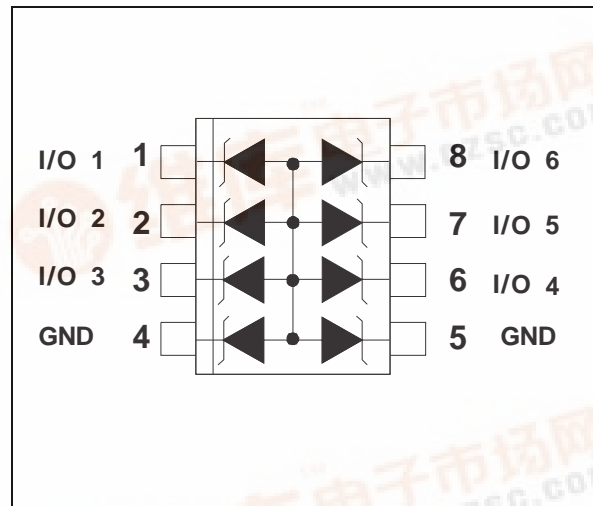
- High ESD protection level : up to 25 kV
- High integration
- Suitable for high density boards

COMPLIES WITH THE FOLLOWING STANDARDS :

- IEC 1000-4-2 : level 4
- MIL STD 883C-Method 3015-6 : class 3 (human body model)



FUNCTIONAL DIAGRAM



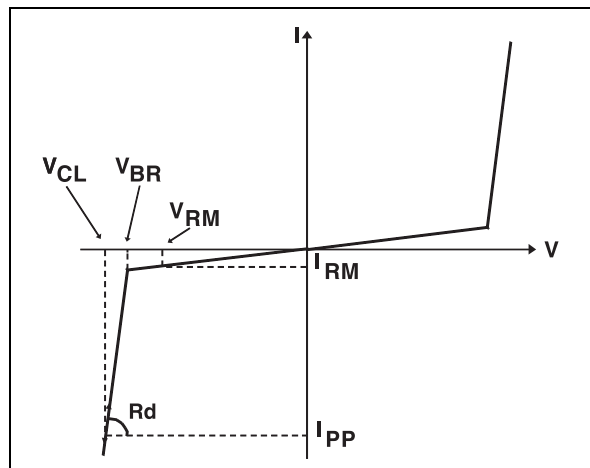
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ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

Symbol	Parameter	Value	Unit
V _{PP}	Electrostatic discharge MIL STD 883C - Method 3015-6	25	kV
P _{PP}	Peak pulse power (8/20μs)	200	W
T _{stg} T _j	Storage temperature range Maximum junction temperature	- 55 to + 150 150	°C °C
T _L	Maximum lead temperature for soldering during 10s	260	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
V _{RM}	Stand-off voltage
V _{BR}	Breakdown voltage
V _{CL}	Clamping voltage
I _{RM}	Leakage current
I _{PP}	Peak pulse current
α _T	Voltage temperature coefficient
C	Capacitance
R _d	Dynamic resistance



Types	V _{BR} @		I _R	I _{RM} @ V _{RM}		R _d typ. note 2	α _T max. note 3	C typ. 0V bias
	min. note 1	max.		max.	V _{RM}			
	V	V	mA	μA	V	Ω	10 ⁻⁴ /°C	pF
ESDA6V1B1	6.1	8	1	2	5	0.7	10	50

note 1 : Between two I/O pins or I/O pin and Ground

note 2 : Square pulse, I_{pp} = 25A, t_p = 2.5μs.

note 3 : Δ V_{BR} = α_T * (T_{amb} - 25°C) * V_{BR} (25°C)

CALCULATION OF THE CLAMPING VOLTAGE

USE OF THE DYNAMIC RESISTANCE

The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage V_{CL} . This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

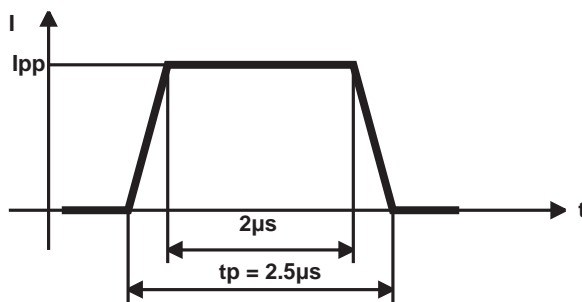
$$V_{CL} = V_{BR} + R_d I_{PP}$$

Where I_{PP} is the peak current through the ESDA cell.

As the value of the dynamic resistance remains stable for a surge duration lower than $20\mu s$, the $2.5\mu s$ rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of R_d .

DYNAMIC RESISTANCE MEASUREMENT

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical $8/20\mu s$ and $10/1000\mu s$ surges.



2.5 μs duration measurement wave.

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Fig. 1 : Peak power dissipation versus initial junction temperature.

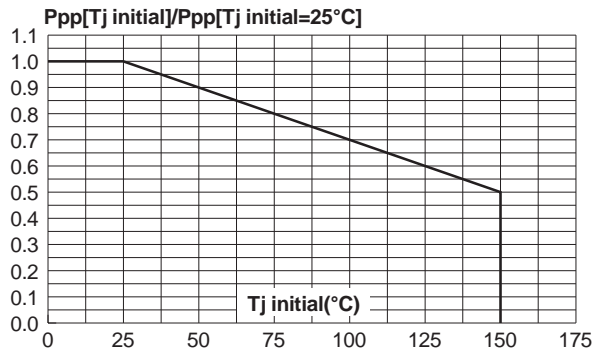


Fig. 2 : Peak pulse power versus exponential pulse duration ($T_j \text{ initial} = 25^\circ\text{C}$).

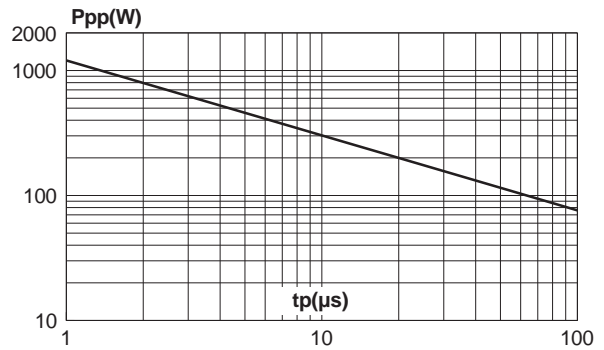


Fig. 3 : Clamping voltage versus peak pulse current ($T_j \text{ initial} = 25^\circ\text{C}$).
Rectangular waveform $t_p = 2.5 \mu\text{s}$.

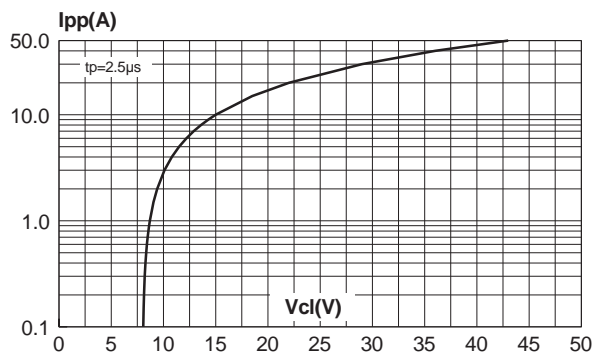


Fig. 4 : Capacitance versus reverse applied voltage (typical values).

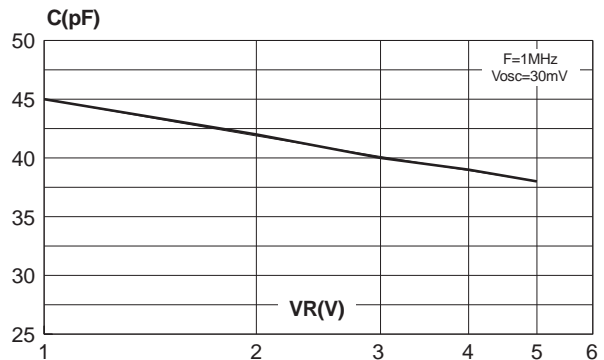
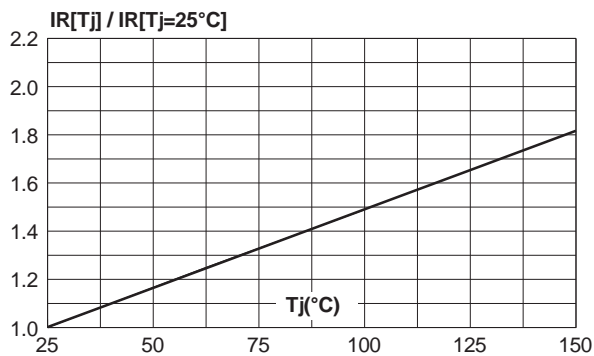
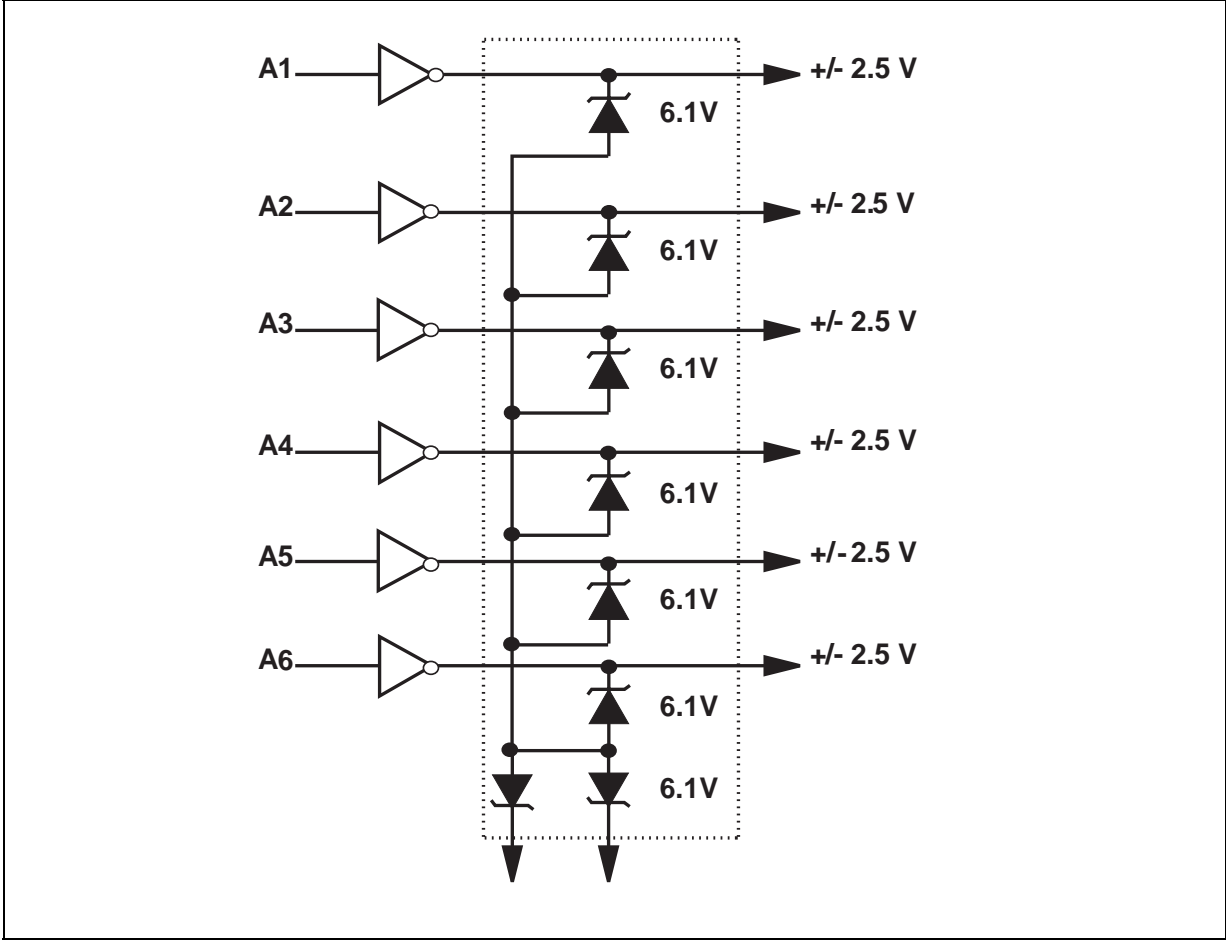


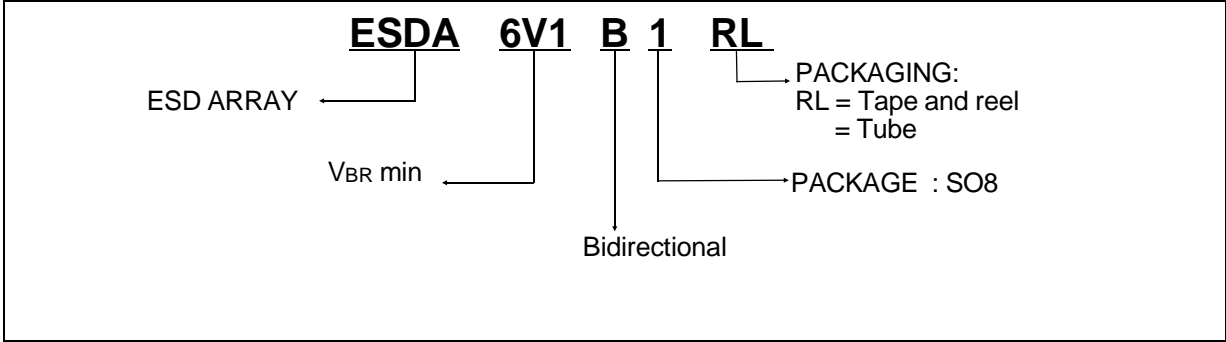
Fig. 5 : Relative variation of leakage current versus junction temperature (typical values).



APPLICATION EXAMPLE: Protection of symmetrical signals.



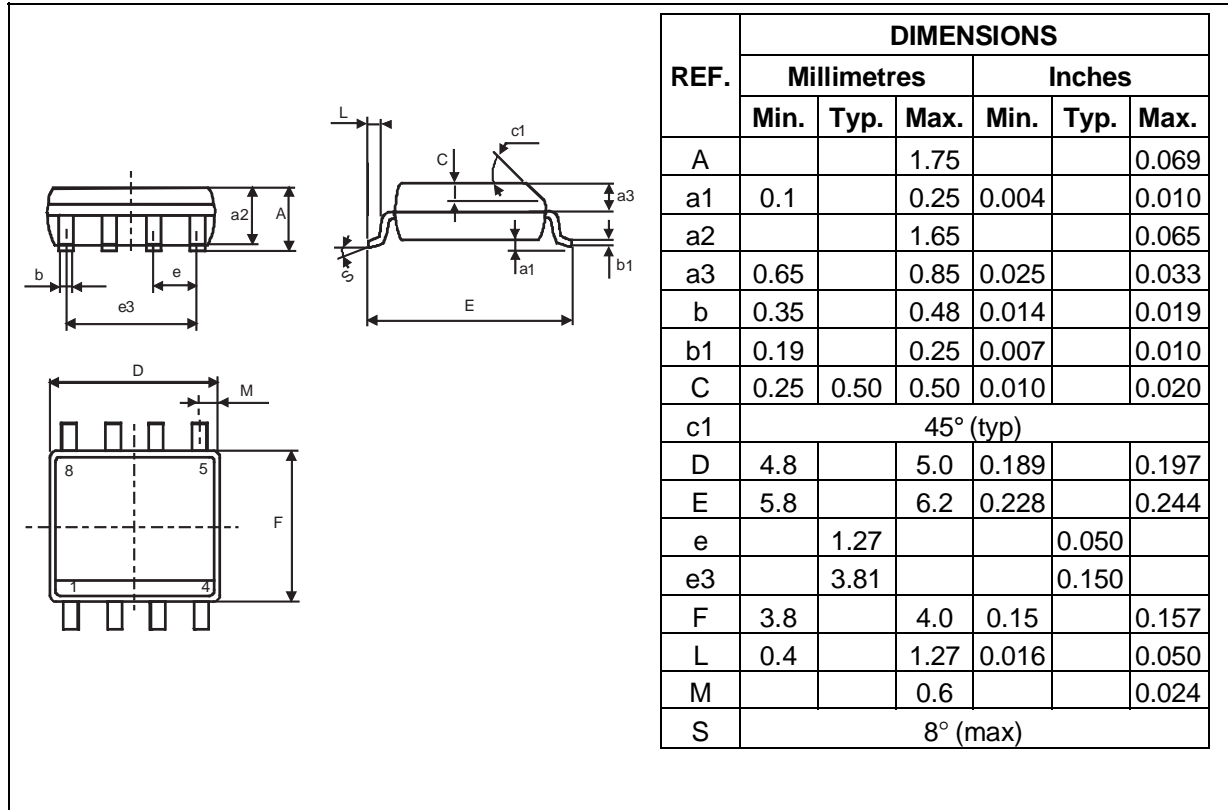
ORDER CODE



ESDA6V1B1

PACKAGE MECHANICAL DATA

SO8 Plastic



MARKING : Logo, Date Code, E25B1

Packaging : Preferred packaging is tape and reel.

Weight : 0.08g.

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