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ANALOG DEVICES

Quad 7 ns Single Supply Comparator

AD8564

FEATURES

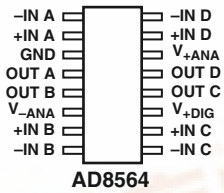
+5 V Single-Supply Operation
7 ns Propagation Delay
Low Power
Separate Input and Output Sections
TTL and CMOS Logic Compatible Outputs
Wide Output Swing
TSSOP, SOIC and PDIP Packages

APPLICATIONS

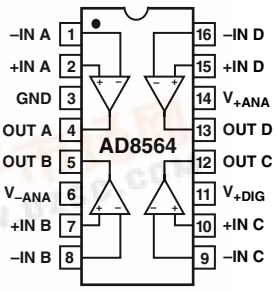
High Speed Timing
Line Receivers
Data Communications
High Speed V-to-F Converters
Battery Operated Instrumentation
High Speed Sampling Systems
Window Comparators
Read Channel Detection
PCMCIA Cards
Upgrade for MAX901 Designs

PIN CONFIGURATIONS

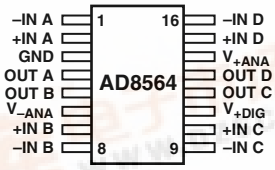
16-Lead Narrow Body SO
(S Suffix)
R-16A



16-Lead Epoxy DIP
(P Suffix)
N-16



16-Lead TSSOP
(RU-Suffix)
RU-16



GENERAL DESCRIPTION

The AD8564 is quad 7 ns comparator with separate input and output supplies, thus enabling the input stage to be operated from ±5 V dual supplies or a +5 V single supply while maintaining a CMOS/TTL-compatible output.

Fast 7 ns propagation delay makes the AD8564 a good choice for timing circuits and line receivers. Independent analog and digital supplies provide excellent protection from supply pin interaction. The AD8564 is pin compatible with the MAX901, and has lower supply currents.

All four comparators have similar propagation delays. The propagation delay for rising and falling signals is similar, and tracks over temperature and voltage. These characteristics make the AD8564 a good choice for high speed timing and data communications circuits. For a similar dual comparator with a latch function, please see the AD8598 data sheet. For a similar single comparator with latch function, please see the AD8561 data sheet.

The AD8564 is specified over the industrial (–40°C to +85°C) temperature range. The quad AD8564 is available in the 16-lead plastic DIP, narrow SO-16 surface mount, and 16-lead TSSOP packages.

REV. A

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AD8564–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_{+ANA} = V_{+DIG} = +5.0 V, V_{-ANA} = 0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2.3	7	mV
		–40°C ≤ T_A ≤ +85°C			8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Input Bias Current	I_B	V_{CM} = 0 V			±4	µA
	I_B	–40°C ≤ T_A ≤ +85°C			±9	µA
Input Offset Current	I_{OS}	V_{CM} = 0 V			±3	µA
Input Common-Mode Voltage Range	V_{CM}		0		+2.75	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ +3.0 V	65	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		3000		V/V
Input Capacitance	C_{IN}			3.0		pF
DIGITAL OUTPUTS						
Logic "1" Voltage	V_{OH}	I_{OH} = –3.2 mA, ΔV_{IN} > 250 mV	2.4	3.5		V
Logic "0" Voltage	V_{OL}	I_{OL} = 3.2 mA, ΔV_{IN} > 250 mV		0.3	0.4	V
DYNAMIC PERFORMANCE						
Propagation Delay	t_P	200 mV Step with 100 mV Overdrive		6.75	9.8	ns
		–40°C ≤ T_A ≤ +85°C[1]			13	ns
Propagation Delay	t_P	100 mV Step with 5 mV Overdrive[1]		8		ns
Differential Propagation Delay (Rising Propagation Delay vs. Falling Propagation Delay)	Δt_P	100 mV Step with 20 mV Overdrive[1]		0.5	2.0	ns
Rise Time		20% to 80%		3.8		ns
Fall Time		20% to 80%		1.5		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	+4.5 V ≤ V_{+ANA} and V_{+DIG} ≤ +5.5 V		80		dB
Analog Supply Current	I_{+ANA}			10.5	14.0	mA
		–40°C ≤ T_A ≤ +85°C			15.6	mA
Digital Supply Current	I_{DIG}	V_O = 0 V, R_L = ∞		6.0	7.0	mA
		–40°C ≤ T_A ≤ +85°C			8.0	mA
Analog Supply Current	I_{-ANA}			–7.0	14.0	mA
		–40°C ≤ T_A ≤ +85°C			15.6	mA

NOTES
[1] Guaranteed by design.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_{+ANA} = V_{+DIG} = +5.0 V, V_{-ANA} = –5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2.3	7	mV
		–40°C ≤ T_A ≤ +85°C			8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Input Bias Current	I_B	V_{CM} = 0 V			±4	µA
	I_B	–40°C ≤ T_A ≤ +85°C			±9	µA
Input Offset Current	I_{OS}	V_{CM} = 0 V			±3	µA
Input Common-Mode Voltage Range	V_{CM}		–4.9		+3.5	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ +3.0 V	65	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		3000		V/V
Input Capacitance	C_{IN}			3.0		pF
DIGITAL OUTPUTS						
Logic "1" Voltage	V_{OH}	I_{OH} = –3.2 mA, ΔV_{IN} > 250 mV	2.6	3.6		V
Logic "0" Voltage	V_{OL}	I_{OL} = 3.2 mA, ΔV_{IN} > 250 mV		0.2	0.3	V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Propagation Delay	t_P	200 mV Step with 100 mV Overdrive		6.75	9.8	ns
		–40°C ≤ T_A ≤ +85°C[1]		8	13	ns
Propagation Delay	t_P	100 mV Step with 5 mV Overdrive[1]		8		ns
Differential Propagation Delay (Rising Propagation Delay vs. Falling Propagation Delay)	Δt_P	100 mV Step with 20 mV Overdrive[1]		0.5	2.0	ns
Rise Time		20% to 80%		3		ns
Fall Time		20% to 80%		3		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	+4.5 V ≤ V_{+ANA} and V_{+DIG} ≤ +5.5 V	50	70		dB
Analog Supply Current	I_{+ANA}			10.8	14.0	mA
		–40°C ≤ T_A ≤ +85°C			15.6	mA
Digital Supply Current	I_{DIG}	V_O = 0 V, R_L = ∞		3.6	4.4	mA
		–40°C ≤ T_A ≤ +85°C			5.6	mA
Analog Supply Current	I_{-ANA}			–8.2	14.0	mA
		–40°C ≤ T_A ≤ +85°C			15.6	mA

NOTES
[1] Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Analog Supply Voltage . . . . . +14 V
Digital Supply Voltage . . . . . +17 V
Analog Positive Supply–Digital Positive Supply . . . . . –600 mV
Input Voltage[1] . . . . . ±7 V
Differential Input Voltage . . . . . ±8 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
N, R, RU Package . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Junction Temperature Range
N, R, RU Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) . . . . . +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
16-Lead Plastic DIP (N)	90	47	°C/W
16-Lead Narrow Body SO (R)	113	37	°C/W
16-Lead TSSOP (RU)	180	37	°C/W

NOTES
[1]The analog input voltage is equal to ±7 V or the analog supply voltage, whichever is less.
[2]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for, P-DIP, and θ_{JA} is specified for device soldered in circuit board for SOIC and TSSOP packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD8564AN	–40°C to +85°C	16-Lead Plastic DIP	N-16
AD8564AR	–40°C to +85°C	16-Lead Narrow Body SOIC	R-16A
AD8564ARU	–40°C to +85°C	16-Lead Thin Shrink Small Outline (TSSOP)	RU-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8564 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD8564–Typical Performance Characteristics ($V_{+ANA} = V_{+DIG} = +5$ V, $V_{-ANA} = 0$ V, $T_A = +25°C$ unless otherwise noted)

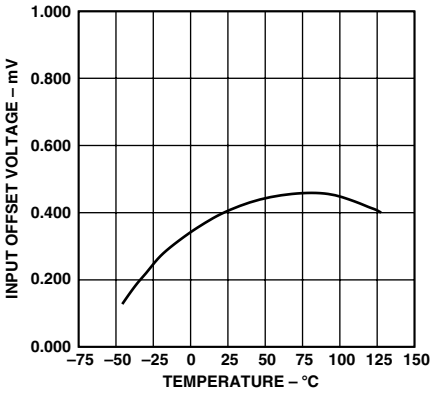


Figure 1. Input Offset Voltage vs. Temperature

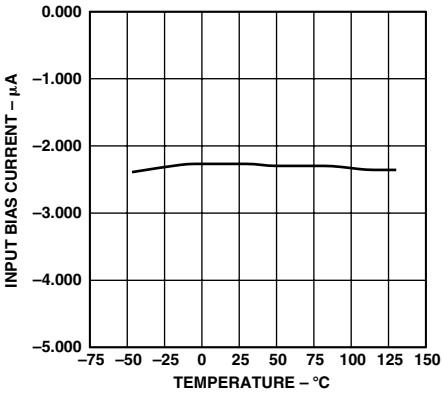


Figure 2. Input Bias Current vs. Temperature

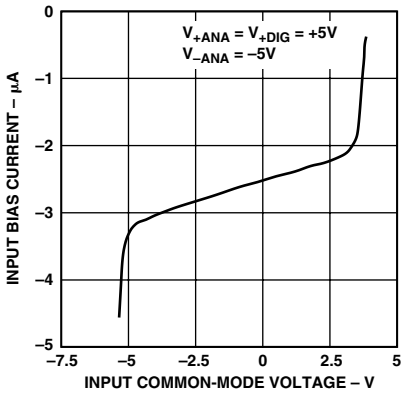


Figure 3. Input Bias Current vs. Input Common-Mode Voltage

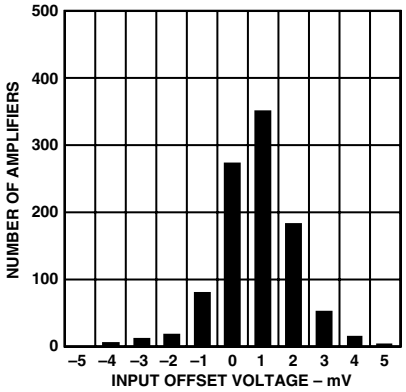


Figure 4. Input Offset Voltage

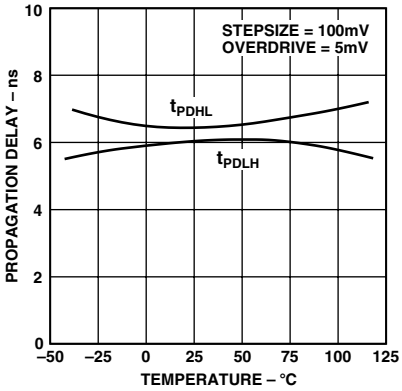


Figure 5. Propagation Delay, t_{PDHL}/ t_{PDLH} vs. Temperature

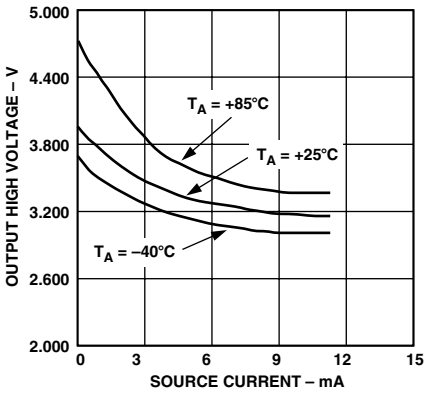


Figure 6. Output High Voltage, V_{OH} vs. Source Current

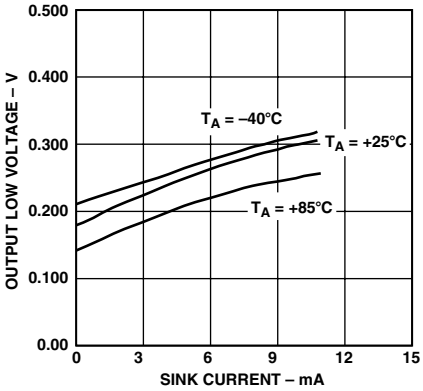


Figure 7. Output Low Voltage, V_{OL} vs. Sink Current

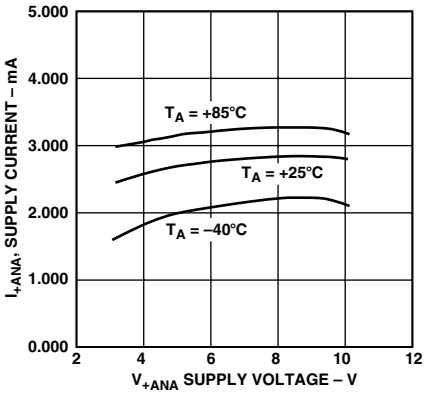


Figure 8. I_{+ANA}: Analog Supply Current/Comparator vs. Supply Voltage

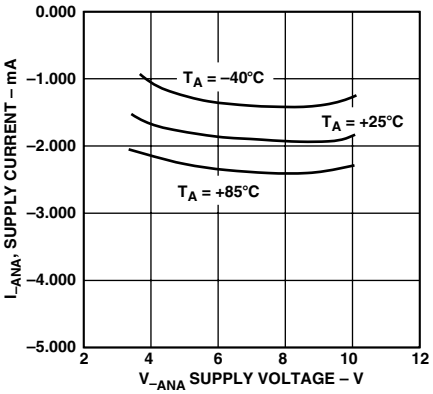


Figure 9. I_{-ANA}: Analog Supply Current/Comparator vs. Supply Voltage

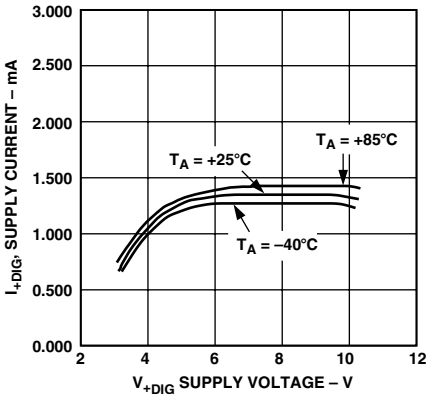


Figure 10. I_{+DIG}: Digital Supply Current/Comparator vs. Supply Voltage

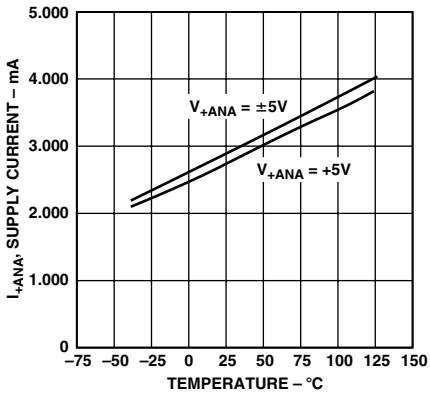


Figure 11. I_{+ANA}: Analog Supply Current/Comparator vs. Temperature

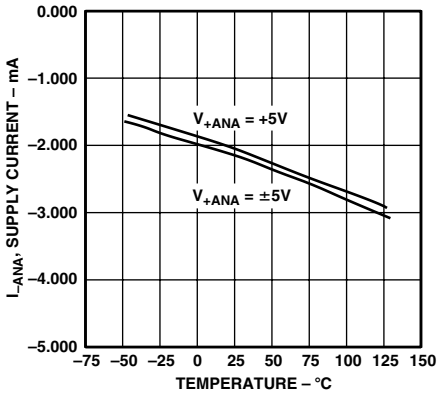


Figure 12. I_{-ANA}: Analog Supply Current/Comparator vs. Temperature

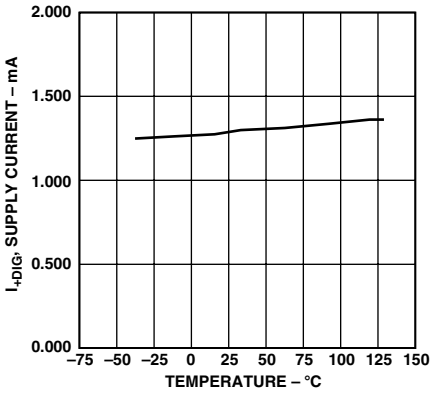


Figure 13. I_{+DIG}: Digital Supply Current/ Comparator vs. Temperature

APPLICATIONS

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator or amplifier, proper design and layout techniques should be used to ensure optimal performance from the AD8564. The performance limits of high speed circuitry can easily be a result of stray capacitance, improper ground impedance or other layout issues.

Minimizing resistance from source to the input is an important consideration in maximizing the high speed operation of the AD8564. Source resistance in combination with equivalent input capacitance could cause a lagged response at the input, thus delaying the output. The input capacitance of the AD8564 in combination with stray capacitance from an input pin to ground could result in several picofarads of equivalent capacitance. A combination of 3 kΩ source resistance and 5 pF of input capacitance yields a time constant of 15 ns, which is slower than the 5 ns capability of the AD8564. Source impedances should be less than 1 kΩ for the best performance.

It is also important to provide bypass capacitors for the power supply in a high speed application. A 1 µF electrolytic bypass capacitor should be placed within 0.5 inches of each power supply pin to ground. These capacitors will reduce any potential voltage ripples from the power supply. In addition, a 10 nF ceramic capacitor should be placed as close as possible from the power supply pins to ground. These capacitors act as a charge reservoir for the device during high frequency switching.

A ground plane is recommended for proper high speed performance. This can be created by using a continuous conductive plane over the surface of the circuit board, only allowing breaks in the plane for necessary current paths. The ground plane provides a low inductance ground, eliminating any potential differences at different ground points throughout the circuit board caused from "ground bounce." A proper ground plane also minimizes the effects of stray capacitance on the circuit board.

OUTPUT LOADING CONSIDERATIONS

The AD8564 output can deliver up to 40 mA of output current without any significant increase in propagation delay. The output of the device should not be connected to more than twenty (20) TTL input logic gates, or drive a load resistance less than 100 Ω.

To ensure the best performance from the AD8564 it is important to minimize capacitive loading of the output of the device. Capacitive loads greater than 50 pF will cause ringing on the output waveform and will reduce the operating bandwidth of the comparator. Propagation delay will also increase with capacitive loads above 100 pF.

INPUT STAGE AND BIAS CURRENTS

The AD8564 uses a PNP differential input stage which enables the input common-mode range to extend all the way from the negative supply rail to within 2.2 V of the positive supply rail. The input common-mode voltage can be found as the average of the voltage at the two inputs of the device. To ensure the fastest response time, care should be taken to not allow the input common-mode voltage to exceed this voltage.

The input bias current for the AD8564 is 4 µA. As with any PNP differential input stage, this bias current will go to zero on an input that is high and will double on an input that is low. Care should be taken in choosing resistor values to be connected to the inputs as large resistors could cause significant voltage drops due to the input bias current.

The input capacitance for the AD8564 is typically 3 pF. This is measured by inserting a kΩ source resistance to the input and measuring the change in propagation delay.

USING HYSTERESIS

Hysteresis can easily be added to a comparator through the addition of positive feedback. Adding hysteresis to a comparator offers an advantage in noisy environments where it is not desirable for the output to toggle between states when the input signal is near the switching threshold. Figure 14 shows a method for configuring the AD8564 with hysteresis.

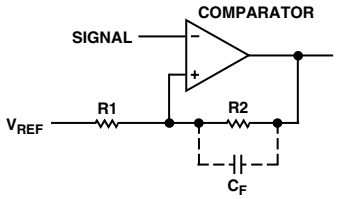


Figure 14. Configuring the AD8564 with Hysteresis

The input signal is connected directly to the inverting input of the comparator. The output is fed back to the noninverting input through R2 and R1. The ratio of R1 to R1 + R2 establishes the width of the hysteresis window with V_{REF} setting the center of the window, or the average switching voltage. The output will switch high when the input voltage is greater than V_{HI} and will not switch low again until the input voltage is less than V_{LO} as given in Equation 1:

$$V_{HI} = \left(V_{+} - 1 - V_{REF}\right)\frac{R1}{R1+R2} + V_{REF}$$

$$V_{LO} = V_{REF}\left(1 - \frac{R1}{R1+R2}\right) \qquad (1)$$

Where V_{+} is the positive supply voltage.

The capacitor C_F can also be added to introduce a pole into the feedback network. This has the effect of increasing the amount of hysteresis at high frequencies. This can be useful when comparing a relatively slow signal in a high frequency noise environment. At frequencies greater than $f_P = \frac{1}{2\pi C_F R2}$, the hysteresis window approaches $V_{HI} = V_{+} - 1$ V and $V_{LO} = 0$ V. At frequencies less than f_P the threshold voltages remain as in Equation 1.

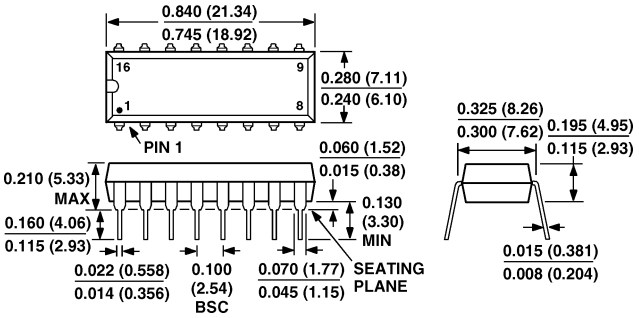
Spice Model

```
*  AD8564 SPICE Macro-Model Typical Values
*  8/98, Ver. 1.0
*  TAM / ADSC
*
* Node assignments
*                    noninverting input
*                    |       inverting input
*                    |       |       positive supply
*                    |       |       |       negative supply
*                    |       |       |       |       Output
*                    |       |       |       |       |
*                    |       |       |       |       |
*                    |       |       |       |       |
*                    |       |       |       |       |
.SUBCKT AD8564       1       2       99      50      45
*
* INPUT STAGE
*
*
Q1      4   3   5   PIX
Q2      6   2   5   PIX
IBIAS   99  5   800E-6
RC1     4   50  1k
RC2     6   50  1k
CL1     4   6   2.5E-12
CIN     1   2   3E-12
EOS     3   1   (4,6) 1E-3
*
* Reference Voltage
*
EREF    98  0   POLY(2)  (99,0)   (50,0)   0 0.5 0.5
RDUM    98  0   100E3
GSY     99  50  POLY(1)  (99,50)  8E-3 –2.6E-3
*
* Gain Stage Av=250 fp=100MHz
*
G1      98  20  (4.6)    0.25
R1      20  98  1E3
C1      20  98  16E-13
D1      20  21  DX
D2      22  20  DX
V1      99  21  DC 0.71
V2      22  50  DC 0.71
*
* Output Stage
*
Q3      99  41  46  NOX
Q4      47  42  50  NOX
RB1     43  41  200
RB2     40  42  200
CB1     99  41  10p
CB2     42  50  5p
RO1     46  45  2E3
RO2     47  45  500
EO1     98  43  POLY(1) (20,98) 0 1
EO2     40  98  POLY(1) (20,98) 0 1
*
* MODELS
*
.MODEL PIX PNP(BF=100,VAF=130,IS=1E-14)
.MODEL NOX NPN(BF=100,VAF=130,IS=1E-14)
.MODEL DX D(IS=1E-14,CJO=1E-15)
.ENDS AD8564
```

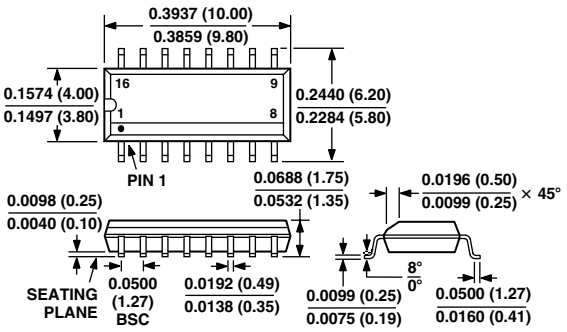
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

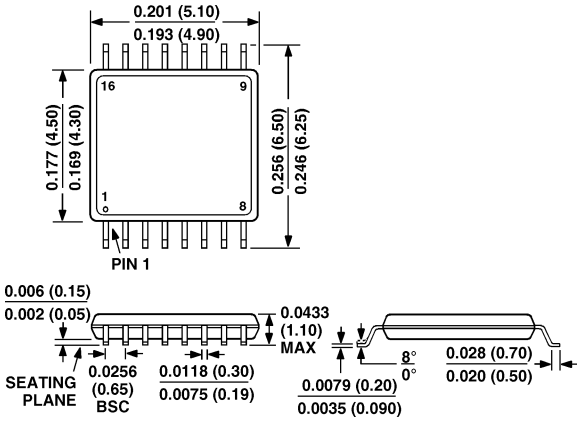
16-Lead Epoxy DIP (N-16)



16-Lead Narrow Body SOIC (R-16A)



16-Lead Thin Shrink Small Outline (TSSOP) (RU-16)



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