National Semiconductor

January 1999

DS90C385/DS90C365 +3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-85 MHz, +3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link-85 MHz

General Description

The DS90C385 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 85 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 297.5 Mbytes/sec. Also available is the DS90C365 that converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. Both transmitters can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge or Falling edge strobe transmitter will interoperate with a Falling edge strobe Receiver (DS90CF386/DS90CF366) without any translation logic.

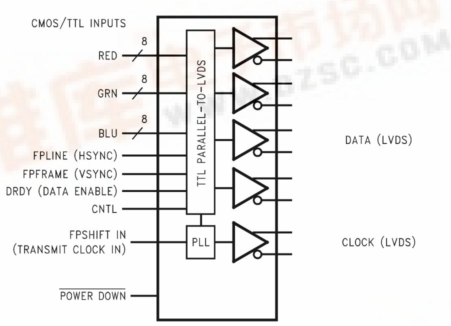
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- 20 to 85 MHz shift clock support
- Best–in–Class Set & Hold Times on TxINPUTs
- Tx power consumption <130 mW (typ) @85MHz Grayscale
- Tx Power-down mode <200µW (max)
- Supports VGA, SVGA, XGA and Single/Dual Pixel SXGA.
- Narrow bus reduces cable size and cost
- Up to 2.38 Gbps throughput
- Up to 297.5 Megabytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead or 48-lead TSSOP package

Block Diagrams

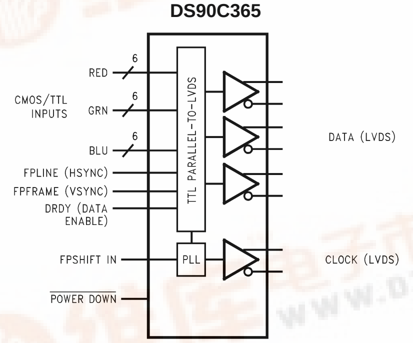
DS90C385



DS100868-1

Order Number DS90C385MTD
See NS Package Number MTD56

DS90C365



DS100868-29

Order Number DS90C365MTD
See NS Package Number MTD48

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

DS90C385/DS90C365 +3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-85 MHz, +3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD)Link-85 MHz

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.5V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec)	+260˚C
Maximum Package Power Dissipation Capacity @ 25˚C	
MTD56 (TSSOP) Package: DS90C385	1.63 W
MTD48 (TSSOP) Package: DS90C365	1.98 W
Package Derating: DS90C385	12.5 mW/˚C above +25˚C
Package Derating: DS90C365	16 mW/˚C above +25˚C
ESD Rating	
(HBM, 1.5kΩ, 100pF)	> 7 kV
(EIAJ, 0Ω, 200 pF)	> 500V
Latch Up Tolerance @ 25˚C	> ±300mA

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Supply Noise Voltage (V_{CC})			100	mV_{PP}
TxCLKIN frequency	20		85	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}			+1.8	+10	µA
		V_{IN} = GND		−10	0		µA
LVDS DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states					35	mV
V_{OS}	Offset Voltage (Note 4)			1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between complimentary output states					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{Power Down}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case DS90C385	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		31	45	mA
			f = 40 MHz		32	50	mA
			f = 65 MHz		37	55	mA
			f = 85 MHz		42	60	mA
ICCTG	Transmitter Supply Current 16 Grayscale DS90C385	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		29	38	mA
			f = 40 MHz		30	40	mA
			f = 65 MHz		35	45	mA
			f = 85 MHz		39	50	mA
ICCTW	Transmitter Supply Current Worst Case DS90C365	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		28	42	mA
			f = 40 MHz		29	47	mA
			f = 65 MHz		34	52	mA
			f = 85 MHz		39	57	mA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
ICCTG	Transmitter Supply Current 16 Grayscale DS90C365	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern *(Figures 3, 4)*	f = 32.5 MHz		26	35	mA
			f = 40 MHz		27	37	mA
			f = 65 MHz		32	42	mA
			f = 85 MHz		36	47	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Driver Outputs in TRI-STATE under Power Down Mode			10	55	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: V_{OS} previously referred as V_{CM}.

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
TCIT	TxCLK IN Transition Time *(Figure 6)*	1.0		6.0	ns
TCIP	TxCLK IN Period *(Figure 7)*	11.76	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*	0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*	0.35T	0.5T	0.65T	ns
TXIT	TxIN Transition Time	1.5		6.0	ns

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 5)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 5)*			0.75	1.5	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figures 13, 14)* (Note 5)	f = 40 MHz	−0.25	0	0.25	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		3.32	3.57	3.82	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		6.89	7.14	7.39	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		10.46	10.71	10.96	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		14.04	14.29	14.54	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		17.61	17.86	18.11	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		21.18	21.43	21.68	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figures 13, 14)* (Note 5)	f = 65 MHz	−0.20	0	0.20	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		2.00	2.20	2.40	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.20	4.40	4.60	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.39	6.59	6.79	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.59	8.79	8.99	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.79	10.99	11.19	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.99	13.19	13.39	ns

Transmitter Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figures 13, 14)* (Note 5)	f = 85 MHz	−0.20	0	0.20	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		1.48	1.68	1.88	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		3.16	3.36	3.56	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		4.84	5.04	5.24	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		6.52	6.72	6.92	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		8.20	8.40	8.60	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		9.88	10.08	10.28	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*		2.5			ns
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay *(Figure 8)* T_A=25˚C,V_{CC}=3.3V		3.8		6.3	ns
	TxCLK IN to TxCLK OUT Delay *(Figure 8)*		2.8		7.1	ns
TJCC	Transmitter Jitter Cycle-to-Cycle *(Figures 15, 16)* (Note 6)	f = 85 MHz		210	230	ps
		f = 65 MHz		210	230	ps
		f = 40 MHz		350	370	ps
TPLLS	Transmitter Phase Lock Loop Set *(Figure 9)*				10	ms
TPDD	Transmitter Power Down Delay *(Figure 12)*				100	ns

Note 5: The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

Note 6: The limits are based on bench characterization of the device's jitter response over the power supply voltage range. Output clock jitter is measured with a cycle-to-cycle jitter of +/−3ns applied to the input clock signal while data inputs are switching (See Figures 15 and 16). A jitter event of 3ns, represents worse case jump in the clock edge from most graphics controller VGA chips currently available. This parameter is used when calculating system margin as described in AN-1059.

AC Timing Diagrams

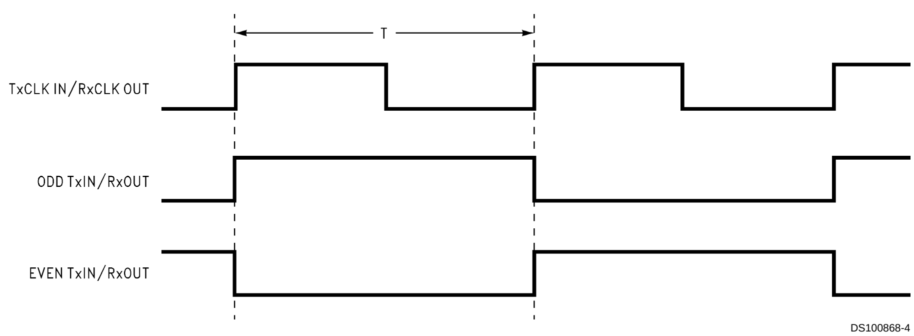


FIGURE 1. "Worst Case" Test Pattern (Note 7)

AC Timing Diagrams (Continued)

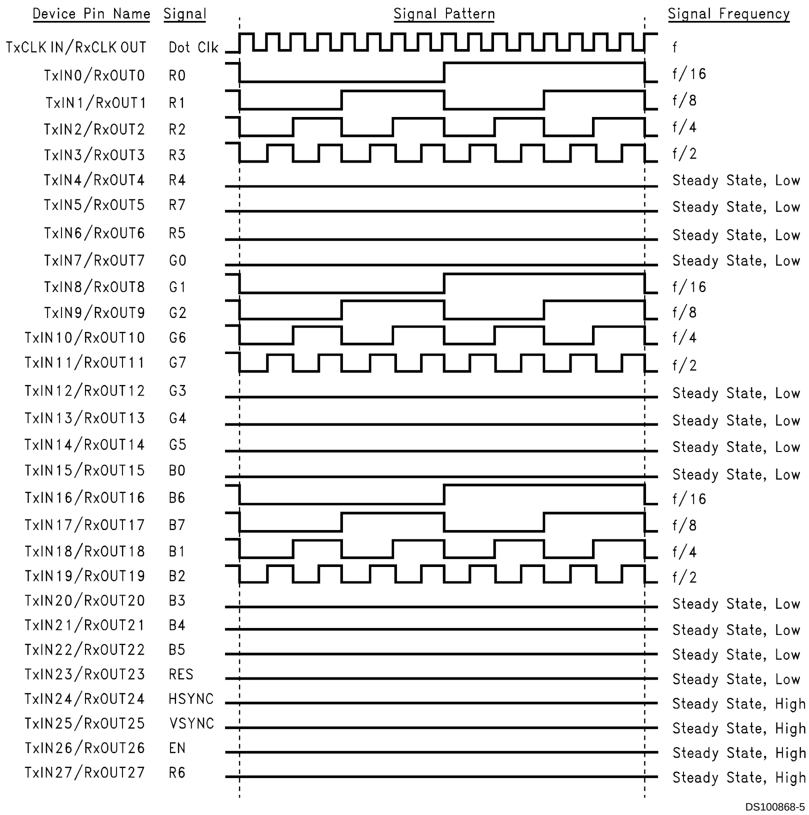


FIGURE 2. "16 Grayscale" Test Pattern - DS90C385 (Notes 8, 9, 10)

AC Timing Diagrams (Continued)

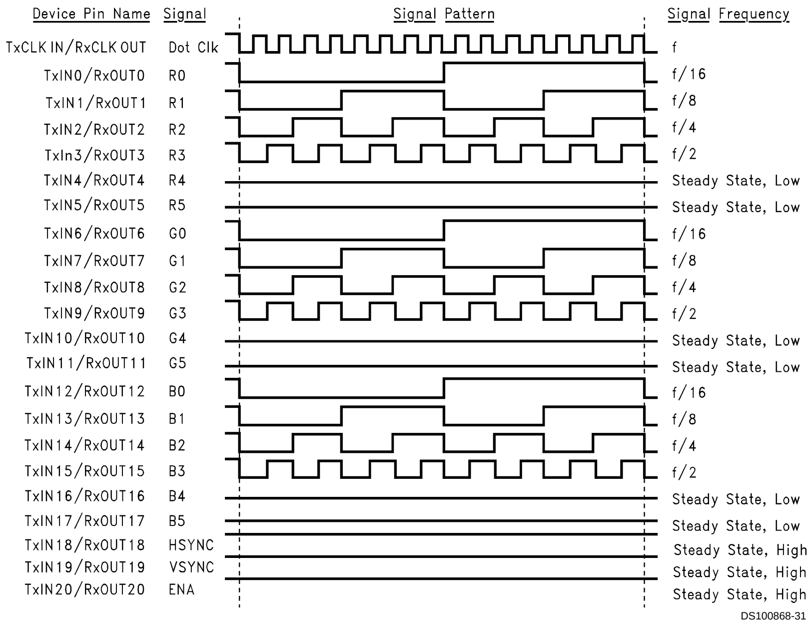


FIGURE 3. "16 Grayscale" Test Pattern - DS90C365 (Notes 8, 9, 10)

Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 8: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 9: *Figures 1, 2, 3* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Note 10: Recommended pin to signal mapping. Customer may choose to define differently.

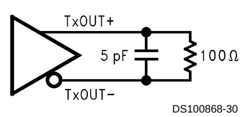


FIGURE 4. DS90C385/DS90C365 (Transmitter) LVDS Output Load

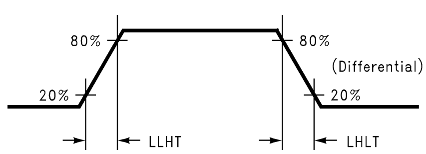


FIGURE 5. DS90C385/DS90C365 (Transmitter) LVDS Transition Times

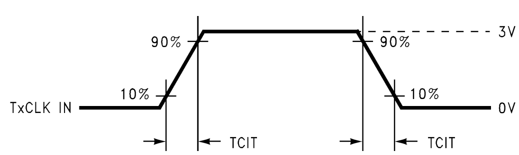


FIGURE 6. DS90C385/DS90C365 (Transmitter) Input Clock Transition Time

AC Timing Diagrams (Continued)

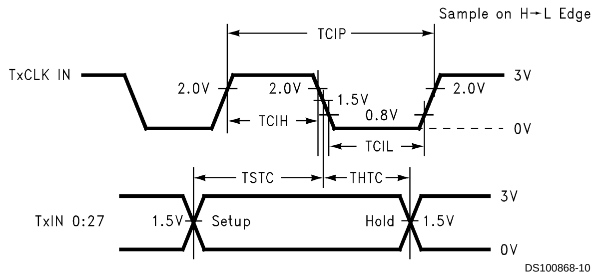


FIGURE 7. DS90C385/DS90C365 (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

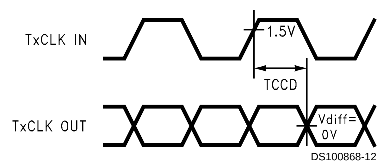


FIGURE 8. DS90C385/DS90C365 (Transmitter) Clock In to Clock Out Delay

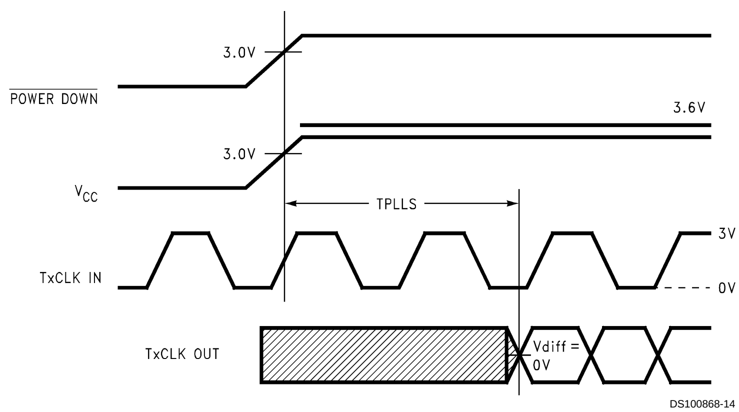


FIGURE 9. DS90C385/DS90C365 (Transmitter) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

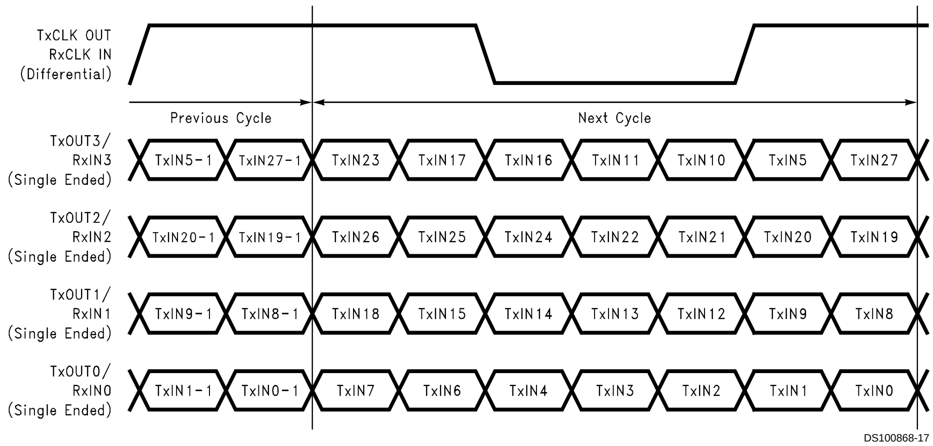


FIGURE 10. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90C385

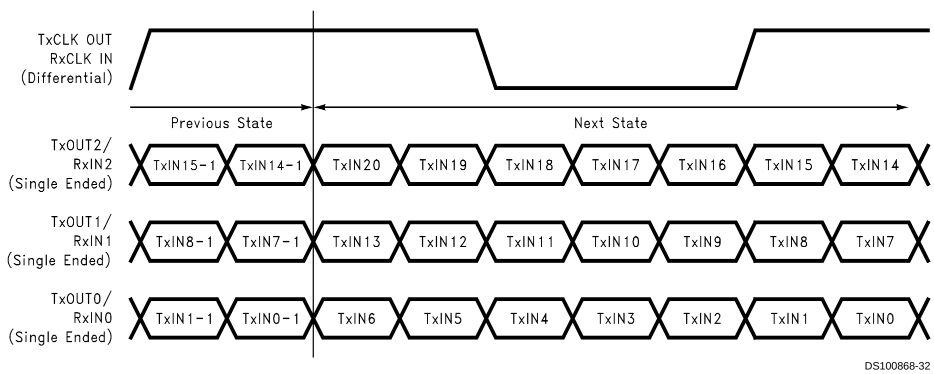


FIGURE 11. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90C365

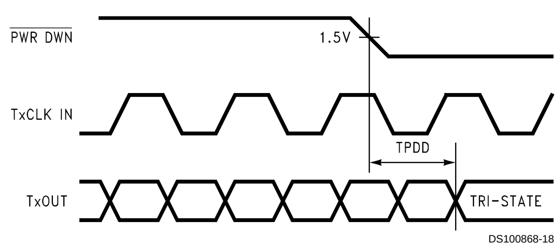


FIGURE 12. Transmitter Power Down Delay

AC Timing Diagrams (Continued)

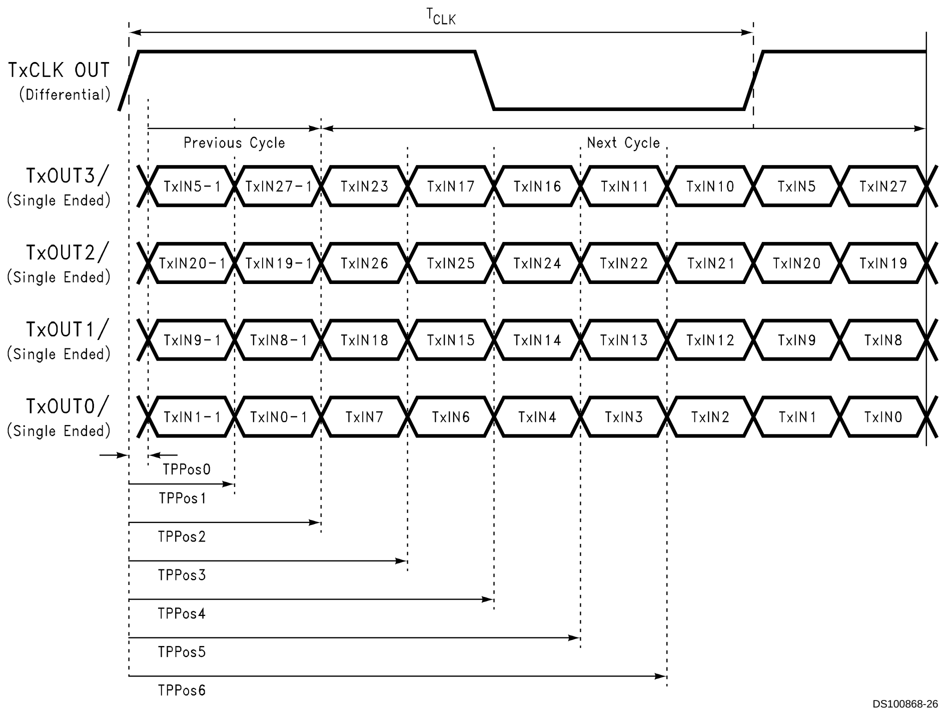


FIGURE 13. Transmitter LVDS Output Pulse Position Measurement - DS90C385

AC Timing Diagrams (Continued)

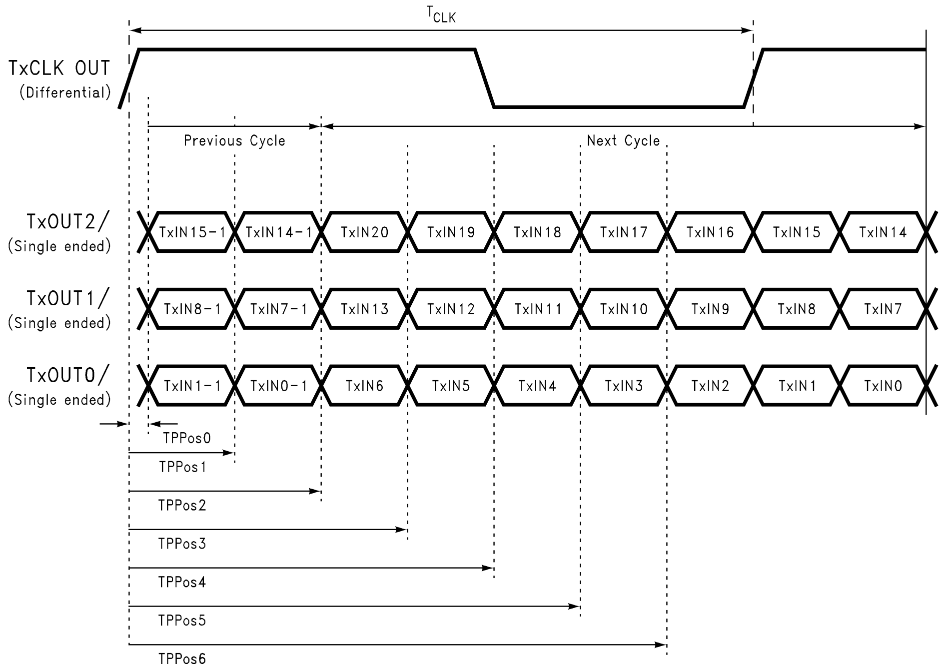


FIGURE 14. Transmitter LVDS Output Pulse Position Measurement - DS90C365

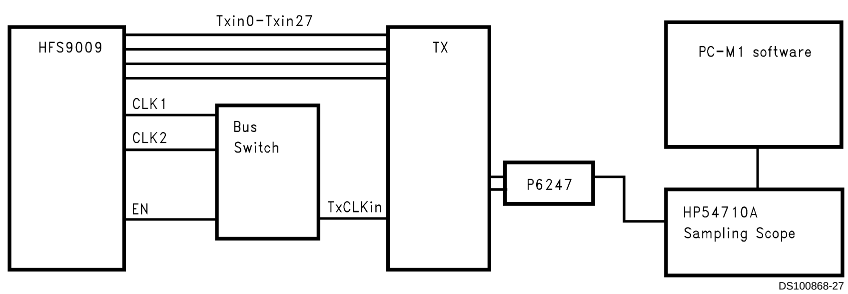


FIGURE 15. TJCC Test Setup - DS90C385 Shown

AC Timing Diagrams (Continued)

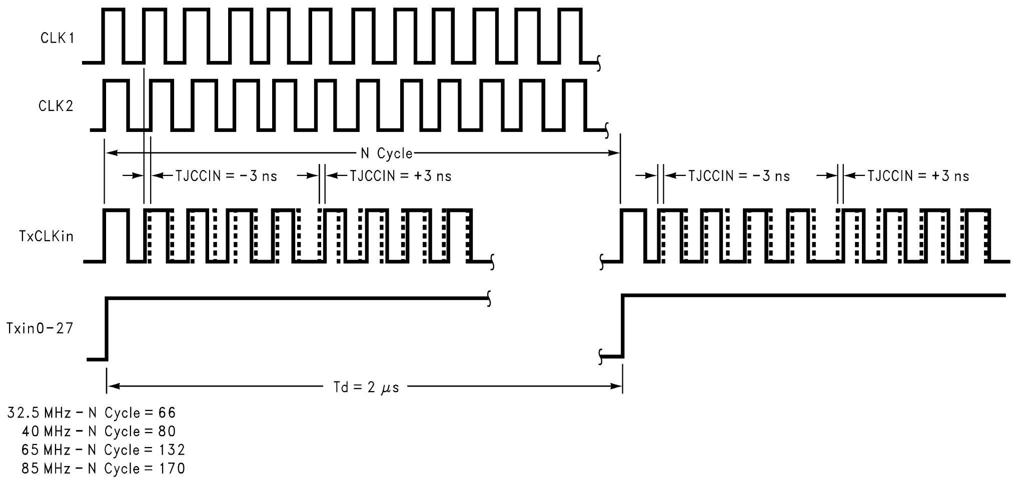


FIGURE 16. Timing Diagram of the Input cycle-to-cycle clock jitter

DS90C385 Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	4	Positive LVDS differential data output.
TxOUT−	O	4	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. Pin name TxCLK IN.
R_FB	I	1	Programmable strobe select (See Table 1).
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	3	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

DS90C365 Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	3	Positive LVDS differential data output.
TxOUT−	O	3	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. Pin name TxCLK IN.
R_FB	I	1	Programmable strobe select (See Table 1).
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.

DS90C365 Pin Description—FPD Link Transmitter (Continued)

Pin Name	I/O	No.	Description
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	3	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

Applications Information

The DS90C385/DS90C365 are backward compatible with the DS90C383/DS90C363, DS90C383A/DS90C363A and are a pin-for-pin replacement. The device (DS90C385/DS90C365) utilizes a different PLL architecture employing an internal 7X clock for enhanced pulse position control.

This device (DS90C385/DS90C365) also features reduced variation of the TCCD parameter which is important for dual pixel applications. (See AN-1084) TCCD variation has been measured to be less than 500ps at 85MHz under normal operating conditions.

This device may also be used as a replacement for the DS90CF583/563 (5V, 65MHz) and DS90CF581/561 (5V, 40MHz) FPD-Link Transmitters with certain considerations/modifications:

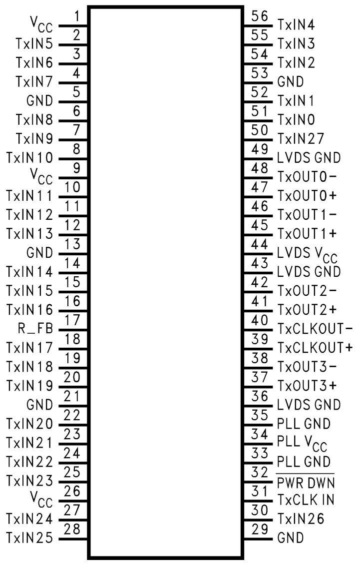
1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of the transmitter.
2. The DS90C385/DS90C365 transmitter input and control inputs accept 3.3V TTL/CMOS levels. They are not 5V tolerant.
3. To implement a falling edge device for the DS90C385/DS90C365, the R_FB pin may be tied to ground OR left unconnected (an internal pull-down resistor biases this pin low). Biasing this pin to Vcc implements a rising edge device.

Transmitter Clock Jitter Cycle-to-Cycle

Figures 15 and 16 illustrate the timing of the input clock relative to the input data. The input clock (TxCLKin) is intentionally shifted to the left −3ns and +3ns to the right when data (Txin0-27) is high. This 3ns of cycle-to-cycle clock jitter is repeated at a period of 2µs, which is the period of the input data (1µs high, 1µs low). At different operating frequencies the N Cycle is changed to maintain the desired 3ns cycle-to-cycle jitter at 2µs period.

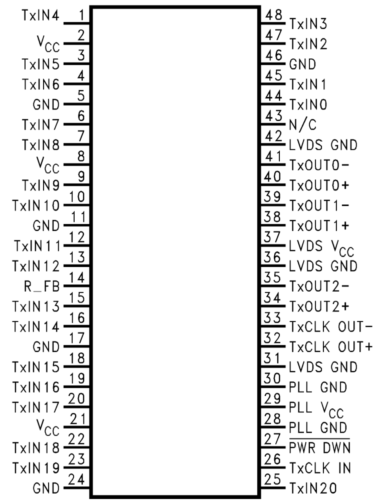
Pin Diagram

DS90C385



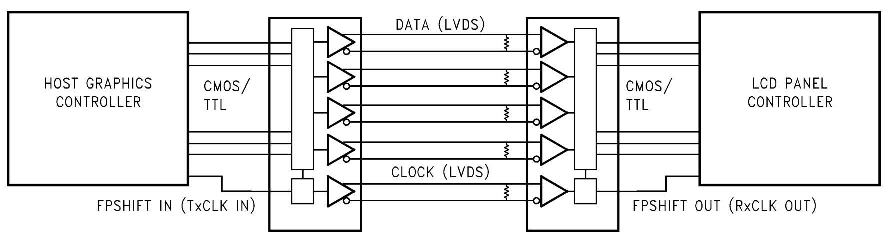
DS100868-23

DS90C365



DS100868-24

Application



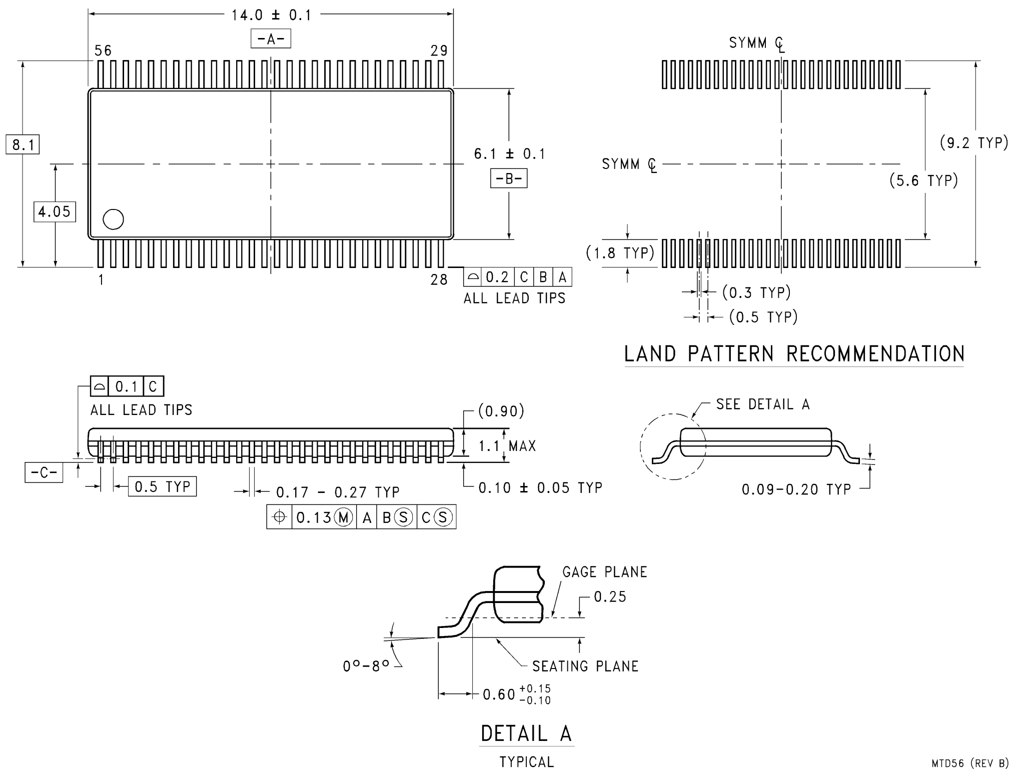
DS100868-3

Truth Table

TABLE 1. Programmable Transmitter (DS90C385/DS90C365)

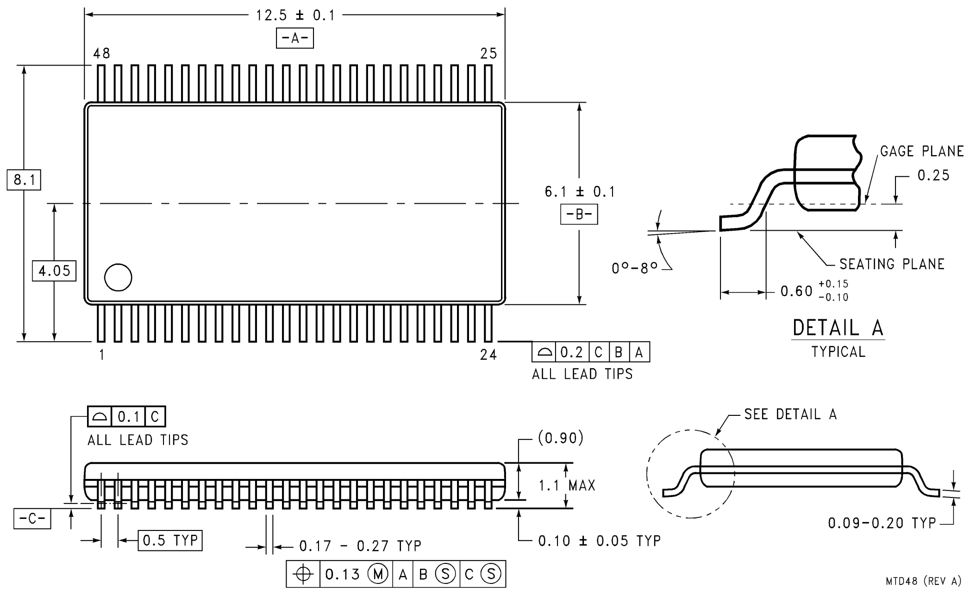
Pin	Condition	Strobe Status
R_FB	R_FB = V_{CC}	Rising edge strobe
R_FB	R_FB = GND or NC	Falling edge strobe

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Molded Thin Shrink Small Outline Package, JEDEC
Dimensions in millimeters only
Order Number DS90C385MTD
NS Package Number MTD56

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Molded Thin Shrink Small Outline Package, JEDEC
Dimensions in millimeters only
Order Number DS90C365MTD
NS Package Number MTD48

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

www.national.com