

GALVANTECH INC.

GVT7164B19
64K X 18 SYNCHRONOUS BURST SRAM

SYNCHRONOUS BURST SRAM

64K x 18 SRAM

**+5V SUPPLY WITH CLOCKED,
REGISTERED INPUTS, BURST COUNTER**

FEATURES

- Fast access times: 8, 9, 10, and 12ns
- Fast clock speed: 83, 66, and 50 MHz
- Provide high performance 2-1-1-1 access rate
- Fast OE# access times: 5 and 6ns
- Single +5V \pm 5% power supply
- 3.3V I/O compatible
- Clamp diodes to VSS at all inputs and outputs
- Common data inputs and data outputs
- Byte writeable via dual write enables
- Address, data and control registers
- Internally self-timed WRITE CYCLE
- Automatic power-down for low power applications
- High board density 52-lead PLCC packages

OPTIONS

- Timing
 - 8ns access/12ns cycle
 - 9ns access/15ns cycle
 - 10ns access/15ns cycle
 - 12ns access/20ns cycle
- Packages
 - 52-pin PLCC

MARKING

- 8
- 9
- 10
- 12
- C

GENERAL DESCRIPTION

The Galvantech Synchronous Burst SRAM family employs high-speed, low power CMOS designs using advanced double-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

The GVT7164B19 SRAM integrates 65,536 x18 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), burst control inputs (ADSC#, ADSP#, and ADV#), and write enables (WEL# and WEH#).

Asynchronous input includes the output enable (OE#). The data outputs (DQ), enabled by OE#, are also asynchronous.

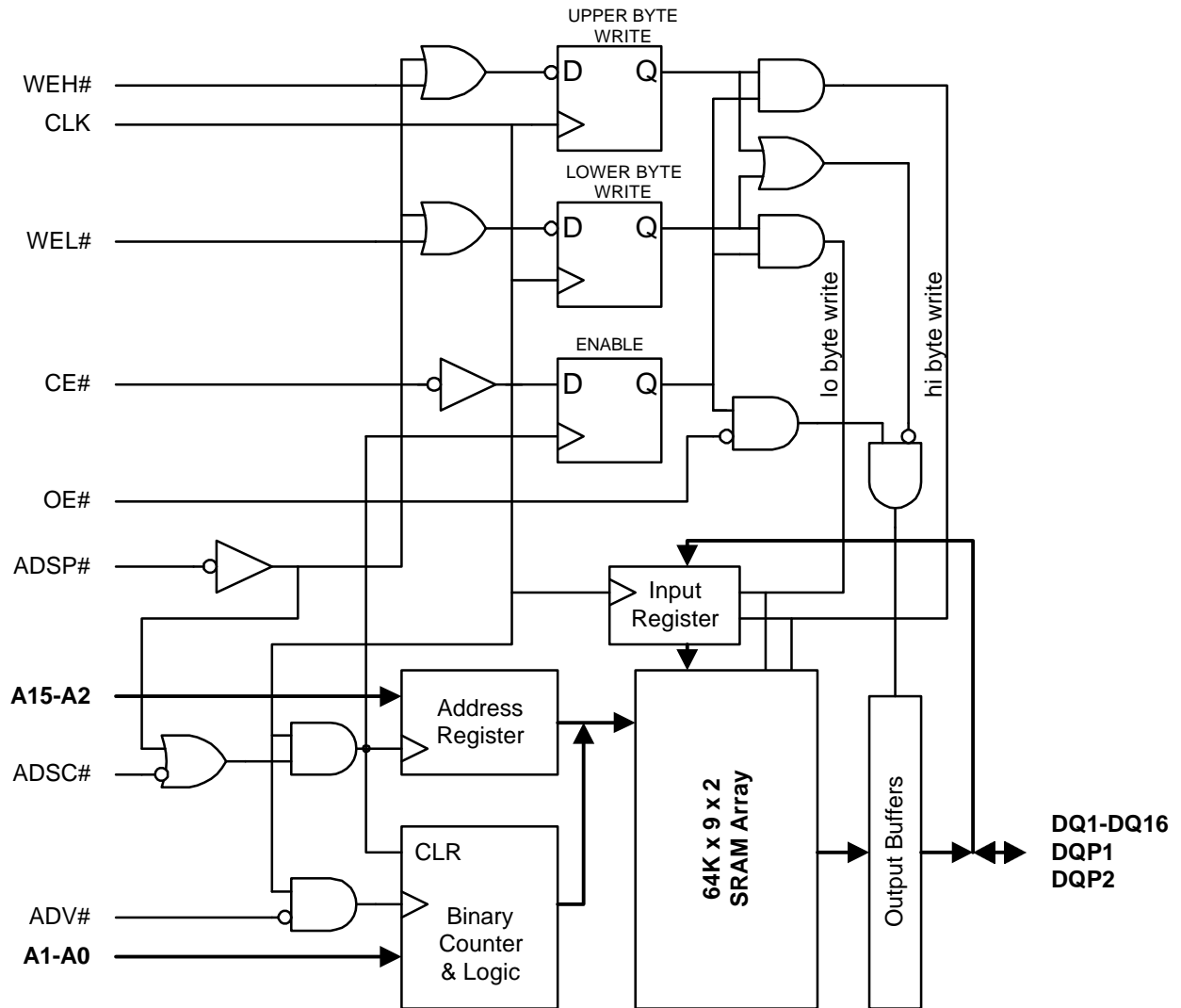
Addresses and chip enables are registered with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address, data inputs, and write controls are registered on-chip to initiate self-timed WRITE cycle. WRITE cycles can be one or two bytes wide as controlled by the write control inputs. Individual byte enables allow individual bytes to be written. WEL# controls DQ1-DQ8 and DQP1. WEH# controls DQ9-DQ16 and DQP2.

The GVT7164B19 operates from a +5V power supply. All inputs and outputs are TTL-compatible. The device is ideally suited for 486, Pentium™, 680x0, and for systems that are benefited from a wide synchronous data bus.

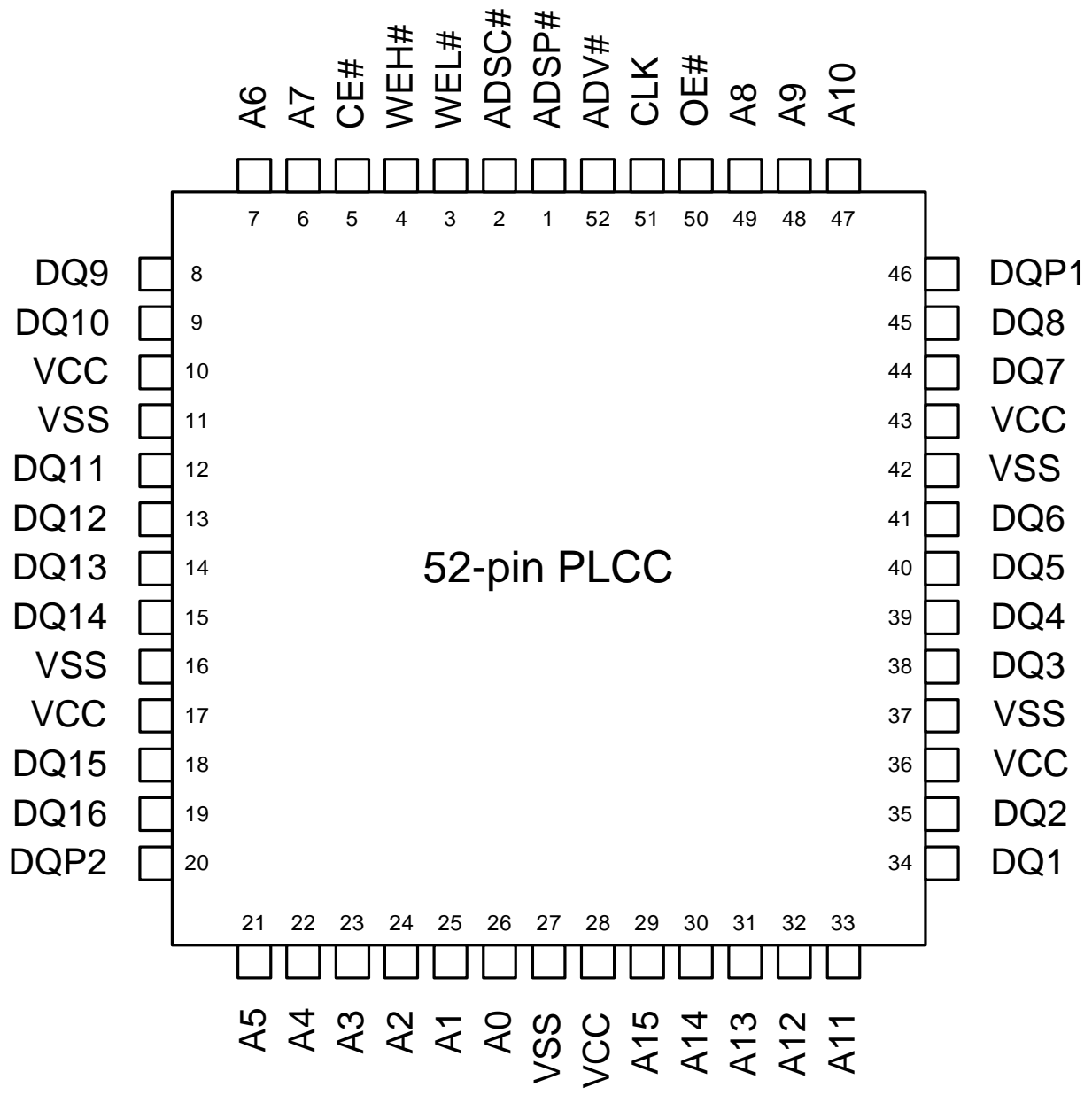


FUNCTIONAL BLOCK DIAGRAM



NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN ASSIGNMENT (Top View)



PIN DESCRIPTIONS

| PLCC PINS | SYMBOL | TYPE | DESCRIPTION |
|--|------------|-------------------|---|
| 26, 25, 24, 23, 22, 21, 7, 6, 49, 48, 47, 33, 32, 31, 30, 29 | A0-A15 | Input-Synchronous | Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle. |
| 3,4 | WEL#, WEH# | Input-Synchronous | Byte Write Enables: A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. WEL# controls DQ1-DQ8 and DQP1. WEH# controls DQ9-DQ16 and DQP2. Data I/O are high impedance if either of these inputs are LOW. |
| 51 | CLK | Input-Synchronous | Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. |
| 5 | CE# | Input-Synchronous | Chip Enable: This active LOW input is used to enable the device. |
| 50 | OE# | Input | Output Enable: This active LOW asynchronous input enables the data output drivers. |
| 52 | ADV# | Input-Synchronous | Address Advance: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance). |
| 1 | ADSP# | Input-Synchronous | Address Status Processor: This active LOW input causes a new external address to be registered and a READ cycle is initiated using the new address. |
| 2 | ADSC# | Input-Synchronous | Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs. |
| 34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19 | DQ1-DQ16 | Input/Output | Data Inputs/Outputs: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK. |
| 46, 20 | DQP1, DQP2 | Input/Output | Parity Inputs/Outputs: DQP1 is parity bit for DQ1-DQ8 and DQP2 is parity bit for DQ9-DQ16. |
| 10, 17, 28, 36, 43 | VCC | Supply | Supply: +5V \pm 5% |
| 11, 16, 27, 37, 42 | VSS | Ground | Ground: GND |

BURST ADDRESS TABLE

| First Address (external) | Second Address (internal) | Third Address (internal) | Fourth Address (internal) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| A...A00 | A...A01 | A...A10 | A...A11 |
| A...A01 | A...A00 | A...A11 | A...A10 |
| A...A10 | A...A11 | A...A00 | A...A01 |
| A...A11 | A...A10 | A...A01 | A...A00 |

TRUTH TABLE

| OPERATION | ADDRESS USED | CE# | ADSP# | ADSC# | ADV# | WRITE# | OE# | CLK | DQ |
|------------------------------|--------------|-----|-------|-------|------|--------|-----|-----|--------|
| Deselected Cycle, Power Down | None | H | X | L | X | X | X | L-H | High-Z |
| Deselected Cycle, Power Down | None | H | L | X | X | X | X | L-H | High-Z |
| READ Cycle, Begin Burst | External | L | L | X | X | X | L | L-H | Q |
| READ Cycle, Begin Burst | External | L | L | X | X | X | H | L-H | High-Z |
| WRITE Cycle, Begin Burst | External | L | H | L | X | L | X | L-H | D |
| READ Cycle, Begin Burst | External | L | H | L | X | H | L | L-H | Q |
| READ Cycle, Begin Burst | External | L | H | L | X | H | H | L-H | High-Z |
| READ Cycle, Continue Burst | Next | X | H | H | L | H | L | L-H | Q |
| READ Cycle, Continue Burst | Next | X | H | H | L | H | H | L-H | High-Z |
| WRITE Cycle, Continue Burst | Next | X | H | H | L | L | X | L-H | D |
| READ Cycle, Suspend Burst | Current | X | H | H | H | H | L | L-H | Q |
| READ Cycle, Suspend Burst | Current | X | H | H | H | H | H | L-H | High-Z |
| WRITE Cycle, Suspend Burst | Current | X | H | H | H | L | X | L-H | D |

- Note:
1. X means "don't care." H means logic HIGH. L means logic LOW. WRITE# = L means WEL#*WEH# equals LOW. WRITE# = H means WEL#*WEH# equals HIGH.
 2. WEL# enables write to DQ1-DQ8 and DQP1. WEH# enables write to DQ9-DQ16 and DQP2.
 3. All inputs except OE# must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
 4. Suspending burst generates wait cycle.
 5. For a write operation following a read operation, OE# must be HIGH before the input data required setup time plus High-Z time for OE# and staying HIGH throughout the input data hold time.
 6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
 7. ADSP# LOW along with chip being selected always initiates an READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting WRITE# LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE FOR READ/WRITE

| FUNCTION | WEH# | WEL# | CE# | OE# |
|-----------------|------|------|-----|-----|
| READ | H | H | L | L |
| WRITE high byte | L | H | L | X |
| WRITE low byte | H | L | L | X |
| WRITE all bytes | L | L | L | X |

ABSOLUTE MAXIMUM RATINGS*

| | |
|--|-------------------|
| Voltage on VCC Supply Relative to VSS..... | -0.5V to +7.0V |
| V _{IN} | -0.5V to VCC+0.5V |
| Storage Temperature (plastic) | -55°C to +125° |
| Junction Temperature | +125° |
| Power Dissipation | 1.6W |
| Short Circuit Output Current | 30mA |

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_a ≤ 70°C; VCC = 5V ±5% unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|------------------------------|--|-----------------|------|---------|-------|-------|
| Input High (Logic 1) voltage | | V _{IH} | 2.2 | VCC+0.3 | V | 1,2 |
| Input Low (Logic 0) Voltage | | V _{IL} | -0.5 | 0.8 | V | 1, 2 |
| Input Leakage Current | 0V ≤ V _{IN} ≤ VCC | I _{L1} | -2 | 2 | uA | |
| Output Leakage Current | Output(s) disabled, 0V ≤ V _{OUT} ≤ VCC | I _{LO} | -2 | 2 | uA | |
| Output High Voltage | I _{OH} = -4.0mA | V _{OH} | 2.4 | 3.3 | V | 1, 11 |
| Output Low Voltage | I _{OL} = 8.0mA | V _{OL} | | 0.4 | V | 1, 11 |
| Supply Voltage | | VCC | 4.75 | 5.25 | V | 1 |

| DESCRIPTION | CONDITIONS | SYM | TYP | -8 | -9 | -10 | -12 | UNITS | NOTES |
|---------------------------------|--|------------------|-----|-----|-----|-----|-----|-------|-----------|
| Power Supply Current: Operating | Device selected; all inputs ≤ V _{IL} or ≥ V _{IH} ; cycle time ≥ 1KC MIN; VCC = MAX; outputs open | I _{CC} | 200 | 300 | 275 | 265 | 250 | mA | 3, 12, 13 |
| CMOS Standby | Device deselected; VCC = MAX; all inputs ≤ VSS +0.2 or ≥ VCC -0.2; all inputs static; CLK frequency = 0 | I _{SB2} | 5 | 12 | 12 | 12 | 12 | mA | 12,13 |
| TTL Standby | Device deselected; all inputs ≤ V _{IL} or ≥ V _{IH} ; all inputs static; VCC = MAX; CLK frequency = 0 | I _{SB3} | 15 | 35 | 35 | 35 | 35 | mA | 12,13 |
| Clock Running | Device deselected; all inputs ≤ V _{IL} or ≥ V _{IH} ; VCC = MAX; CLK cycle time ≥ 1KC MIN | I _{SB4} | 30 | 60 | 50 | 50 | 40 | mA | 12,13 |

CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | MAX | UNITS | NOTES |
|-------------------------------|--|----------------|-----|-----|-------|-------|
| Input Capacitance | T _A = 25°C; f = 1 MHz VCC = 5.0V | C _I | 4 | 5 | pF | 4 |
| Input/Output Capacitance (DQ) | | C _O | 6 | 8 | pF | 4 |

THERMAL CONSIDERATION

| DESCRIPTION | CONDITIONS | SYMBOL | PLCC TYP | UNITS | NOTES |
|--|--|-----------------|----------|-------|-------|
| Thermal Resistance - Junction to Ambient | Still air, soldered on 4.25 x 1.125 inch 4-layer PCB | θ _{JA} | TBD | °C/W | |
| Thermal Resistance - Junction to Case | | θ _{JC} | 3 | °C/W | |

AC ELECTRICAL CHARACTERISTICS

(Note 5) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 5.0\text{V} \pm 5\%$)

| DESCRIPTION | SYM | -8 | | -9 | | -10 | | -12 | | UNITS | NOTES |
|-------------------------------|------------|-----|-----|-----|-----|-----|-----|-----|-----|-------|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAN | | |
| Clock | | | | | | | | | | | |
| Clock cycle time | t_{KC} | 12 | | 15 | | 15 | | 20 | | ns | |
| Clock HIGH time | t_{KH} | 4 | | 5 | | 5 | | 6 | | ns | |
| Clock LOW time | t_{KL} | 4 | | 5 | | 5 | | 6 | | ns | |
| Output Times | | | | | | | | | | | |
| Clock to output valid | t_{KQ} | | 8 | | 9 | | 10 | | 12 | ns | |
| Clock to output invalid | t_{KQX} | 3 | | 3 | | 3 | | 3 | | ns | |
| Clock to output in Low-Z | t_{KQLZ} | 5 | | 6 | | 6 | | 6 | | ns | 6,7 |
| Clock to output in High-Z | t_{KQHZ} | | 5 | | 5 | | 5 | | 6 | ns | 6,7 |
| OE to output valid | t_{OEQ} | | 5 | | 5 | | 5 | | 6 | ns | 9 |
| OE to output in Low-Z | t_{OELZ} | 0 | | 0 | | 0 | | 0 | | ns | 6,7 |
| OE to output in High-Z | t_{OEHZ} | | 5 | | 5 | | 5 | | 6 | ns | 6,7 |
| Setup Times | | | | | | | | | | | |
| Address, Controls and Data In | t_S | 2.5 | | 2.5 | | 2.5 | | 3 | | ns | 10 |
| Hold Times | | | | | | | | | | | |
| Address, Controls and Data In | t_H | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns | 10 |

CAPACITANCE DERATING

| DESCRIPTION | SYMBOL | TYP | MAX | UNITS | NOTES |
|-----------------------|-----------------|-------|-----|---------|-------|
| Clock to output valid | Δt_{KQ} | 0.016 | | ns / pF | 14 |

AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input pulse levels | 0V to 3.0V |
| Input rise and fall times | 1.5ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See Figures 1 and 2 |

OUTPUT LOADS

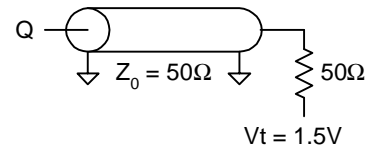


Fig. 1 OUTPUT LOAD EQUIVALENT

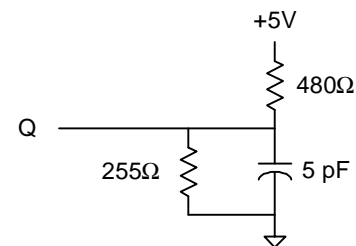
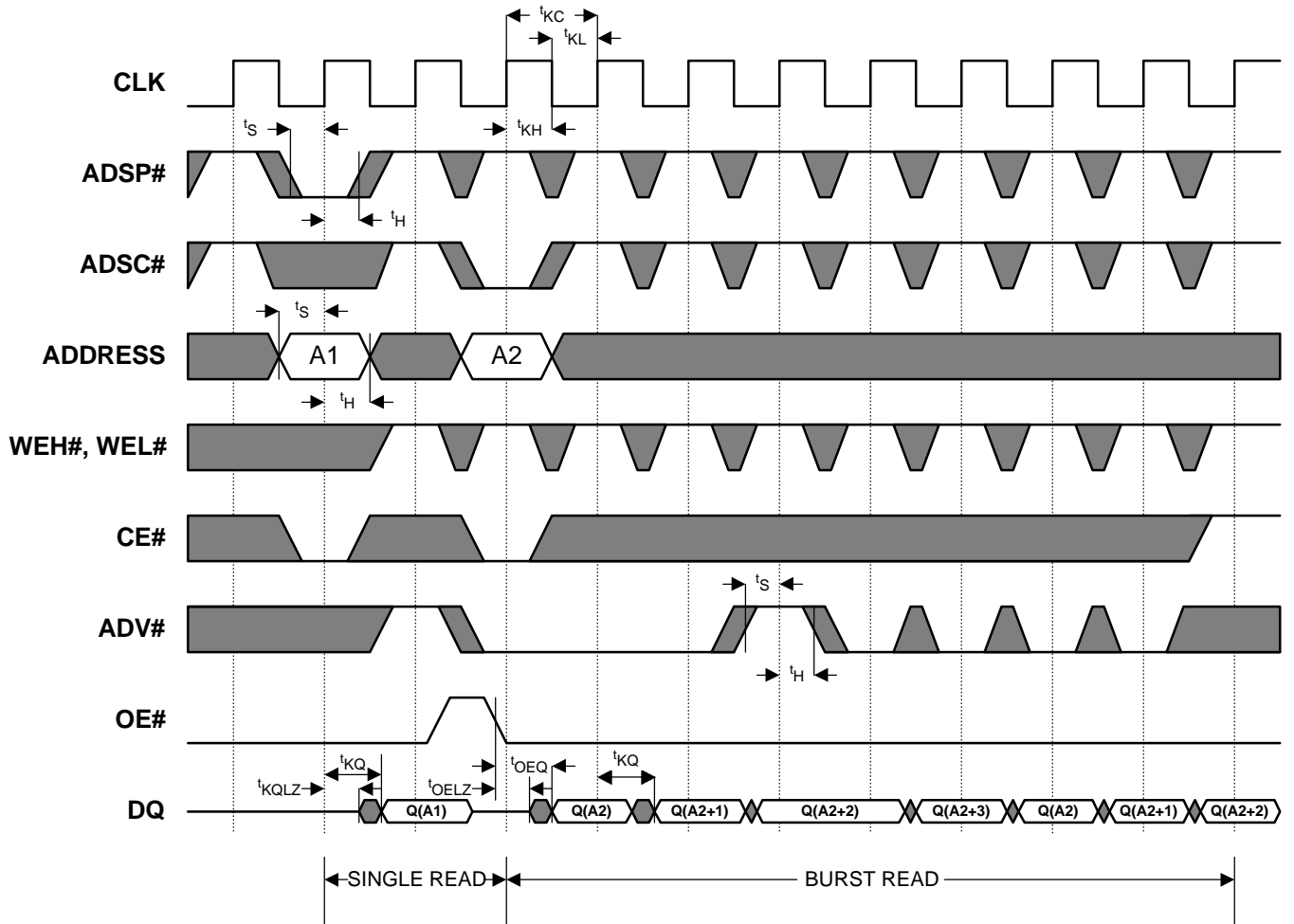


Fig. 2 OUTPUT LOAD EQUIVALENT

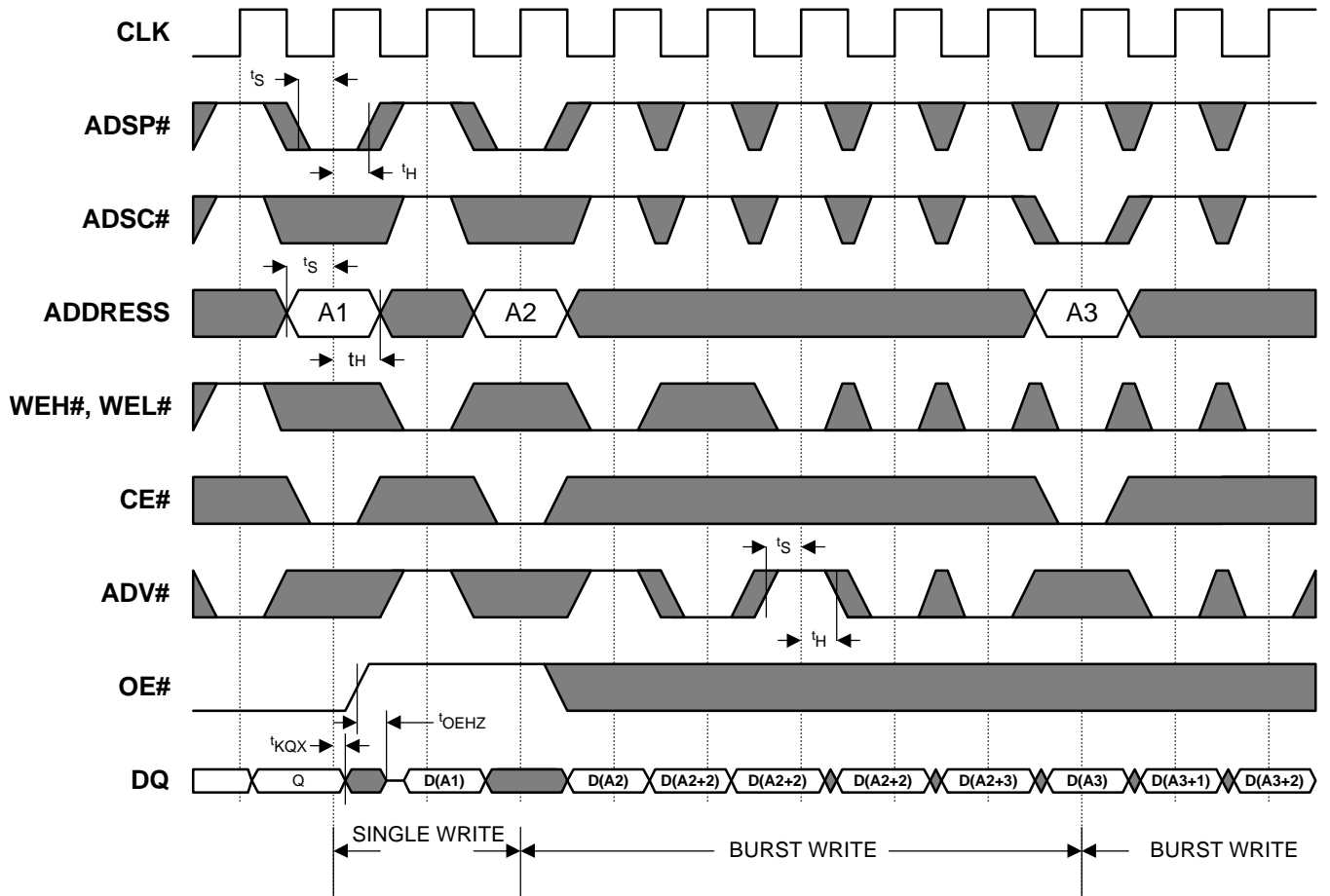
NOTES

- All voltages referenced to VSS (GND).
- Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^1K C / 2$.
Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^1K C / 2$
- I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- Output loading is specified with $CL=5pF$ as in Fig. 2.
- At any given temperature and voltage condition, 1KQHZ is less than 1KQLZ and 1OEHZ is less than 1OELZ .
- A READ cycle is defined by byte write enables all HIGH or ADSP# LOW along with chip enables being active for the required setup and hold times. A WRITE cycle is defined by at one byte or all byte WRITE per READ/WRITE TRUTH TABLE.
- OE# is a "don't care" when a byte write enable is sampled LOW.
- This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for "don't care" as defined in the truth table.
- AC I/O curves are available upon request.
- "Device Deselected" means the device is in POWER -DOWN mode as defined in the truth table. "Device Selected" means the device is active.
- Typical values are measured at 5.0V, 25°C and 20ns cycle time.
- Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.

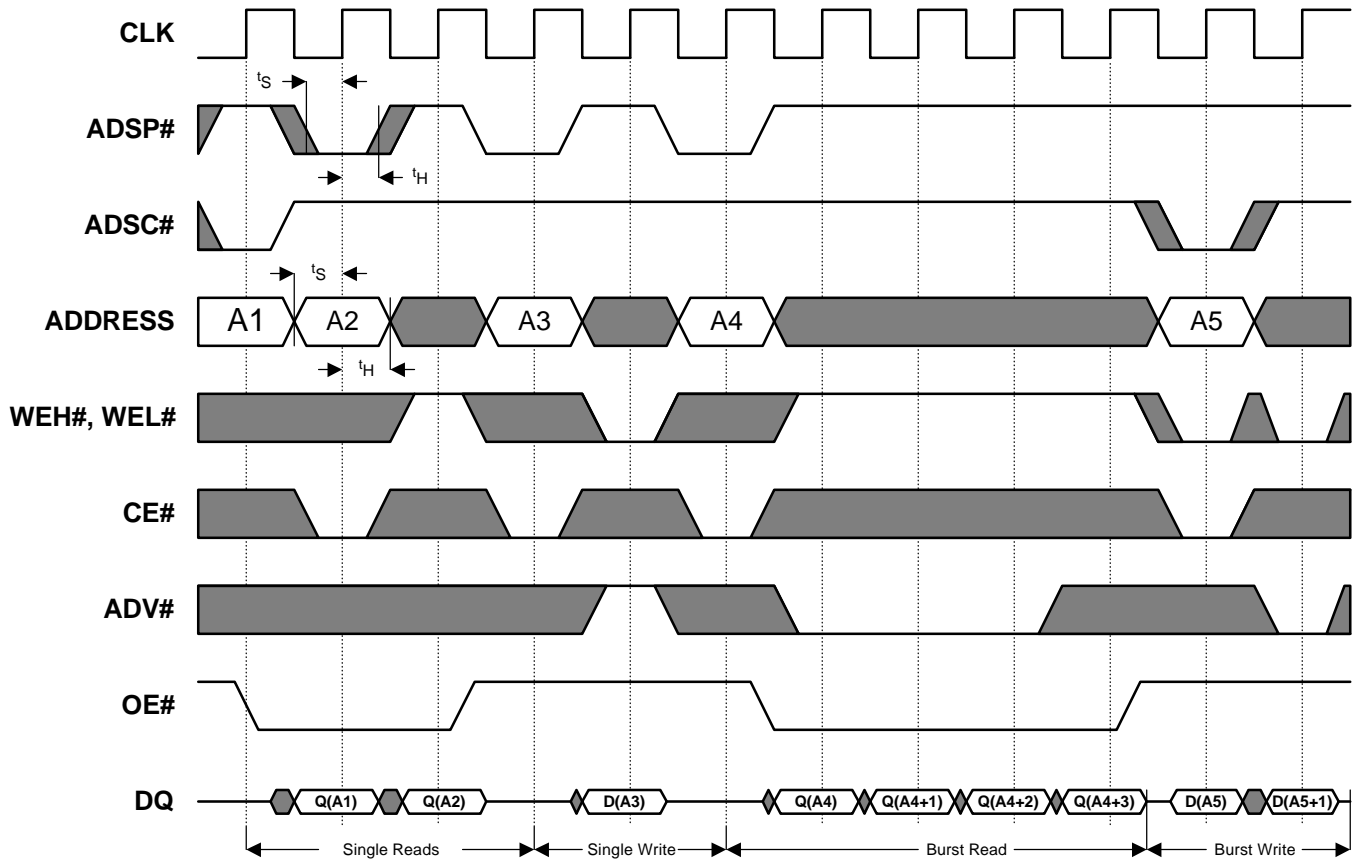
READ TIMING



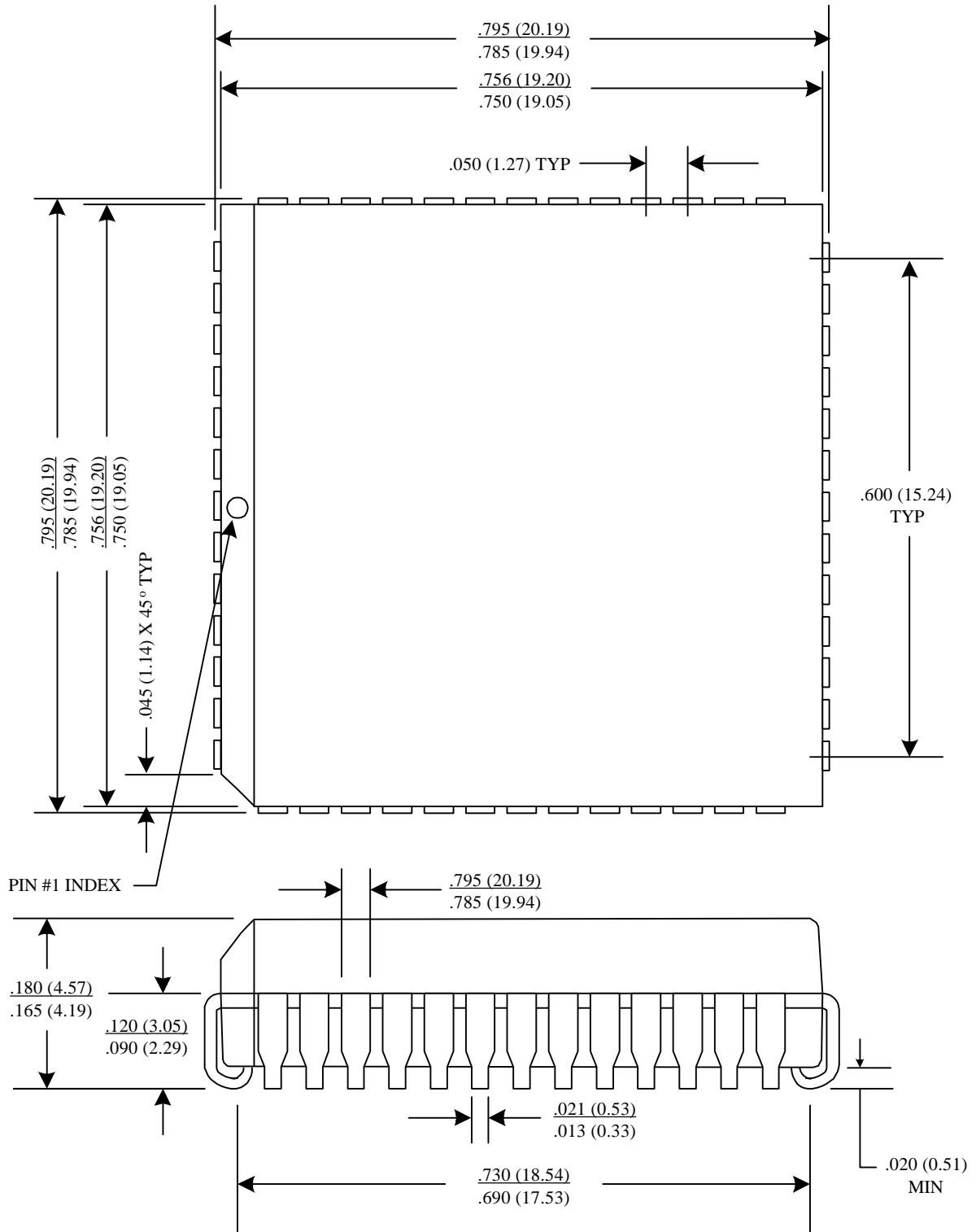
WRITE TIMING



READ/WRITE TIMING



52 Pin PLCC Package Dimensions



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Ordering Information

GVT 7164B19 X - XX

Galvantech Prefix

Part Number

Speed (8 = 8ns access/12ns cycle
9 = 9ns access/15ns cycle
10 = 10ns access/15ns cycle
12 = 12ns access/20ns cycle)

Package (C = 52 PIN PLCC)