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MH1RT

1.6M used gates Sea of Gates / Embedded

1. Description

The MH1RT Series Gate Array and Embedded Array families from TEMIC are fabricated on a radiation tolerant 0.35µ CMOS process, with up to 4 levels of metal for interconnect. This family features arrays with up to 1.6 million routable gates and 596 pins. The high density and high pin count capabilities of the MH1RT family, coupled with the ability to embed cores, or memory on the same silicon, makes the MH1RT series of arrays an ideal choice for System Level Integration.

The MH1RT series is supported by an advance software environment based on industry standards linking proprietary and commercial tools. Verilog, DFT, Sysnopsys and Vital are the reference front end tools. Floor planning associated with timing driven layout provides a short back end cycle.

The MH1RT series comes as a dual use of the MH1 series, adding:

● through process changes, the 100 MeV latch up immunity and the 200Krads+ total dose capability as required by most of the space programs,

● through cells relayout, an SEU immunity allowing to SEU harden only where it is actually necessary with respect to function requirements.

The MH1RT series comes as the TEMIC 7 th generation of ASIC series designed for radiation hardened applications in a 15 years time frame.

It is also made available to any of the currently available quality grades: commercial, industrial, automotive, military and space.

2. Features

● High Speed - 180 ps Gate Delay - 2 input NAND, FO=2 (nominal)

● Up to 1.198 M Used Gates and 512 Pins with 3.3 V, 3 V and 2.5 V Libraries when tested to space quality grades

● Up to 1.6M Used Gates and 596 Pins with 3.3 V, 3 V and 2.5 V Libraries when tested to mil quality grades

● System Level Integration Technology Cores on request:
   • MEMORY: SRAMs, TPRAMs and FIFOs; Gate Level or Embedded, with EDACS

● I/O Interfaces:
   • CMOS, LVTTL, LVDS - Output Currents up to 24 mA, 5V Tolerant and compliant I/O
   • cold sparing buffers (2 microA max. leakage current @ 3.6V worst case mil temp.)

● 300 MHz PLL, 260 MHz LVDS and 800 MHz max toggle frequency @ 3.3 V

● Deep Submicron CAD Flow

● Latch up immune and 200+ Krads total dose capability

● SEU free cell

● QML Q and V certification pending

Table 1. MHR!RT Array organization

Device Number	Max sites count	4 LM Routable Gates (Typ)	Max Pad Count	Max I/O Count	Gate Speed(1)
MH1099E	921,000	519,000	332	324	180 ps
MH1156E	1,452,000	764,000	412	404	180 ps
MH1242E	2,275,000	1,198,000	512	504	180 ps
MH1332E (2)	3,105,000	1,634,000	596	588	180 ps

1. Nominal 2 Input NAND Gate FO=2 at 3.3 volts.

2. available only when tested to mil quality grades

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3. Design

3.1 Design Systems Supported

TEMIC supports several major software systems for design with complete macro cell libraries, as well as utilities for checking the netlist and estimated pre-route delay simulations.

The following design systems are supported:

Table 2. Supported design systems

System		Available / Planned Tools
Cadence™		Pearl™ - Static Path Verilog-XL™ - Verilog Simulator Logic Design Planner™ - Floorplanner BuildGates™ - Synthesis (Ambit)
Mentor/Model Tech™		Modelsim Verilog and VHDL (VITAL) Simulator Leonardo Spectrum™ - Synthesis Velocity - Static Path
Synopsys™		VSS™ - VHDL Simulator Design Compiler™ - Synthesis Test Compiler™ - Scan Insertion and ATPG TestGen™ - Scan Insertion and ATPG VCS™ - Verilog Simulator Primetime™ - Static Path

4. Design Flow and Tools

TEMIC's design flow for Gate Arrays/Embedded Arrays is structured to allow the designer to consolidate the greatest number of system components possible onto the same silicon chip, using available third party design tools. TEMIC's cell library reflects silicon performance over extremes of temperature, voltage, and process, and includes the effects of metal loading, inter-level capacitance, and edge rise and fall times. The Design Flow includes clock tree synthesis to customer specified skew and latency goals. RC extraction is performed on final design database and incorporated into the timing analysis.

The **Typical Gate Array/Embedded Array Design Flow**, shown on page 3, provides a pictorial description of the typical interaction between TEMIC's Gate Array/Embedded Array design staff and the customer. TEMIC will deliver design kits to support the customer's synthesis, verification, floorplanning, and SCAN insertion activities. Tools such as Synopsys™, Cadence™, Verilog-HDL™ and CTgen™ are used, and many others are available. Should a design include embedded memory or an embedded core, TEMIC will support a design review with the customer. The purpose of the design review is to permit TEMIC to understand the partition of the Gate Array/Embedded Array, and define the location of the memory blocks and / or cores so that an underlayer layout model can be created.

Following a Preliminary Design Review, the design is routed, and post-route RC data is extracted. Following post-route verification and a Final Design Review, the design is taped out for fabrication.

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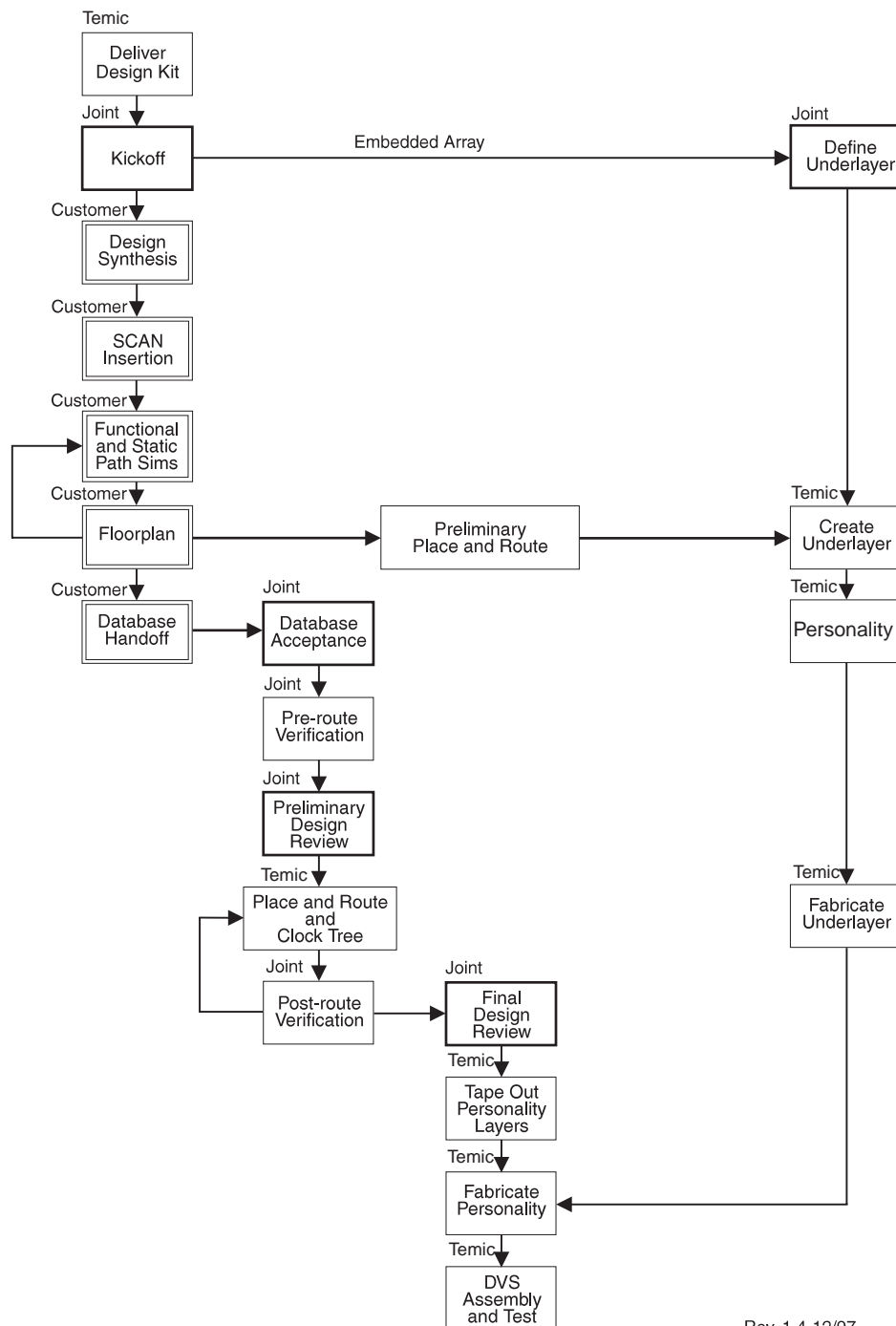
Figure 1. Typical Gate Array/Embedded Array Design Flow

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5. Pin Definition Requirements

The corner pads are reserved for Power and Ground only. All other pads are fully programmable as Input, Output, Bidirectional, Power or Ground. When implementing a design with 5 volt tolerant buffers, one buffer site must be reserved for the V_{DD5} pin, which is used to distribute power to the buffers.
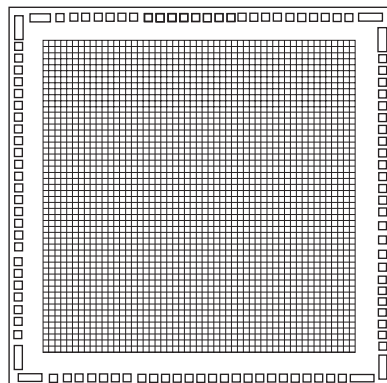
Figure 2. Gate Array
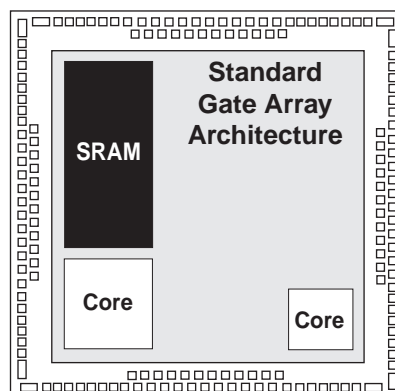
Figure 3. Embedded Array

5.1 I/O site: Pad and Sub-Sections:

The I/O sites are configurable as input, output, 3-state output and bidirectional buffers, each with pullup ur pulldown capability, if required, by utilizing their corresponding sub-section. Bidirectionnal buffers are the result of an input and output buffers placed in adjacent sub-sections in the same I/O site. Special buffers may require multiple I/O sites. Oscillators require 2 I/O sites, each power and ground pin utilizes one I/O site.

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6. Design Options

6.1 ASIC Design Translation

TEMIC has successfully translated existing designs from most major ASIC vendors (LSI Logic[TM], Motorola[TM], SMOS[TM], Oki[TM], NEC[TM], Fujitsu[TM], AMI[TM] and others) into the gate arrays. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated for a pin-for-pin compatible, drop-in replacement.

6.2 Design Entry

Design entry is performed by the customer using an TEMIC provided macro cell library. A complete netlist and vector set must then be provided to TEMIC. Upon acceptance of this data set, TEMIC continues with the standard design flow.

6.3 FPGA and PLD Conversions

TEMIC has successfully translated existing FPGA/PLD designs from most major vendors (Xilinx[TM], Actel[TM], Altera[TM], AMD[TM] and TEMIC) into the gate arrays. There are four primary reasons to convert from an FPGA/ PLD to a gate array. Conversion of high volume devices for a single or combined design is cost effective. Performance can often be optimized for speed or low power consumption. Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements. Finally, in situations where an FPGA/PLD was used for fast cycle time prototyping, a gate array may provide a lower cost answer for long-term volume production.

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7. MH1RT Series Cell Library

TEMIC's MH1RT Series gate arrays make use of an extensive library of macro cell structures, including logic cells, buffers and inverters, multiplexers, decoders, and I/O options. Soft macros are also available.

The MH1RT Series PLL operates at frequencies of up to 250MHz with minimal phase error and jitter, making it ideal for frequency synthesis of high speed on-chip clocks and chip to chip synchronization.

These cells are well characterized by use of SPICE modeling at the transistor level, with performance verified on manufactured test arrays. Characterization is performed over the rated temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product.

Table 3. Cell index

Cell Name	Description	Gate Count
ADD3X	1 bit full adder with buffered outputs	10
AND2	2 input AND	2
AND2H	2 input AND - high drive	3
AND3	3 input AND	3
AND3H	3 input AND - high drive	4
AND4	4 input AND	3
AND4H	4 input AND - high drive	4
AND5	5 input AND	5
AOI22	2 input AND into 2 input NOR	2
AOI22H	2 input AND into 2 input NOR - high drive	4
AOI222	Two, 2 input ANDs into 2 input NOR	2
AOI222H	Two, 2 input ANDs into 2 input NOR - high drive	4
AOI2223	Three, 2 input ANDs into 3 input NOR	4
AOI2223H	Three, 2 input ANDs into 3 input NOR - high drive	8
AOI23	2 input AND into 3 input NOR	3
BUF1	1x buffer	2
BUF2	2x buffer	2
BUF2T	2x Tri State bus driver with active high enable	4
BUF2Z	2x Tri State bus driver with active low enable	4
BUF3	3x buffer	3
BUF4	4x buffer	3
BUF4T	4x Tri-State bus driver with active high enable	6
BUF8	8x buffer	5
BUF8T	8x Tri-State bus driver with active high enable	10
BUF12	12x buffer	8
BUF16	16x buffer	10
CLA7X	7 input carry lookahead	5
DEC4	2:4 decoder	8
DEC4N	2:4 decoder with active low enable	10
DEC8N	3:8 decoder with active low enable	22
DFF	D flip-flop	8
DFFBCPX	D flip-flop with asynchronous clear and preset with complementary outputs	16
DFFBSRX	D flip-flop with asynchronous set and reset with complementary outputs	16
DFFC	D flip flop with asynchronous clear	9
DFFR	D flip-flop with asynchronous reset	10
DFFRQ	Quad D flip-flop with asynchronous reset	40
DFFS	D flip-flop with asynchronous set	9
DFFSR	D flip-flop with asynchronous set and reset	11
DLY1	Delay buffer 1.0 ns	6
DLY2	Delay buffer 1.5 ns	9
DLY3	Delay buffer 2.0 ns	11
DSS	Set scan flip-flop	12
DSSQ	Quad Set scan D flip-flop	36
DSSBCPY	Set scan flip-flop with clear and preset	16
DSSBR	Set scan flip-flop with reset	14
DSSBS	Set scan flip-flop with set	14

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Table 3. Cell index

Cell Name	Description	Gate Count
DSSR	Set scan D flip-flop with reset	12
DSSRQ	Quad Set Scan D flip-flop with reset	48
DSSS	Set scan D flip-flop with set	14
DSSSR	Set scan D flip-flop with set and reset	16
INV1	1x inverter	1
INV2	2x inverter	1
INV2T	2x Tri State inverter with active high enable	3
INV3	3x inverter	2
INV4	4x inverter	2
INV8	8x inverter	4
INV10	10x inverter	8
INV1D	Dual 1x inverter	2
INV1Q	Quad 1x inverter	4
INV1TQ	Quad 1x Tri State inverter with active high enable	8
JKF	JK flip-flop	10
JKFBCPX	Clear preset JK flip-flop with asynchronous clear and preset and complementary outputs	16
JKFC	JK flip-flop with asynchronous clear	12
LAT	LATCH	6
LATB	LATCH with complementary outputs	6
LATBG	LATCH with complementary outputs and inverted gate signal	6
LATBH	LATCH with high drive complementary outputs	7
LATIQ	Quad Latch	20
LATR	LATCH with reset	5
LATS	LATCH with set	6
LATSR	LATCH with set and reset	8
MUX2	2:1 MUX	4
MUX2H	2:1 MUX - high drive	5
MUX2I	2:1 MUX with inverted output	3
MUX2IH	2:1 MUX with inverted output - high drive	4
MUX2N	2:1 MUX with active low enable	5
MUX2NQ	Quad 2:1 MUX with active low enable	18
MUX2Q	Quad 2:1 MUX	16
MUX3I	3:1 MUX with inverted output	6
MUX3IH	3:1 MUX with inverted output - high drive	8
MUX4	4:1 MUX	10
MUX4X	4:1 MUX with transmission gate data inputs	9
MUX4XH	4:1 MUX with transmission gate data inputs - high drive	10
MUX5H	5:1 MUX - high drive	14
MUX8	8:1 MUX	20
MUX8N	8:1 MUX with active low enable	20
MUX8XH	8:1 MUX with transmission gate data inputs - high drive	16
NAN2	2 input NAND	2
NAN2D	Dual 2 input NAND	3
NAN2H	2 input NAND - high drive	2
NAN3	3 input NAND	2
NAN3H	3 input NAND - high drive	3
NAN4	4 input NAND	3
NAN4H	4 input NAND - high drive	4
NAN5	5 input NAND	5
NAN5H	5 input NAND - high drive	6
NAN6	6 input NAND	6
NAN6H	6 input NAND - high drive	7
NAN8	8 input NAND	7
NAN8H	8 input NAND - high drive	8
NOR2	2 input NOR	2
NOR2D	Dual 2 input NOR	3
NOR2H	2 input NOR - high drive	2
NOR3	3 input NOR	2
NOR3H	3 input NOR - high drive	3
NOR4	4 input NOR	3
NOR4H	4 input NOR - high drive	5

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Table 3. Cell index

Cell Name	Description	Gate Count
NOR5	5 input NOR	5
NOR8	8 input NOR	7
OAI22	2 input OR into 2 input NAND	2
OAI22H	2 input OR into 2 input NAND - high drive	4
OAI222	Two, 2 input ORs into 2 input NAND	3
OAI222H	Two, 2 input ORs into 2 input NAND - high drive	6
OAI22224	Four, 2 input ORs into 4 input NAND	8
OAI23	2 input OR into 3 input NAND	3
ORR2	2 input OR	2
ORR2H	2 input OR - high drive	3
ORR3	3 input OR	3
ORR3H	3 input OR - high drive	4
ORR4	4 input OR	3
ORR4H	4 input OR - high drive	4
ORR5	5 input OR	5
XNR2	2 input exclusive NOR	4
XNR2H	2 input exclusive NOR - high drive	4
XOR2	2 input exclusive OR	4
XOR2H	2 input exclusive OR - high drive	4

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Table 4. I/O Buffer Cell Index

Buffer	I/O order	Description
PIC	AI,P	CMOS input buffer, TTL compatible at 3.0V
PICH	AI,P	CMOS input buffer, TTL compatible at 3.0V, high drive
PICI	AI,P	CMOS input buffer, TTL compatible at 3.0V, inverted output
PICS	AI,P	CMOS input buffer with schmitt trigger, TTL compatible at 3.0V
PICSI	AI,P	CMOS input buffer with schmitt trigger, TTL compatible at 3.0V, inverted output
PICSV	AI,P	CMOS input buffer with schmitt trigger, TTL compatible at 3.0V, 5V tolerant
PICSV5	AI,P,VCC	CMOS input buffer with schmitt trigger, TTL compatible at 3.0V, 5V compliant
PICV	AI,P	CMOS input buffer, TTL compatible at 3.0V, 5V tolerant
PICV5	AI,P,VCC	CMOS input buffer, TTL compatible at 3.0V, 5V compliant
PID	AI,P,REF,EN	Differential input buffer
PO11	P,AO,E0	Tristate output buffer, 2mA drive
PO11F	P,AO,E0	Tristate output buffer, 2mA drive, fast slew rate control
PO11S	P,AO,E0	Tristate output buffer, 2mA drive, slow slew rate control
PO11V	P,AO,E0	Tristate output buffer, 2mA drive, 5V tolerant
PO11V5	P,AO,E0,VCC	Tristate output buffer, 2mA drive, 5V compliant
PO11VF	P,AO,E0	Tristate output buffer, 2mA drive, fast slew rate control, 5V tolerant
PO11VS	P,AO,E0	Tristate output buffer, 2mA drive, slow slew rate control, 5V tolerant
PO22	P,AO,E0	Tristate output buffer, 4mA drive
PO22F	P,AO,E0	Tristate output buffer, 4mA drive, fast slew rate control
PO22I	P,AO,E0	Tristate output buffer, 4mA drive, inverted output
PO22S	P,AO,E0	Tristate output buffer, 4mA drive, slow slew rate control
PO22V	P,AO,E0	Tristate output buffer, 4mA drive, 5V tolerant
PO22V5	P,AO,E0,VCC	Tristate output buffer, 4mA drive, 5V compliant
PO22VF	P,AO,E0	Tristate output buffer, 4mA drive, fast slew rate control, 5V tolerant
PO22VS	P,AO,E0	Tristate output buffer, 4mA drive, slow slew rate control, 5V tolerant
PO33	P,AO,E0	Tristate output buffer, 6mA drive
PO33F	P,AO,E0	Tristate output buffer, 6mA drive, fast slew rate control
PO33S	P,AO,E0	Tristate output buffer, 6mA drive, slow slew rate control
PO33V	P,AO,E0	Tristate output buffer, 6mA drive, 5V tolerant
PO33VF	P,AO,E0	Tristate output buffer, 6mA drive, fast slew rate control, 5V tolerant
PO33VS	P,AO,E0	Tristate output buffer, 6mA drive, slow slew rate control, 5V tolerant
PO44	P,AO,E0	Tristate output buffer, 8mA drive
PO44F	P,AO,E0	Tristate output buffer, 8mA drive, fast slew rate control
PO44S	P,AO,E0	Tristate output buffer, 8mA drive, slow slew rate control
PO44V	P,AO,E0	Tristate output buffer, 8mA drive, 5V tolerant
PO44V5	P,AO,E0,VCC	Tristate output buffer, 8mA drive, 5V compliant
PO44VF	P,AO,E0	Tristate output buffer, 8mA drive, fast slew rate control, 5V tolerant
PO44VS	P,AO,E0	Tristate output buffer, 8mA drive, slow slew rate control, 5V tolerant
PO55	P,AO,E0	Tristate output buffer, 10mA drive
PO55F	P,AO,E0	Tristate output buffer, 10mA drive, fast slew rate control
PO55S	P,AO,E0	Tristate output buffer, 10mA drive, slow slew rate control
PO55V	P,AO,E0	Tristate output buffer, 10mA drive, 5V tolerant
PO55VF	P,AO,E0	Tristate output buffer, 10mA drive, fast slew rate control, 5V tolerant

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Buffer	I/O order	Description
PO55VS	P,AO,E0	Tristate output buffer, 10mA drive, slow slew rate control, 5V tolerant
PO66	P,AO,E0	Tristate output buffer, 12mA drive
PO66F	P,AO,E0	Tristate output buffer, 12mA drive, fast slew rate control
PO66S	P,AO,E0	Tristate output buffer, 12mA drive, slow slew rate control
PO66V	P,AO,E0	Tristate output buffer, 12mA drive, 5V tolerant
PO66VF	P,AO,E0	Tristate output buffer, 12mA drive, fast slew rate control, 5V tolerant
PO66VS	P,AO,E0	Tristate output buffer, 12mA drive, slow slew rate control, 5V tolerant
PO77	P,AO,E0	Tristate output buffer, 14mA drive
PO77F	P,AO,E0	Tristate output buffer, 14mA drive, fast slew rate control
PO77S	P,AO,E0	Tristate output buffer, 14mA drive, slow slew rate control
PO77V	P,AO,E0	Tristate output buffer, 14mA drive, 5V tolerant
PO77VF	P,AO,E0	Tristate output buffer, 14mA drive, fast slew rate control, 5V tolerant
PO77VS	P,AO,E0	Tristate output buffer, 14mA drive, slow slew rate control, 5V tolerant
PO88	P,AO,E0	Tristate output buffer, 16mA drive
PO88F	P,AO,E0	Tristate output buffer, 16mA drive, fast slew rate control
PO88S	P,AO,E0	Tristate output buffer, 16mA drive, slow slew rate control
PO88V	P,AO,E0	Tristate output buffer, 16mA drive, 5V tolerant
PO88VF	P,AO,E0	Tristate output buffer, 16mA drive, fast slew rate control, 5V tolerant
PO88VS	P,AO,E0	Tristate output buffer, 16mA drive, slow slew rate control, 5V tolerant
PO99	P,AO,E0	Tristate output buffer, 18mA drive
PO99F	P,AO,E0	Tristate output buffer, 18mA drive, fast slew rate control
PO99S	P,AO,E0	Tristate output buffer, 18mA drive, slow slew rate control
PO99V	P,AO,E0	Tristate output buffer, 18mA drive, 5V tolerant
PO99VF	P,AO,E0	Tristate output buffer, 18mA drive, fast slew rate control, 5V tolerant
PO99VS	P,AO,E0	Tristate output buffer, 18mA drive, slow slew rate control, 5V tolerant
POAA	P,AO,E0	Tristate output buffer, 20mA drive
POAAF	P,AO,E0	Tristate output buffer, 20mA drive, fast slew rate control
POAAS	P,AO,E0	Tristate output buffer, 20mA drive, slow slew rate control
POAAV	P,AO,E0	Tristate output buffer, 20mA drive, 5V tolerant
POAAVF	P,AO,E0	Tristate output buffer, 20mA drive, fast slew rate control, 5V tolerant
POAAVS	P,AO,E0	Tristate output buffer, 20mA drive, slow slew rate control, 5V tolerant
POBB	P,AO,E0	Tristate output buffer, 22mA drive
POBBF	P,AO,E0	Tristate output buffer, 22mA drive, fast slew rate control
POBBS	P,AO,E0	Tristate output buffer, 22mA drive, slow slew rate control
POBBV	P,AO,E0	Tristate output buffer, 22mA drive, 5V tolerant
POBBVF	P,AO,E0	Tristate output buffer, 22mA drive, fast slew rate control, 5V tolerant
POBBVS	P,AO,E0	Tristate output buffer, 22mA drive, slow slew rate control, 5V tolerant
POCC	P,AO,E0	Tristate output buffer, 24mA drive
POCCF	P,AO,E0	Tristate output buffer, 24mA drive, fast slew rate control
POCCS	P,AO,E0	Tristate output buffer, 24mA drive, slow slew rate control
PRD1	P	20KOhms pull-down terminator
PRD10	P	200KOhms pull-down terminator
PRD10V5	P,VCC	200KOhms pull-down terminator, 5V compliant
PRD11	P	220KOhms pull-down terminator
PRD11V5	P,VCC	220KOhms pull-down terminator, 5V compliant

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Buffer	I/O order	Description
PRD12	P	240KOhms pull-down terminator
PRD12V5	P,VCC	240KOhms pull-down terminator, 5V compliant
PRD13	P	260KOhms pull-down terminator
PRD13V5	P,VCC	260KOhms pull-down terminator, 5V compliant
PRD14	P	280KOhms pull-down terminator
PRD14V5	P,VCC	280KOhms pull-down terminator, 5V compliant
PRD15	P	300KOhms pull-down terminator
PRD15V5	P,VCC	300K pull-down terminator, 5V compliant
PRD16	P	320KOhms pull-down terminator
PRD16V5	P,VCC	320K pull-down terminator, 5V compliant
PRD17	P	340KOhms pull-down terminator
PRD17V5	P,VCC	340K pull-down terminator, 5V compliant
PRD18	P	360KOhms pull-down terminator
PRD18V5	P,VCC	360K pull-down terminator, 5V compliant
PRD19	P	380KOhms pull-down terminator
PRD19V5	P,VCC	380K pull-down terminator, 5V compliant
PRD1V5	P,VCC	20K pull-down terminator, 5V compliant
PRD2	P	40KOhms pull-down terminator
PRD20	P	400KOhms pull-down terminator
PRD20V5	P,VCC	400K pull-down terminator, 5V compliant
PRD21	P	420KOhms pull-down terminator
PRD21V5	P,VCC	420K pull-down terminator, 5V compliant
PRD22	P	440KOhms pull-down terminator
PRD22V5	P,VCC	440K pull-down terminator, 5V compliant
PRD23	P	460KOhms pull-down terminator
PRD23V5	P,VCC	460K pull-down terminator, 5V compliant
PRD24	P	480KOhms pull-down terminator
PRD24V5	P,VCC	480K pull-down terminator, 5V compliant
PRD25	P	500KOhms pull-down terminator
PRD25V5	P,VCC	500K pull-down terminator, 5V compliant
PRD26	P	520KOhms pull-down terminator
PRD26V5	P,VCC	520K pull-down terminator, 5V compliant
PRD27	P	540KOhms pull-down terminator
PRD27V5	P,VCC	540K pull-down terminator, 5V compliant
PRD28	P	560KOhms pull-down terminator
PRD28V5	P,VCC	560K pull-down terminator, 5V compliant
PRD29	P	580KOhms pull-down terminator
PRD29V5	P,VCC	580K pull-down terminator, 5V compliant
PRD2V5	P,VCC	40K pull-down terminator, 5V compliant
PRD3	P	60KOhms pull-down terminator
PRD30	P	600KOhms pull-down terminator
PRD30V5	P,VCC	600K pull-down terminator, 5V compliant
PRD31	P	620KOhms pull-down terminator
PRD31V5	P,VCC	620K pull-down terminator, 5V compliant
PRD3V5	P,VCC	60K pull-down terminator, 5V compliant

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Buffer	I/O order	Description
PRD4	P	80KOhms pull-down terminator
PRD4V5	P,VCC	80K pull-down terminator, 5V compliant
PRD5	P	100KOhms pull-down terminator
PRD5V5	P,VCC	100K pull-down terminator, 5V compliant
PRD6	P	120KOhms pull-down terminator
PRD6V5	P,VCC	120K pull-down terminator, 5V compliant
PRD7	P	140KOhms pull-down terminator
PRD7V5	P,VCC	140K pull-down terminator, 5V compliant
PRD8	P	160KOhms pull-down terminator
PRD8V5	P,VCC	160K pull-down terminator, 5V compliant
PRD9	P	180KOhms pull-down terminator
PRD9V5	P,VCC	180K pull-down terminator, 5V compliant
PRU1	P	20KOhms pull-up terminator
PRU10	P	200KOhms pull-up terminator
PRU10V5	P,VCC	200KOhms pull-up terminator, 5V compliant
PRU11	P	220KOhms pull-up terminator
PRU11V5	P,VCC	220KOhms pull-up terminator, 5V compliant
PRU12	P	240KOhms pull-up terminator
PRU12V5	P,VCC	240KOhms pull-up terminator, 5V compliant
PRU13	P	260KOhms pull-up terminator
PRU13V5	P,VCC	260KOhms pull-up terminator, 5V compliant
PRU14	P	280KOhms pull-up terminator
PRU14V5	P,VCC	280KOhms pull-up terminator, 5V compliant
PRU15	P	300KOhms pull-up terminator
PRU15V5	P,VCC	300KOhms pull-up terminator, 5V compliant
PRU16	P	320KOhms pull-up terminator
PRU16V5	P,VCC	320KOhms pull-up terminator, 5V compliant
PRU17	P	340KOhms pull-up terminator
PRU17V5	P,VCC	340KOhms pull-up terminator, 5V compliant
PRU18	P	360KOhms pull-up terminator
PRU18V5	P,VCC	360KOhms pull-up terminator, 5V compliant
PRU19	P	380KOhms pull-up terminator
PRU19V5	P,VCC	380KOhms pull-up terminator, 5V compliant
PRU1V5	P,VCC	20KOhms pull-up terminator, 5V compliant
PRU2	P	20KOhms pull-up terminator
PRU20	P	400KOhms pull-up terminator
PRU20V5	P,VCC	400KOhms pull-up terminator, 5V compliant
PRU21	P	420KOhms pull-up terminator
PRU21V5	P,VCC	420KOhms pull-up terminator, 5V compliant
PRU22	P	440KOhms pull-up terminator
PRU22V5	P,VCC	440KOhms pull-up terminator, 5V compliant
PRU23	P	460KOhms pull-up terminator
PRU23V5	P,VCC	460KOhms pull-up terminator, 5V compliant
PRU24	P	480KOhms pull-up terminator
PRU24V5	P,VCC	480KOhms pull-up terminator, 5V compliant

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Buffer	I/O order	Description
PRU25	P	500KOhms pull-up terminator
PRU25V5	P,VCC	500KOhms pull-up terminator, 5V compliant
PRU26	P	520KOhms pull-up terminator
PRU26V5	P,VCC	520KOhms pull-up terminator, 5V compliant
PRU27	P	540KOhms pull-up terminator
PRU27V5	P,VCC	540KOhms pull-up terminator, 5V compliant
PRU28	P	560KOhms pull-up terminator
PRU28V5	P,VCC	560KOhms pull-up terminator, 5V compliant
PRU29	P	580KOhms pull-up terminator
PRU29V5	P,VCC	580KOhms pull-up terminator, 5V compliant
PRU2V5	P,VCC	40KOhms pull-up terminator, 5V compliant
PRU3	P	60KOhms pull-up terminator
PRU30	P	600KOhms pull-up terminator
PRU30V5	P,VCC	600KOhms pull-up terminator, 5V compliant
PRU31	P	620KOhms pull-up terminator
PRU31V5	P,VCC	620KOhms pull-up terminator, 5V compliant
PRU3V5	P,VCC	60KOhms pull-up terminator, 5V compliant
PRU4	P	80KOhms pull-up terminator
PRU4V5	P,VCC	80KOhms pull-up terminator, 5V compliant
PRU5	P	100KOhms pull-up terminator
PRU5V5	P,VCC	100KOhms pull-up terminator, 5V compliant
PRU6	P	120KOhms pull-up terminator
PRU6V5	P,VCC	120KOhms pull-up terminator, 5V compliant
PRU7	P	140KOhms pull-up terminator
PRU7V5	P,VCC	140KOhms pull-up terminator, 5V compliant
PRU8	P	160KOhms pull-up terminator
PRU8V5	P,VCC	160KOhms pull-up terminator, 5V compliant
PRU9	P	180KOhms pull-up terminator
PRU9V5	P,VCC	180KOhms pull-up terminator, 5V compliant
PX1L	AI,PI,GD,GU,REN	Crystal Oscillator (frequency range TBD)
PX1R	AI,PI,GD,GU,REN	Crystal Oscillator (frequency range TBD)
PX2L	AI,PI,GD,GU,REN	Crystal Oscillator (frequency range TBD)
PX3L	AI,PI,GD,GU,REN	Crystal Oscillator (frequency range TBD)
PX4L	AI,PI,GD,GU,REN	Crystal Oscillator (frequency range TBD)

Table 5. Cold sparing buffers

Cell Name	Description
PO11VZ	Tristate output buffer, 1.6mA drive, for cold sparing, V tolerant
PO11Z	Tristate output buffer, 2mA drive, for cold sparing
PO22VZ	Tristate output buffer, 3.2mA drive, for cold sparing, V tolerant
PO22Z	Tristate output buffer, 4mA drive, for cold sparing
PO33VZ	Tristate output buffer, 4.8mA drive, for cold sparing, V tolerant
PO33Z	Tristate output buffer, 6mA drive, for cold sparing
PO44VZ	Tristate output buffer, 6.4mA drive, for cold sparing, V tolerant
PO44Z	Tristate output buffer, 8mA drive, for cold sparing
PO55VZ	Tristate output buffer, 8mA drive, for cold sparing, V tolerant
PO55Z	Tristate output buffer, 10mA drive, for cold sparing

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Table 5. Cold sparing buffers

Cell Name	Description
PO66VZ	Tristate output buffer, 9.6mA drive, for cold sparing, V tolerant
PO66Z	Tristate output buffer, 12mA drive, for cold sparing
PO77VZ	Tristate output buffer, 11.2mA drive, for cold sparing, V tolerant
PO77Z	Tristate output buffer, 14mA drive, for cold sparing
PO88VZ	Tristate output buffer, 12.8mA drive, for cold sparing, V tolerant
PO88Z	Tristate output buffer, 16mA drive, for cold sparing
PO99VZ	Tristate output buffer, 14.4mA drive, for cold sparing, V tolerant
PO99Z	Tristate output buffer, 18mA drive, for cold sparing
POAAVZ	Tristate output buffer, 16mA drive, for cold sparing, V tolerant
POAAZ	Tristate output buffer, 20mA drive, for cold sparing
POBBVZ	Tristate output buffer, 17.6mA drive, for cold sparing, V tolerant
POBBZ	Tristate output buffer, 22mA drive, for cold sparing
POCCVZ	Tristate output buffer, 19.2mA drive, for cold sparing, V tolerant
POCCZ	Tristate output buffer, 24mA drive, for cold sparing

Table 6. SEU hardened cells

Cell Name	Description
HDS	SEU hardened set scan D flip-flop
HDSR	SEU hardened set scan D flip-flop with async. reset
HDSP	SEU hardened set scan D flip-flop with async. preset
HDF	SEU hardened D flip-flop
HDFR	SEU hardened D flip-flop with async. reset
HDFP	SEU hardened D flip-flop with async. preset
HLT	SEU hardened latch
HLTR	SEU hardened latch with async. reset
HTLP	SEU hardened latch with async. preset

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8. Absolute Maximum Ratings

Operating Ambient
Temperature-55˚C to +125˚C

Storage Temperature-65˚C to +150˚C

Maximum Input Voltage:

Inputs V_{DD} +0.5V

5V tolerant V_{DD5} +0.5V

Maximum Operating Voltage 3.6V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9. DC Characteristics

9.1 2.5V DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		-55	25	125	degreesC
V_{DD}	Supply Voltage	All		2.3	2.5	2.7	V
I_{IH}	Low level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD(max)}$ No Pull up	-5	1.0	5	µA
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD(max)}$, No Pull up	-5	1.0	5	µA
I_{OZ}	High-Impedance State Output Current	All	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD(max)}$, No pull up	-5	1.0	5	µA
I_{OS}	Output Short-circuit Current	PO11	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD(max)}$		9		mA
		PO11	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD(max)}$		-6		
V_{IH}	High-level Input Voltage	CMOS, LVTTL		0.7 VDD			V
		CMOS Level Schmitt		0.7 VDD	1.5		
V_{IL}	Low-level Input Voltage	CMOS				0.3 VDD	V
		CMOS Level Schmitt			1.0	0.3 VDD	
V_{OH}	High-level Output Voltage	CMOS, LVTTL	I_{OH} = as rated, $V_{DD} = V_{DD(min)}$	$0.7V_{DD}$			V
V_{OL}	Low-level Output Voltage	PO11	I_{OL} = as rated, $V_{DD} = V_{DD(min)}$			0.4	V
ICCSB	Leakage current per cell		$V_{DD} = V_{DD(max)}$		0.5		nA

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9.2 3V DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		-55	25	125	degreesC
V_{DD}	Supply Voltage	All		2.7	3.0	3.3	V
I_{IH}	Low level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD(max)}$	-5	1.0	5	μA
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD(max)}$, Pull up = 620KΩ	-5	1.0	5	μA
I_{OZ}	High-Impedance State Output Current	All	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD(max)}$, No pull up	-5	1.0	5	μA
I_{OS}	Output Short-circuit Current	PO11	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD(max)}$		14		
		PO11	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD(max)}$		-9		mA
V_{IH}	High-level Input Voltage	CMOS, LVTTL		2.0			
		CMOS Level Schmitt		2.0	1.7		V
V_{IL}	Low-level Input Voltage	CMOS				0.8	
		CMOS Level Schmitt			1.1	0.8	V
V_{OH}	High-level Output Voltage	CMOS, LVTTL	I_{OH} = as rated, $V_{DD} = V_{DD(min)}$	$0.7V_{DD}$			V
V_{OL}	Low-level Output Voltage	PO11	I_{OL} = as rated, $V_{DD} = V_{DD(min)}$			0.4	V
ICCSB	Leakage current per cell		$V_{DD} = V_{DD(max)}$		0.6	5	nA

9.3 3.3V DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		-55	25	125	degreesC
V_{DD}	Supply Voltage	All		3.0	3.3	3.6	V
I_{IH}	Low level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD(max)}$	-5	1.0	5	μA
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD(max)}$, Pull up = 620KΩ	-5	1.0	5	μA
I_{OZ}	High-Impedance State Output Current	All	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD(max)}$, No pull up	-5	1.0	5	μA
I_{OS}	Output Short-circuit Current	PO11	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD(max)}$		15		
		PO11	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD(max)}$		-10		mA
V_{IH}	High-level Input Voltage	CMOS, LVTTL		2.0			
		CMOS Level Schmitt		2.0	1.7		V
V_{IL}	Low-level Input Voltage	CMOS				0.8	
		CMOS Level Schmitt			1.1	0.8	V
V_{OH}	High-level Output Voltage	CMOS, LVTTL	I_{OH} = as rated, $V_{DD} = V_{DD(min)}$	$0.7V_{DD}$			V
V_{OL}	Low-level Output Voltage	PO11	I_{OL} = as rated, $V_{DD} = V_{DD(min)}$			0.4	V
ICCSB	Leakage current per cell		$V_{DD} = V_{DD(max)}$		0.6	5	nA

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9.4 5V DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		-55	25	125	degreesC
V_{DD}	Supply Voltage	All		2.7	3.0	3.3	V
I_{IH}	Low level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD(max)}$	-5	1.0	5	μA
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD(max)}$, Pull up = 620KΩ	-5	1.0	5	μA
I_{OZ}	High-Impedance State Output Current	All	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD(max)}$, No pull up	-5	1.0	5	μA
I_{OS}	Output Short-circuit Current	PO11	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD(max)}$		8		mA
		PO11	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD(max)}$		-7		
V_{IH}	High-level Input Voltage	CMOS, LVTTL		2.0	5.0	5.5	V
		CMOS Level Schmitt		2.0	1.7		
V_{IL}	Low-level Input Voltage	CMOS			$0.5V_{DD}$	0.8	V
		CMOS Level Schmitt			1.1	0.8	
V_{OH}	High-level Output Voltage	CMOS, LVTTL	I_{OH} = as rated, $V_{DD} = V_{DD(min)}$	$0.7V_{DD}$ $0.7V_{D5}$			V
V_{OL}	Low-level Output Voltage	PO11	I_{OL} = as rated, $V_{DD} = V_{DD(min)}$			0.4	V
ICCSB	Leakage current per cell		$V_{DD} = V_{DD(max)}$		1.0	10	nA

Table 7: I/O buffers DC characteristics

Symbol	Parameter	Test Condition	Typical	Units
C_{IN}	Capacitance, Input Buffer (die)	3 V	2.4	pF
C_{OUT}	Capacitance, Output Buffer (die)	3 V	5.6	pF
$C_{I/O}$	Capacitance, Bi-Directional	3 V	6.6	pF

10. Testability Techniques

For complex designs, involving blocks of memory and / or cores, careful attention must be given to design-for-test techniques. The sheer size of complex designs and the number of functional vectors that would need to be created to exercise them fully, strongly suggests the use of more efficient techniques. Combinations of SCAN paths, multiplexed access to memory and/or core blocks, and built-in-self-test logic must be employed, in addition to functional test patterns, to provide both the user and TEMIC the ability to test the finished product.

An example of a highly complex design could include a PLL for clock management or synthesis, a microcontroller or DSP engine or both, SRAM to support the microcontroller or DSP engine, and glue logic to support the interconnectivity of each of these blocks. The design of each of these blocks must take into consideration the fact that the manufactured device will be tested on a high performance digital tester. Combinations of parametric, functional, and structural tests, defined for digital testers, should be employed to create a suite of manufacturing tests.

The type of block dictates the type of testability technique to be employed. The PLL will, by construction, provide access to key nodes so that functional and / or parametric testing can be performed. Since a digital tester must control all the clocks during the testing of a Gate Array/Embedded Array, provision must be made for the VCO to be bypassed. TEMIC's PLLs include a multiplexing capability for just this purpose. The addition of a few pins will allow other portions of the PLL to be isolated for test, without impinging upon the normal functionality.

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In a similar vein, access to microcontroller, DSP, and SRAM blocks must be provided so that controllability and observability of the inputs and outputs to the blocks are achieved with the minimum amount of preconditioning. SRAM blocks need to provide access to both address and data ports so that comprehensive memory tests can be performed. Multiplexing I/O pins provides a method for providing this accessibility.

The glue logic can be designed using full SCAN techniques to enhance its testability.

It should be noted that, in almost all of these cases, the purpose of the testability technique is to provide TEMIC a means to assess the structural integrity of a Gate Array/Embedded Array, i.e., sort devices with manufacturing-induced defects. All of the techniques described above should be considered supplemental to a set of patterns which exercise the functionality of the design in its anticipated operating modes.

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11. Advanced Packaging

The MH1RT Series gate arrays are offered in a wide variety of standard ceramic packages, including quad flatpacks (CQFP), multi layers quad flatpacks (MQFP), pin grid arrays (CPGA) and land grid arrays (CLGA). High volume onshore and offshore contractors can provide assembly and test for commercial or industrial quality grades, when agreed. Custom package designs are also available as required to meet a customer's specific needs, and are supported through TEMIC's package design center. When a standard package cannot meet a customer's need, a package can be designed to precisely fit the application and to maintain the performance obtained in silicon. TEMIC has delivered custom-designed packages in a wide variety of configurations.

Table 8. Packaging Options

Package Type	Pin Count
PQFP (*)	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 304
Power Quad (*)	144, 160, 208, 240, 304
L/TQFP (*)	32, 44, 48, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC (*)	20, 28, 32, 44, 52, 68, 84
CPGA (**)	64, 68, 84, 100, 144, 180, 223, 391
CQFP (**)	64, 68, 84, 100, 120, 132, 144, 160, 224, 340
PBGA (*)	121, 169, 225, 313, 352, 388
Super PBGA (*)	168, 204, 240, 256, 304, 352, 432, 560, 600
MQFPF	196, 256, 352
CLGA	349, 472, 564

Note: (*) contact factory

Note: (**) not recommended for space

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