

TEMIC

TELEFUNKEN Semiconductors

TDA4455

Multistandard VIF Amplifier and PLL Demodulator

Application

Monolithic integrated circuit for vision IF signal processing in multistandard TV and VTR sets.

Description

This multistandard video IF processing circuit with PLL picture carrier regeneration gives a high performance of linear video demodulation.

With two IF inputs (Pins 1–2 and Pins 17–18), it is possible to select between two signal sources. The input selector switch (Pin 16) works independent from the standard switch (Pin 11).

The IF signal is internally fed via a 3-stage controlled wideband amplifier to the video demodulator and the phase detector. The phase detector compares the phase of IF signal (0°) with the output signal of the VCO (90°) and sets the VCO frequency accordingly. A lock detector switches the PLL loop filter according to the state of the PLL (locked-PLL slow, unlocked-PLL fast).

A second output of the VCO (0°) provides the reference carrier for the video demodulator. The polarity of the demodulator can be inverted by the standard switch (Pin 11), so that negative or positive modulated IF signals

are always available with the same polarity at the demodulator output. The demodulated video signal is filtered, amplified and fed via an interference limiter to the video output (Pin 7).

The standard switch also determines the clamp level of the video amplifier and the required IF-AGC mode. In the standard B/G mode the sync peak value is the criterion for a fast charge and discharge. In the standard L mode on the other hand, fast AGC action is achieved by charging at peak white level and discharging by the averaged video signal (time constant on Pin 8). The response level for discharge has a hysteresis. In the D2MAC mode a similar function is applied to achieve the AGC, but with different threshold levels.

An overload detector prevents the PLL becoming unlocked by large IF input signals.

To achieve a delayed tuner-AGC action, the current output (Pin 4) can be adjusted with a resistor at Pin 3.

Features

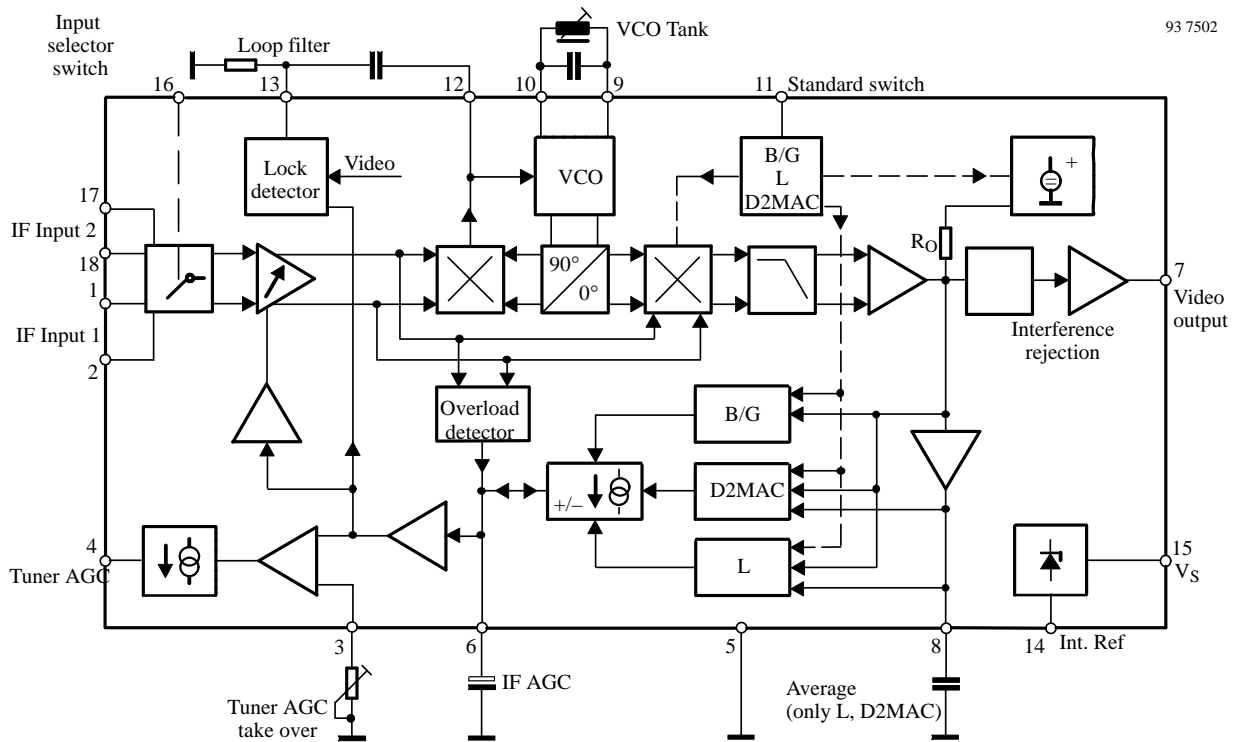
- Suitable for standard B/G, L and D2MAC, processes negative and positive modulated IF-signals with equal polarity of the output signal
- Two IF-inputs, for switching between two signal sources (e.g., two tuners and two SAW-filters)
- High performance video demodulator with PLL picture carrier regeneration
- Extended video bandwidth (12 MHz) for the demodulation of amplitude modulated MAC-signals
- Standard B/G: AGC acting on the sync peak pulse
- Standard L: fast AGC acting on peak white level with average value controlled capacitor discharge and reference hysteresis
- D2MAC: fast AGC acting on peak level with controlled capacitor discharge
- Output for delayed tuner-AGC, take over point adjustable
- High input sensitivity
- Ultra white and ultra black limiting
- Supply voltage range 6.8 to 13 V
- Low power consumption
- ESD protection

Package Options

Case: 18-pin DIL plastic



Block Diagram



Pin Description

Pin	Symbol	Function
1, 2		IF input 1
3		Tuner AGC adjustment (turn over point)
4		Delayed tuner AGC current
5, 14		Ground
6		IF AGC time constant
7		Video output
8		Video averaging for standard L and D2MAC

Pin	Symbol	Function
9, 10		VCO circuit
11		Standard switch
12		PLL loop filter
13		PLL time constant switch
15		Supply voltage
16		Input selector switch
17, 18		IF input 2

Absolute Maximum Ratings

reference point Pin 4, unless otherwise specified

Parameters	Symbol	Value	Unit
Supply voltage	V_s	6.8 to 13.0	V
Supply current	I_s	60	mA
Output current	I_{out}	5.0	mA
Maximum power dissipation	P	720	mW
Junction temperature	T_j	+125	°C
Ambient temperature	T_{amb}	-25 to +85	°C
Storage temperature	T_{stg}	-25 to +125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient (when soldered to PCB)	R_{thJA}	60	K/W

External Voltage

Pin	Voltage range *)
1, 2	$0 \leq V_{pin} \leq \min(V_s, 8 \text{ V})$
3	$0 \leq V_{pin} \leq V_s$
4	$0 \leq V_{pin} \leq \min(V_s, 10 \text{ V})$
6	$0 \leq V_{pin} \leq \min(V_s, 10 \text{ V})$
7	$0 \leq V_{pin} \leq 6 \text{ V}$
8	$0 \leq V_{pin} \leq \min(V_s, 8 \text{ V})$
9, 10	$0 \leq V_{pin} \leq V_s$
11	$0 \leq V_{pin} \leq V_s$
12	$0 \leq V_{pin} \leq \min(V_s, 7.5 \text{ V})$
13	$0 \leq V_{pin} \leq V_s$
15	$6.8 \text{ V} \leq V_{pin} \leq V_s$
16	$0 \leq V_{pin} \leq V_s$
17, 18	$0 \leq V_{pin} \leq \min(V_s, 8 \text{ V})$

*) $\min(V_s, xV)$: the lesser of the two values is the lower limit

Electrical Characteristics

$V_s = 8\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$, reference point Pin 5, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DC-supply Pin 15						
Supply voltage		V_s	6.8	8.0	13.0	V
Supply current		I_s		50	60	mA
IF-amplifier Pins 1–2 or Pins 17–18						
Input sensitivity	sync peak value, B/G	V_{in}		80	120	μV_{eff}
Input impedance		R_{in}		1.2		$\text{k}\Omega$
Input capacitance		C_{in}		2		pF
IF-AGC Pins 6 and 8						
IF gain control range		G_v	60	66		dB
Response time, standard L	Note 1	t_{AGC}			10	μsec
AGC capacitor		C_6		4.7		μF
Average capacitor		C_8		68		nF
Tuner-AGC Pins 3 and 4						
Available tuner-AGC current		I_4		4		mA
Automatic turn over point		$G_{v,\text{tun}}$		65		dB
PLL Pins 9–10, 12, 13 see note 2						
PLL capture range		Δf_{cap}		± 1.5		MHz
VCO-tuning range		Δf_{vco}		3.0		MHz
VCO-tuning sensitivity		$\Delta f / \Delta u$	3.0	4.5		kHz/mV
Video demodulator output Pin 7 see note 3						
Composite video output signal standard B/G	Note 4	V_{out}	1.8	2.0	2.2	V_{pp}
Video output signal standard L	Note 5	V_{out}	1.2	1.4	1.6	V_{pp}
Difference of the video signals	Standard B/G and L	ΔV_{out}			10	%
Ultra white level, standard B/G	Zero carrier level	V_7		4.2		V
Ultra black level, Stand. L	Zero carrier level	V_7		1.9		V
Supply voltage influence on the ultra black level (B /G)		$\Delta V/v$		0.5		%/V
Supply voltage influence on the ultra black level (L)		$\Delta V/v$		0.5		%/V
Video bandwidth (–3 dB)		B	12			MHz
Video frequency response over the AGC range		ΔB			2.0	dB
Differential gain error		ΔG		3		%
Differential phase error		$\Delta \Phi$		3		deg
Video demodulator output Pin 7						
Sound chroma beat (1.07 MHz intermodulation) related to demodulated auxiliary colour carrier.	Picture carrier = 0 dB Colour carrier = –6 dB Sound carrier = –24 dB	a_{IM}	52			dB

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
IF residual voltage f = 38.9 MHz f = 77.8 MHz		V_{res1}		2		mV
		V_{res2}		5		mV
Upsetting factor of sync pulse in the AGC range		ΔV_{sync} V_{sync}		3		%
Tilt of half picture between black and white	Standard L			5	10	%
Ultra black limiting threshold	Below sync level	ΔV_{lim1}		250		mV
Ultra white limiting threshold	Above ultra white level	ΔV_{lim2}		500		mV
Standard switch Pin 11						
Control voltage B/G	Note 6	V_{sw1}	2.5		4.0	V
Control voltage L		V_{sw2}	0		1.5	V
Control voltage D2MAC		V_{sw3}	5.0		V_s	V
Input selector switch Pin 16						
Control voltage – input 1 active	Note 7		5.0		V_s	V
Control voltage – input 2 active			0		2.5	V

Notes

1. A peak white value for at least 10 μ s must be transmitted for each complete frame
2. Loop filter: $R1 = 500 \Omega - 1 k$, $C1 = 0.47 \mu F$
Capacitor VCO circuit: $C_{VCO} = 27 - 47 pF$
3. Pin 7 unloaded
4. Residual carrier: 10% carrier amplitude
5. Blanking level: 30% carrier amplitude
6. Without control voltage at Pin 11 – standard B/G is automatically selected
7. Without control voltage at Pin 16 – input 1 is automatically active

Alignment of the VCO

1. Apply 4.5 V to Pin 6, to disable the broadband amplifier.
2. Measure the dc-voltage at Pin 12 (phase detector).
3. Apply a 38.9 MHz unmodulated carrier signal to the IF input (Pins 1–2 or Pins 17–18); adjust the input level so that the AGC voltage at Pin 6 is between 2.0 V and 2.5 V.
4. Adjust the VCO circuit until at Pin 12 is the same DC-voltage as measured in step 2.

Pin Related Internal Circuits (Continued)

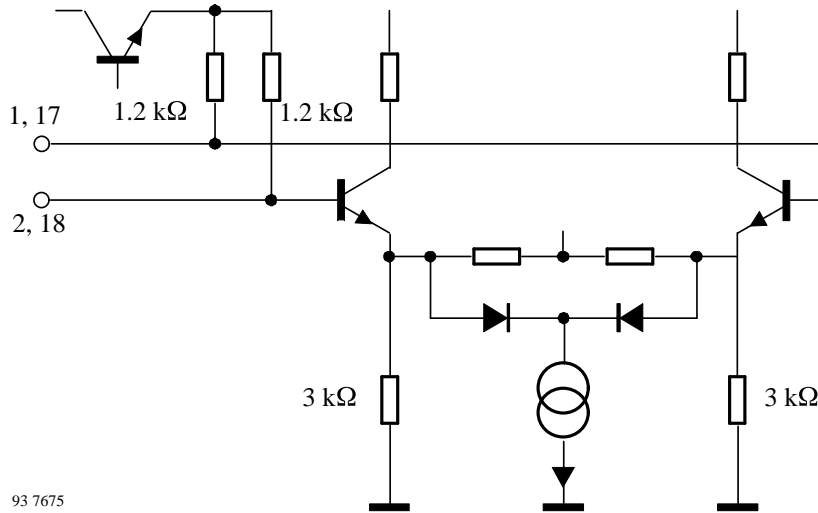


Figure 1. Pin 1-2, Pin 17-18

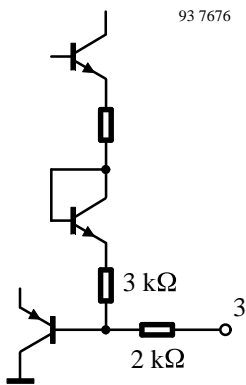


Figure 2. Pin 3

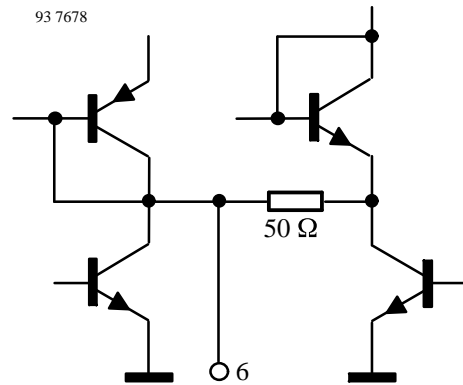


Figure 4. Pin 6

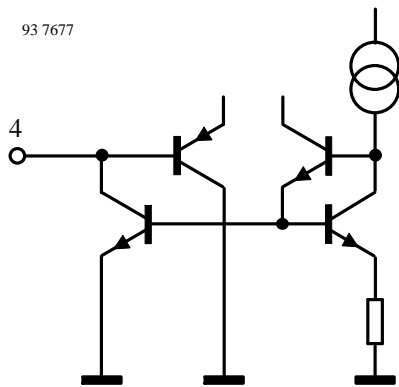


Figure 3. Pin 4

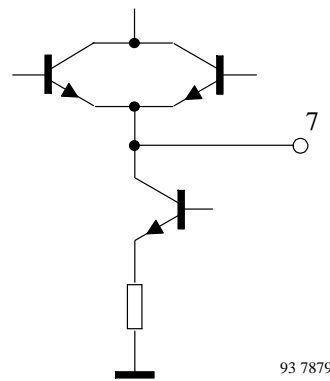


Figure 5. Pin 7

Pin Related Internal Circuits (Continued)

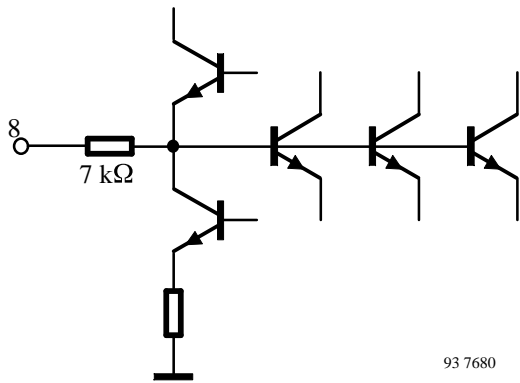


Figure 6. Pin 8

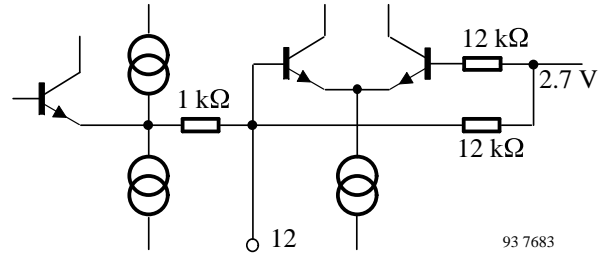


Figure 9. Pin 12

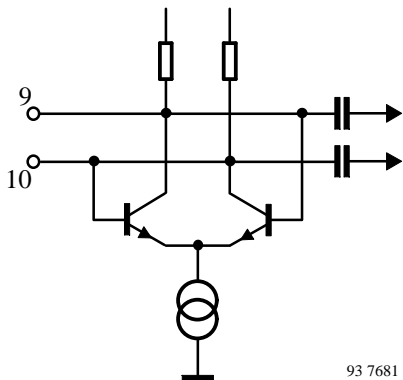


Figure 7. Pin 9-10

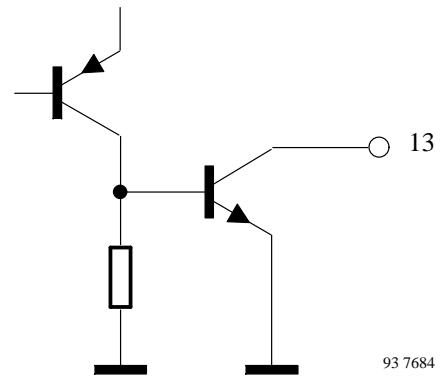


Figure 10. Pin 13

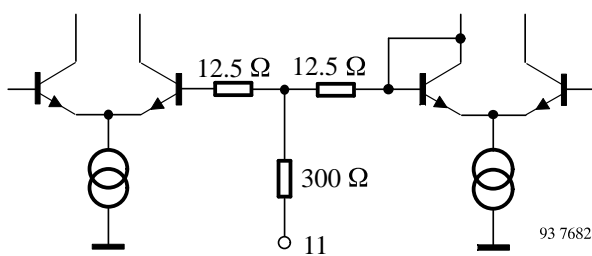


Figure 8. Pin 11

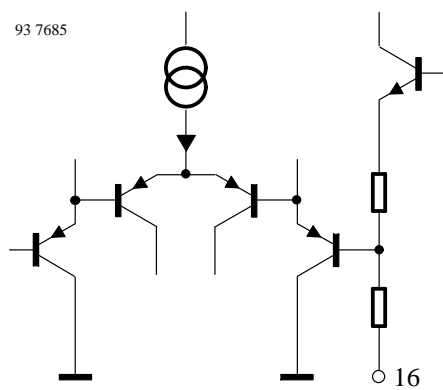


Figure 11. Pin 16

IF-AGC, Switching Thresholds

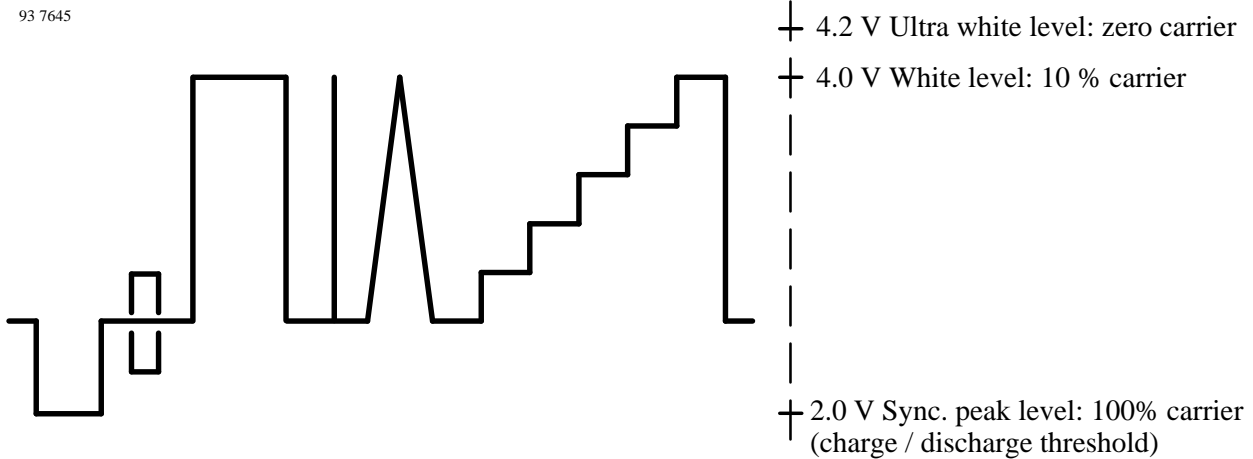


Figure 12. B/G-standard (neg. modulated)

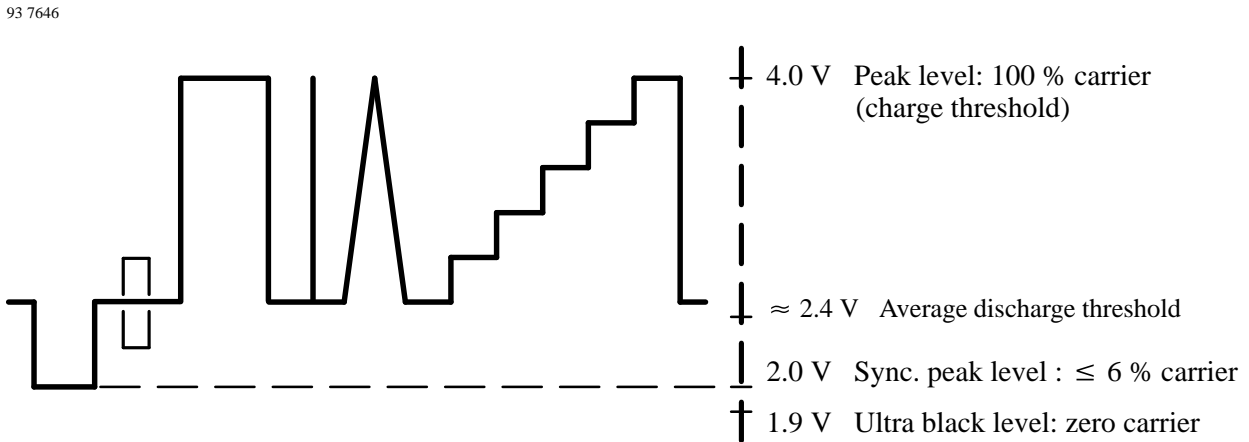


Figure 13. L-standard (pos. modulated)

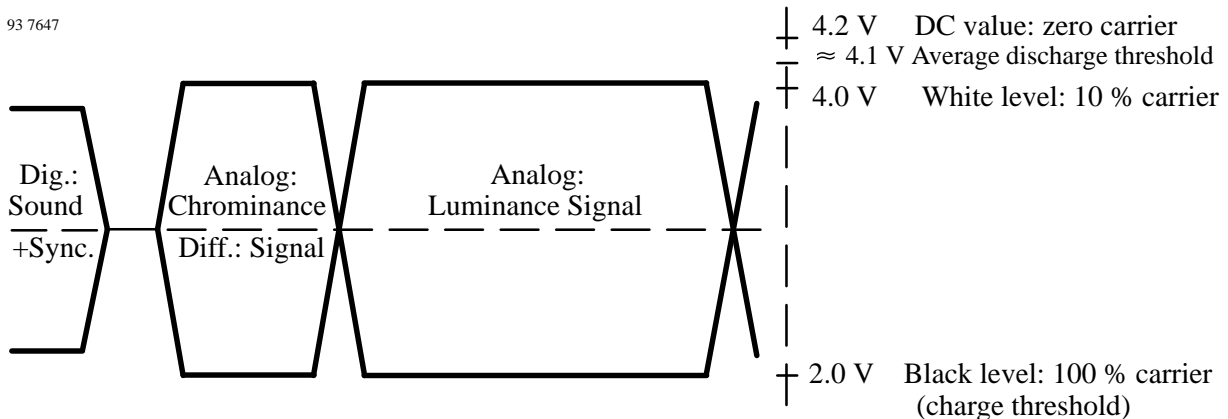
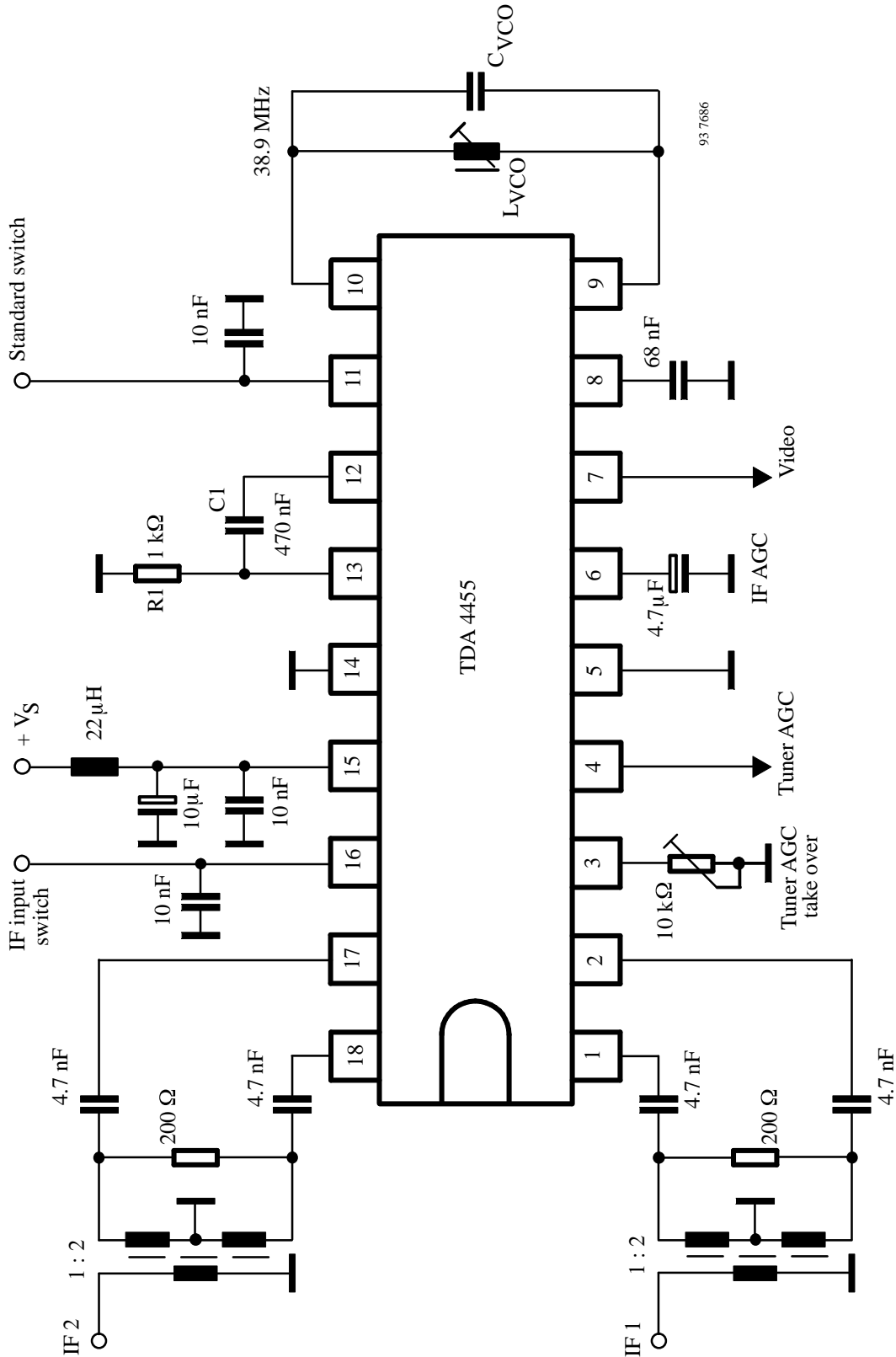


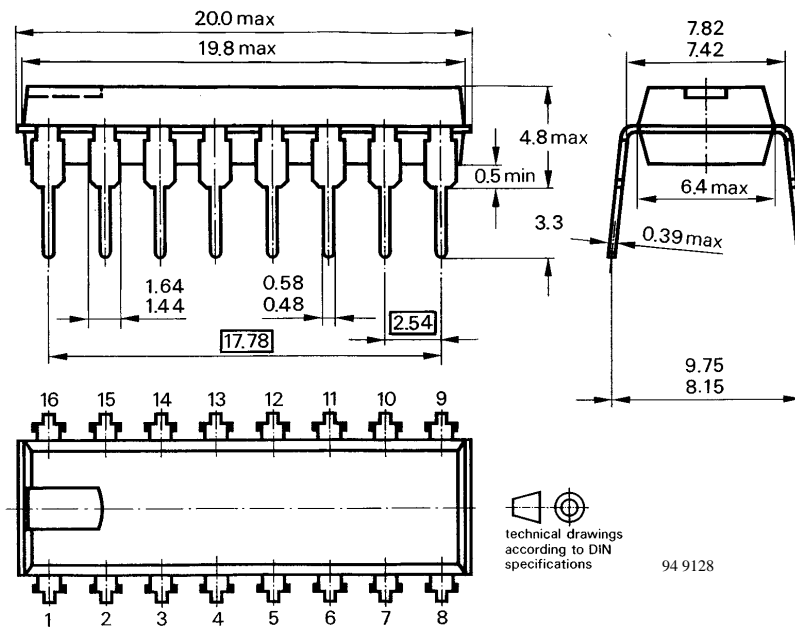
Figure 14. D2MAC-standard (neg. modulated)

Test Circuit



Dimensions in mm

Package: DIP 16



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

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