TEMIC
Semiconductors

U2758M-B

DAB Channel Decoder

Description

The channel decoder chip set for the DAB receiver consists of 4 ICs (U2758B-B, U2757M-B, a dynamic RAM 256 × 4 bit and a digital signal processor, e.g., MT DSP56166). The U2758M-B performs the program selection, de-interleaving and Viterbi decoding.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- U2758M-B supports all 4 transmission modes of EUREKA 147 DAB preliminary system definition and ETSI DAB standard (ETS 300 401)
- Processing of FIC and up to 6 application channels
- Parallel use of up to 8 U2758M with separate application selection possible
- Functions:
  - Program selection
  - Frequency, time and block de-interleaving
  - Depuncturing with **E**qual **E**rror **P**rotection (EEP) and **U**nequal **E**rror **P**rotection (UEP) profiles
  - Soft decision 384 kbit/s Viterbi decoder
  - PRBS descrambler
  - Reliability information calculation
  - CRC checksum comparison
- Interfaces:
  - Metric interface: U2757M-B interface
  - DRAM interface: 256 × 4-bit dynamic RAM
  - DAB3 interface: source decoder interface
  - L3-bus interface: microcontroller (MC) interface

Block Diagram

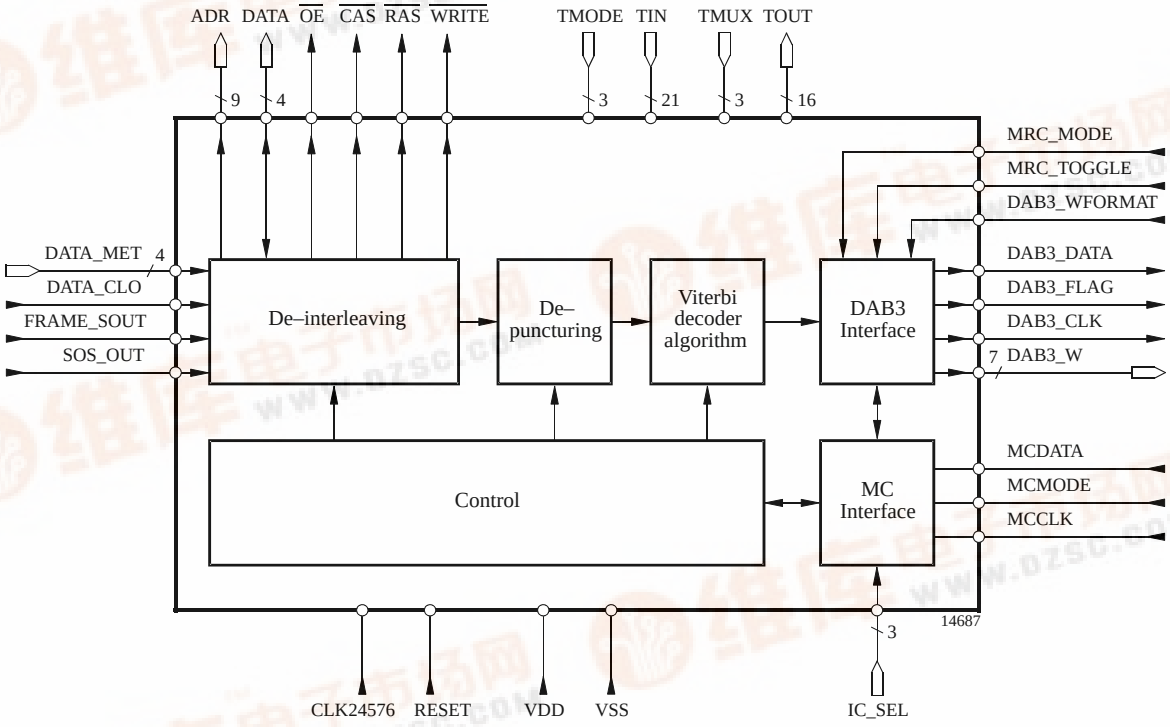

Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2758M-BFT	TQFP100	

Preliminary Information

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1 Pin Description

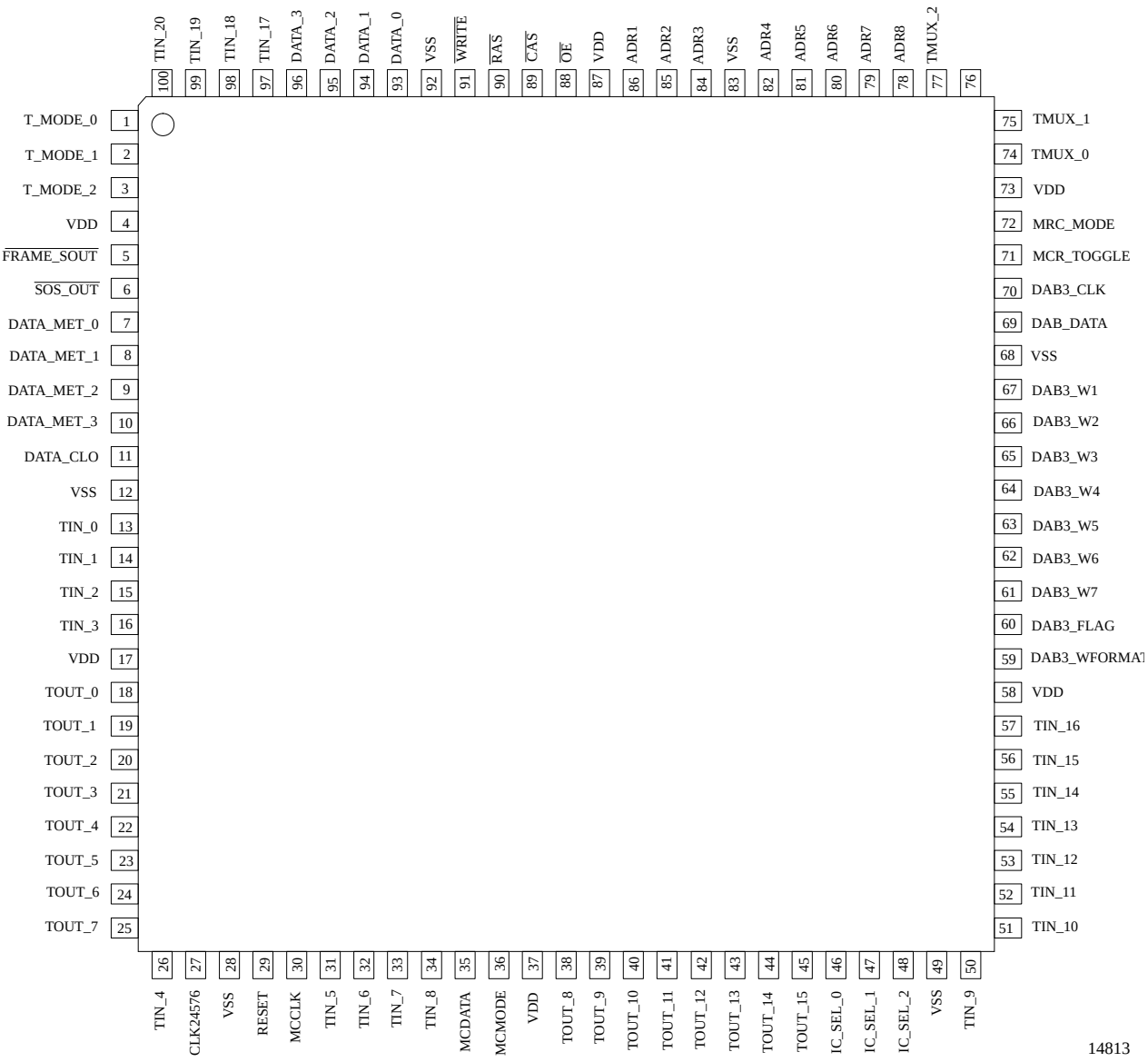


Figure 2. Pinning

Pinning (Plastic TQFP100 Thin Quad-Flat Package)

Pin	Signal	Description	PAD Type
Left Side			
1	T_MODE_0	Test mode selection bit 0 (LSB)	BINCDN
2	T_MODE_1	Test mode selection bit 1	BINCDN
3	T_MODE_2	Test mode selection bit 2 (MSB)	BINCDN
4	VDD	Power supply	
5	FRAME_SOUT	Frame synchronization signal input	BINCMOS
6	SOS_OUT	Symbol synchronization signal input	BINCMOS
7	DATA_MET_0	4-bit metric input (LSB)	BINCMOS
8	DATA_MET_1	4-bit metric input	BINCMOS
9	DATA_MET_2	4-bit metric input	BINCMOS
10	DATA_MET_3	4-bit metric input (MSB)	BINCMOS
11	DATA_CLO	Metric data clock 12.288 MHz	BINCMOS
12	VSS	Ground	
13	TIN_0	Test input bit 0	BINCDN
14	TIN_1	Test input bit 1	BINCDN
15	TIN_2	Test input bit 2	BINCDN
16	TIN_3	Test input bit 3	BINCDN
17	VDD	Power supply	
18	TOUT_0	Test output bit 0	BOUT6
19	TOUT_1	Test output bit 1	BOUT6
20	TOUT_2	Test output bit 2	BOUT6
21	TOUT_3	Test output bit 3	BOUT6
22	TOUT_4	Test output bit 4	BOUT6
23	TOUT_5	Test output bit 5	BOUT6
24	TOUT_6	Test output bit 6	BOUT6
25	TOUT_7	Test output bit 7	BOUT6
Bottom Side			
26	TIN_4	Test input bit 4	BINCDN
27	CLK24576	System clock 24.576 MHz	BTGCMOS
28	VSS	Ground	
29	RESET	Reset signal (active high)	BINCMOS
30	MCCLK	MC bus clock signal	BINCMOS
31	TIN_5	Test input bit 5	BINCDN
32	TIN_6	Test input bit 6	BINCDN
33	TIN_7	Test input bit 7	BINCDN
34	TIN_8	Test input bit 8	BINCDN
35	MCDATA	MC bus data signal	BIOC6
36	MCMODE	MC bus mode signal	BINCMOS
37	VDD	Power supply	
38	TOUT_8	Test output bit 8	BOUT6
39	TOUT_9	Test output bit 9	BOUT6
40	TOUT_10	Test output bit 10	BOUT6
41	TOUT_11	Test output bit 11	BOUT6
42	TOUT_12	Test output bit 12	BOUT6
43	TOUT_13	Test output bit 13	BOUT6
44	TOUT_14	Test output bit14	BOUT6
45	TOUT_15	Test output bit15	BOUT6
46	IC_SEL_0	IC selection Pin 0 (LSB)	BINCMOS
47	IC_SEL_1	IC selection Pin 1	BINCMOS
48	IC_SEL_2	IC selection Pin 2	BINCMOS
49	VSS	Ground	
50	TIN_9	Test input bit 9	BINCDN

Pin	Signal	Description	PAD Type
Right Side			
51	TIN_10	Test input bit 10	BINCDN
52	TIN_11	Test input bit 11	BINCDN
53	TIN_12	Test input bit 12	BINCDN
54	TIN_13	Test input bit 13	BINCDN
55	TIN_14	Test input bit 14	BINCDN
56	TIN_15	Test input bit 15	BINCDN
57	TIN_16	Test input bit 16	BINCDN
58	VDD	Power supply	
59	DAB3_WFORMAT	DAB3 window format selection	BINCDN
60	DAB3_FLAG	DAB3 error flag	B3STA6
61	DAB3_W7	DAB3 window signal 7	B3STA6
62	DAB3_W6	DAB3 window signal 6	B3STA6
63	DAB3_W5	DAB3 window signal 5	B3STA6
64	DAB3_W4	DAB3 window signal 4	B3STA6
65	DAB3_W3	DAB3 window signal 3	B3STA6
66	DAB3_W2	DAB3 window signal 2	B3STA6
67	DAB3_W1	DAB3 window signal 1	B3STA6
68	VSS	Ground	
69	DAB3_DATA	DAB3 data output	B3STA6
70	DAB3_CLK	DAB3 clock output 384 kHz	B3STA6
71	MRC_TOGGLE	Multiplex reconfiguration toggle signal	BINCDN
72	MRC_MODE	Multiplex reconfiguration mode signal	BINCDN
73	VDD	Power supply	
74	TMUX_0	Test output multiplexer bit 0 (LSB)	BINCDN
75	TMUX_1	Test output multiplexer bit 1	BINCDN
Top Side			
76	TMUX_2	Test output multiplexer bit 2 (MSB)	BINCDN
77	ADR8	External DRAM address bit 8 (MSB)	BOUT6
78	ADR7	External DRAM address bit 7	BOUT6
79	ADR6	External DRAM address bit 6	BOUT6
80	ADR5	External DRAM address bit 5	BOUT6
81	ADR4	External DRAM address bit 4	BOUT6
82	VSS	Ground	
83	ADR3	External DRAM address bit 3	BOUT6
84	ADR2	External DRAM address bit 2	BOUT6
85	ADR1	External DRAM address bit 1	BOUT6
86	ADR0	External DRAM address bit 0 (LSB)	BOUT6
87	VDD	Power	
88	$\overline{\text{OE}}$	Output enable signal for external DRAM	BOUT6
89	$\overline{\text{CAS}}$	Column address strobe for external DRAM	BOUT6
90	$\overline{\text{RAS}}$	Row address strobe for external DRAM	BOUT12
91	$\overline{\text{WRITE}}$	Read/write for external DRAM	BOUT6
92	VSS	Ground	
93	DATA_0	Data signal bit 0 of external DRAM (LSB)	BIOT6
94	DATA_1	Data signal bit 1 of external DRAM	BIOT6
95	DATA_2	Data signal bit 2 of external DRAM	BIOT6
96	DATA_3	Data signal bit 3 of external DRAM (MSB)	BIOT6
97	TIN_17	Test input bit 17	BINCDN
98	TIN_18	Test input bit 18	BINCDN
99	TIN_19	Test input bit 19	BINCDN
100	TIN_20	Test input bit 20	BINCDN

1.1 Overview of Pins

	VSS	VDD	IN	OUT	IN/OUT	
Left	1	2	14	8	0	25
Bottom	2	1	13	8	1	25
Right	1	2	12	10	0	25
Top	2	1	5	13	4	25
	6	6	44	39	5	100

2 Functional Description

2.1 De-interleaving

- Specification: ETSI DAB standard (ETS 300401)
- Input is metric result of the U2757M-B
- Bit reversal on transmission symbol level
- Frequency de-interleaving
- Time de-interleaving
  The time de-interleaved data are stored in an external 1-Mbit DRAM. If the multiplex configuration is changed, the output of the U2758M-B is invalid for 16 CIFs after the reprogramming of the U2758M-B.
- Program selection via L3 bus
  (see chapter ‘MC Bus Interface Description’)
- DRAM interface processing including DRAM refresh controller (see chapter ‘DRAM Interface Description’)
  DRAM requirements: – 256 × 4 bit configuration
  – 110 ns cycle time
  – 60 ns access time
  – 8 ms or 1 ms refresh time

2.2 Depuncturing

- Specification: ETSI DAB standard (ETS 300401)
  (see DAB standard section 11.1.2, table 31: puncturing vectors)
- Error protection profiles are selected via the MC bus
  (see chapter ‘MC Bus Interface Description’)
- **U**nequal **E**rror **P**rotection (UEP) for audio services
  (see DAB standard section 11.3.1, table 33: audio service component protection profile)
- **E**qual **E**rror **P**rotection (EEP) for data services
- Bit rates in multiples of 8 kbit/s and 32 kbit/s
  (see DAB standard section 11.3.2)

2.3 Viterbi Decoder

- 4-bit soft decision Viterbi decoder
- Constraint length 7
- Generator polynomials 133, 171, 145, 133 in octal form
- Output data clock is 384 kHz
- Reliability-information calculation using re-encoding and comparison
- Bit error flag (DAB3 interface, DAB3_FLAG) and error flag count EFC (sum of error flags per application is stored in the MC memory)
  (see chapters ‘DAB3 Interface Description’ and ‘MC Bus Interface Description’)

2.4 DAB3 Interface

- Energy dispersal (PRBS descrambling) for every application, output is DAB3_DATA
- Window signal selection
- Binary- or decimal-coded window signals
- Generation of 24 ms output frame and 384 kHz data clock burst
- Multiplex reconfiguration mode processing
  (see chapter ‘DAB3 Interface Description’)

2.5 MC Bus Interface

- Programming of the U2758M-B:
  – Application information
  – Mode information
- U2758M-B device selection via the MC bus
- MC memory delivers processing information
  (see chapter ‘MC Bus Interface Description’)
  – FIC with CRC checksum comparison in the last two bytes of every FIB
  – EFC per application
  – MC memory organisation
    – 5 ports with 32 bytes per port
    – 3 – 4 ports for FIC information
      (mode I, II:96 bytes, mode III: 128 bytes)
    – 1 port for EFC (sum of error flag bit) 2 bytes per application

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	–0.5		7	V
Input / output voltage	$V_{in/Vout}$	–0.5		V_{DD} + 0.5	V
Storage temperature	T_{stg}	–65		150	°C

3.2 Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	t.b.d.	K/W

3.3 Operating Range

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.5		5.5	V
Input / output voltage	$V_{in/Vout}$	0		V_{DD}	V
Ambient temperature	T_{amb}	–40		+85	°C
Power dissipation	P_{stat}		t.b.d.		mW
	P_{dyn}		t.b.d.		mW

3.4 DC Characteristics

The DRAM interface has TTL level, all other interfaces CMOS level

Parameter	Conditions	PAD type	Symbol	Min.	Typ.	Max.	Unit
Input HIGH voltage		BINCMOS	V_{IH}	3.5			V
		BINCDN	V_{IH}	3.5			V
		BIOC6	V_{IH}	3.5			V
		BIOT6	V_{IH}	2.0			V
Input LOW voltage		BINCMOS	V_{IL}			1.5	V
		BINCDN	V_{IL}			1.5	V
		BIOC6	V_{IL}			1.5	V
		BIOT6	V_{IL}			0.8	V
Positive threshold		BTGCMOS	V_{T+}		3.1	3.9	V
Negative threshold		BTGCMOS	V_{T-}	0.9	1.3		V
Input leakage	$V_{IN} = V_{DD}$ or V_{SS}	BINCMOS	I_L		±1	±5	µA
	$V_{IN} = V_{DD}$ or V_{SS}	BTGCMOS	I_L		±1	±5	µA
	$V_{IN} = V_{DD}$	BINCDW	I_L		40	100	µA
Output HIGH voltage	I_{OH} = +6 mA	BOUT6	V_{OH}	2.4			V
	I_{OH} = +12 mA	BOUT12	V_{OH}	2.4			V
	I_{OH} = +6 mA	BIOC6	V_{OH}	2.4			V
	I_{OH} = +6 mA	BIOT6	V_{OH}	2.4			V
	I_{OH} = +6 mA	B3STA6	V_{OH}	2.4			V
Output LOW voltage	I_{OL} = –6 mA	BOUT6	V_{OL}			0.4	V
	I_{OL} = –12 mA	BOUT12	V_{OL}			0.4	V
	I_{OL} = –6 mA	BIOC6	V_{OL}			0.4	V
	I_{OL} = –6 mA	BIOT6	V_{OL}			0.4	V
	I_{OL} = –6 mA	B3STA6	V_{OL}			0.4	V
Tristate output leakage current	$V_{OUT} = V_{DD}$ or V_{SS}	BIOC6	I_{OZ}		± 1	± 5	µA
	$V_{OUT} = V_{DD}$ or V_{SS}	BIOT6	I_{OZ}		± 1	± 5	µA
	$V_{OUT} = V_{DD}$ or V_{SS}	B3STA6	I_{OZ}		± 1	± 5	µA

4 Technical Description

4.1 General

The channel decoder of the TEMIC DAB receiver is partioned into 4 ICs. These ICs are U2757M-B (FFT, differential demodulation and metric generation), U2758M-B (program selection, de-interleaving and Viterbi decoding), a DSP, for example MT DSP56166, and a dynamic RAM 256 × 4 bit.

The following functions are available in the U2758M-B:

As defined in the ETS 300401 document, the different services consist of service components which correspond to a sub channel in the Main Service Channel. Via the MC bus, up to 7 sub-channels, including FIC processing, can be selected. FIC processing is fixed on application channel 1. Thus a maximum 7 selected sub channels or application channels will be de-interleaved, depunctured and Viterbi decoded. Afterwards, the decoded bitstream, a corresponding window signal and a reliability information is available at the DAB3 interface. For the time de-interleaver, an external DRAM is necessary to store the interleaved data of the application channels.

Whenever a mode selection or an application channel selection command is invoked by the microcontroller, the DAB3 output interface of U2758M-B in invalid for 16 CIFs.

4.2 Interface Description

The interface description is divided into four parts: metric interface description; DRAM interface description; MC bus interface description; and DAB3 interface description.

All test input and output signals are implemented with a corresponding pull-up or pull down resistor, so all test pins can be unconnected for normal application.

4.3 Metric Interface Description

The 4-bit-wide metric input interface receives the metric from the U2757M-B. The data input clock is DATA_CLO and $\overline{\text{SOS\_OUT}}$ is the window signal of the DATA_MET bus. $\overline{\text{FRAME\_SOUT}}$ is the frame synchronization input, also delivered by the U2757M.

Table 1. Metric interface signal description

Signal Name	Description
DATA_MET[3:0]	Metric input data The metric DATA_MET[3:0] of U2758M-B correspond to the 4-bit output DATA_MET[5:2] of U2757M-B. U2757M-B output — U2758M-B input U2757M-B/DATA_MET[5] — U2758M-B/DATA_MET[3] — MSB U2757M-B/DATA_MET[4] — U2758M-B/DATA_MET[2] U2757M-B/DATA_MET[3] — U2758M-B/DATA_MET[1] U2757M-B/DATA_MET[2] — U2758M-B/DATA_MET[0] — LSB These mode-dependent data arise in bit-reversed order at a data rate of DATA_CLO. For mode I 4096 values in bit reversed order are delivered by U2757M-B. For example, in mode I the first metric value belongs to the unused carrier 0, the second value to carrier 1024, the third value to carrier 512, and so on.
DATA_CLO	Input clock for DAT_MET This clock is a windowed 12.288-MHz clock, depending on the validity of DATA_MET delivered by U2757M-B.
FRAME_SOUT	Frame synchronization signal input, (active low signal) The signal defines the start of a transmission frame.The falling edge of $\overline{\text{FRAME\_SOUT}}$ is used for the synchronization of the U2758M-B delivered by U2757M-B.
SOS_OUT	Start of symbol window input signal of DATA_MET (active low signal). The signal defines the start of a symbol in a transmission frame and should be activated on the first input of each symbol. The falling edge of $\overline{\text{SOS\_OUT}}$ is used for the synchronization of the U2758M-B and is delivered by U2757M-B.

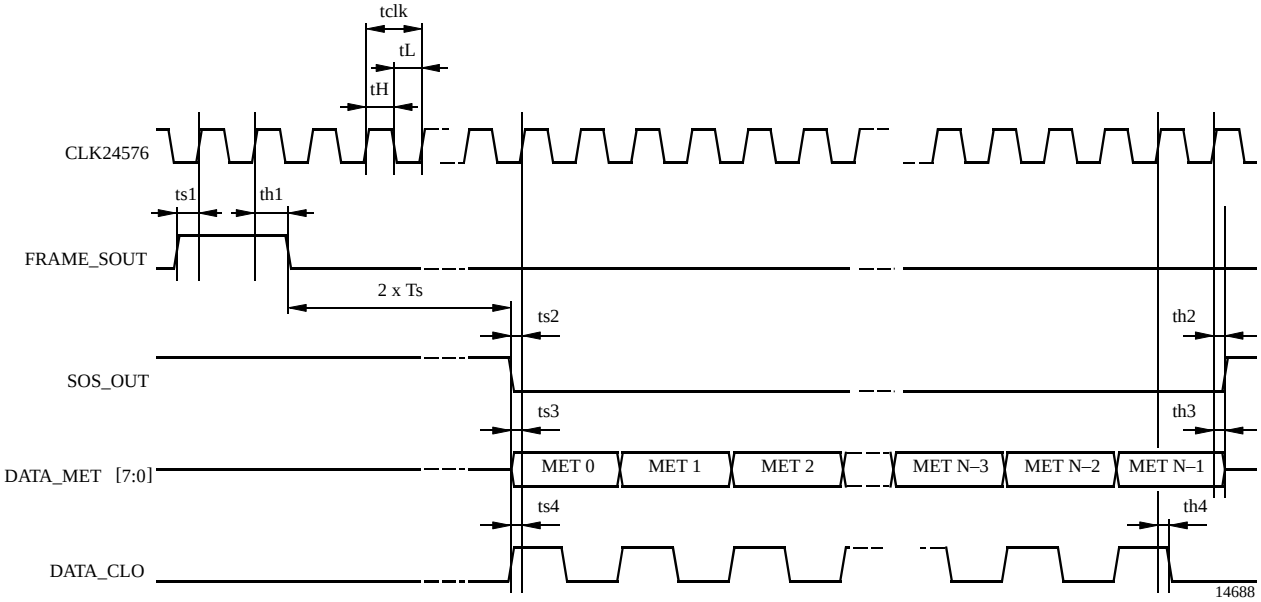


Figure 3. Metric input interface

Table 2. Metric interface setup and hold times

Parameters	Symbol	Min.	Typ.	Max.	Unit
CLK24576 clock period	tclk		40.7		ns
CLK24576 clock HIGH	tH	18.35		22.35	ns
CLK24576 clock LOW	tL	18.35		22.35	ns
Set-up time *FRAME_SOUT	ts1	0		10	ns
Hold time *FRAME_SOUT	th1	25		35	ns
Pulse width *FRAME_SOUT		1600		tguard*	ns
Set-up time *SOS_OUT	ts2	0		10	ns
Hold time *SOS_OUT	th2	25		35	ns
Se-tup time DATA_MET	ts3	–20		–10	ns
Hold time DATA_MET	th3	25		35	ns
Set-up time DATA_CLO	ts4	0		10	ns
Hold time DATA_CLO	th4	25		35	ns

* see ETS 300401 standard

4.4 DRAM Interface Description

For the time de-interleaving function an external DRAM of 1 Mbit is necessary.

The U2758M-B includes a refresh controller. Therefore, the refresh period specification of the DRAM can be down to 1 ms.

The DRAM has the following requirements:

- 262144 (256 k) words by 4-bit organization
- Min. access time 60 ns and min. cycle time 110 ns
- Refresh period min. 1 ms
- DRAM access modes: write cycle (early write), read cycle and $\overline{\text{RAS}}$ only refresh cycle

Table 3. DRAM interface signal description

Signal Name	Description
DATA[0:3] I/O	Data input / output
ADR[0:8] A	Address input
RAS	Row address strobe, active LOW signal
CAS	Column address strobe, active LOW signal
WRITE	Read / write input
OE	Output enable, active LOW signal

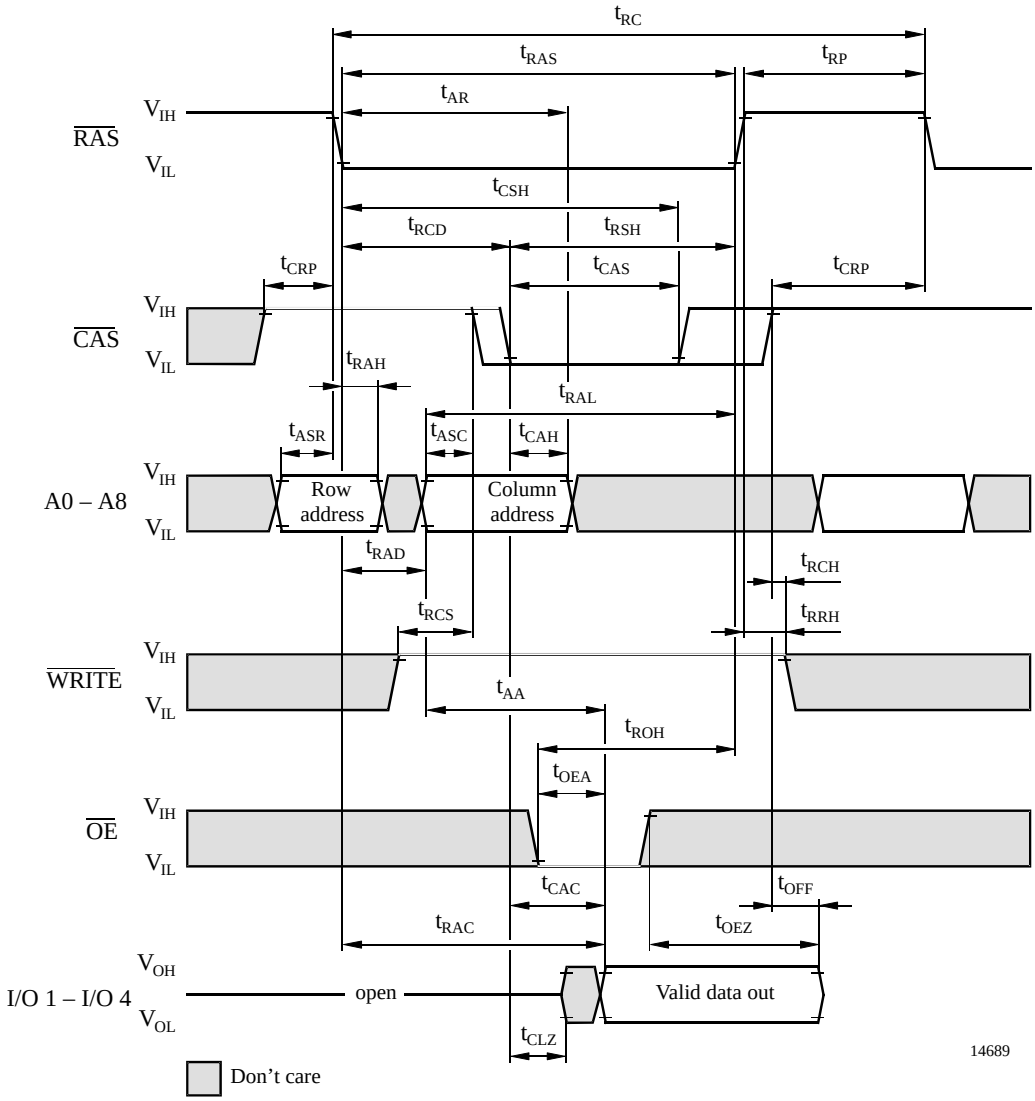


Figure 4. Read cycle

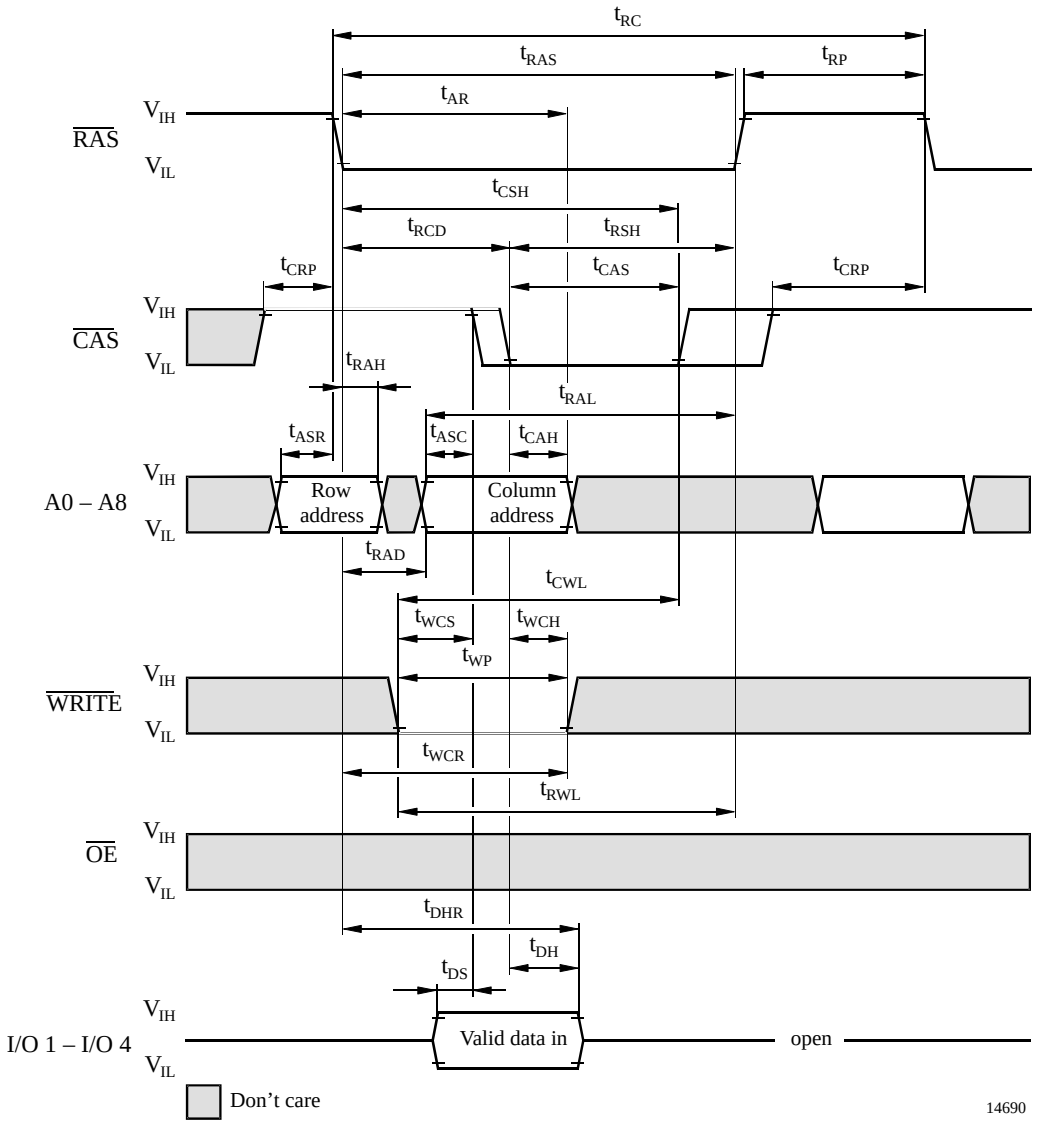


Figure 5. Write cycle (early write)

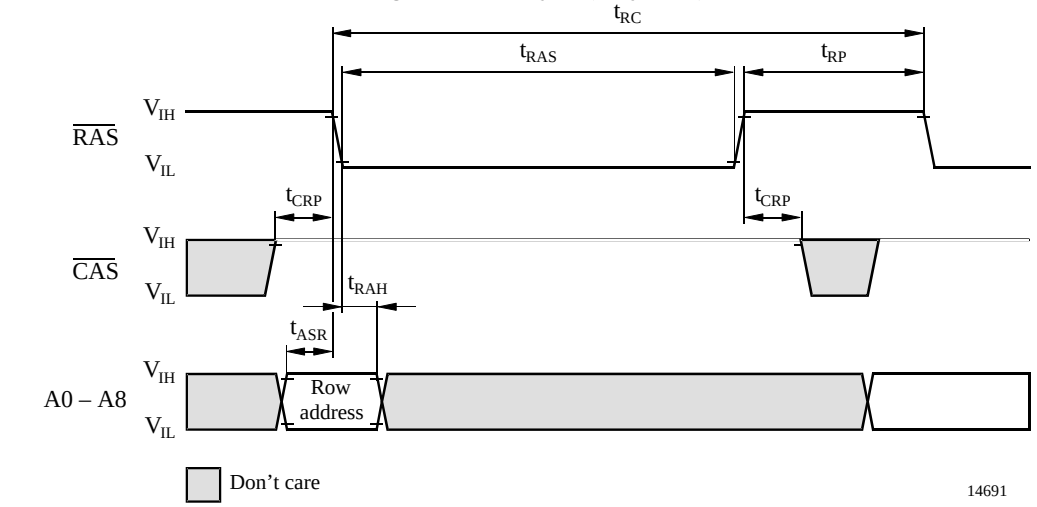


Figure 6. $\overline{\text{RAS}}$ only refresh cycle

Table 4. DRAM timing parameters

Parameter	Symbol	DRAM		U2758M			Unit
		Min.	Max.	Min.	Typ.	Max.	
Random read or write cycle time	t_{RC}	110	–		120		ns
Access time from $\overline{RAS}$	t_{RAC}	–	60				ns
Access time from $\overline{CAS}$	t_{CAC}	–	20				ns
Access time from column address	t_{AA}	–	30				ns
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–				ns
Output buffer turn-off delay	t_{OFF}	0	20				ns
$\overline{RAS}$ precharge time	t_{RP}	40	–		40		ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000		80		ns
$\overline{RAS}$ hold time	t_{RSH}	20	–		40		ns
$\overline{CAS}$ hold time	t_{CSH}	60	–		80		ns
$\overline{CAS}$ pulse width	t_{CAS}	20	10000		40		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40		40		ns
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30		20		ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–		40		ns
Row address set-up time	t_{ASR}	0	–		20		ns
Row address hold time	t_{RAH}	10	–		20		ns
Column address set-up time	t_{ASC}	0	–		20		ns
Column address hold time	t_{CAH}	15	–		40		ns
Column address hold time referred to $\overline{RAS}$	t_{AR}	50	–		80		ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–		60		ns
Read command set-up time	t_{RCS}	0	–		100		ns
Read command hold time	t_{RCH}	0	–		60		ns
Read command hold time referred to $\overline{RAS}$	t_{RRH}	0	–		60		ns
Write command hold time	t_{WCH}	15	–		20		ns
Write command hold time referred to $\overline{RAS}$	t_{WCR}	50	–		60		ns
Write command pulse width	t_{WP}	15	–		40		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–		60		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–		60		ns
Data set-up time	t_{DS}	0	–		40		ns
Data hold time	t_{DH}	15	–		40		ns
Data hold time referred to $\overline{RAS}$	t_{DHR}	50	–		80		ns
Write command set-up time	t_{WCS}	0	–		20		ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–				ns
$\overline{RAS}$ hold time referred to $\overline{OE}$	t_{ROH}	10	–		40		ns
$\overline{OE}$ access time	t_{OEA}	–	20				ns
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	20				ns

4.5 MC Bus Interface Description

This section describes the data transfer between a microcontroller and the U2758M-B.

The MCMODE signal must be set low during the RESET active period to define the use of the L3 bus. Via the MC bus interface, the microcontroller has to select the application channel, which can be either an audio or a data sub channel. Also the DAB mode has to be chosen.

The carrier shift function is not supported any longer. The MC bus interface includes a so-called MC memory which offers the possibility of accessing some processing information, like FIC (**F**ast **I**nformation **C**hannel), EFC (**E**rror **F**lag **C**ount) and the result of the comparision of the transmitted CRC signature and the on-chip calculated CRC signature of the FIC.

A set of MC commands invoke the processing which starts time aligned with the next frame synchronization input signal $\overline{\text{FRAME\_SOUT}}$ including a set-up time of approximately 0.5 ms.

The following signals are influenced by the MC bus interface:

Table 5. MC bus interface signal description

Signal Name	Description
IC_SEL[0:2]	IC selection input pins Define the number of the U2758M-B, binary coded IC_SEL[0] LSB, IC_SEL[2] MSB
MCDATA	MC bus data line for L3 bus
MCMODE	If MC_MODE = 1 during RESET active don't care If MC_MODE = 0 during RESET active L3 bus mode line
MCCLK	MC bus clock line for L3 bus

The MC bus selection is performed with the signal MCMODE during the RESET high active phase. If MCMODE is '1' during the RESET active high period, the MC interface is disabled. If MCMODE is '0' during the RESET active high period, the MC interface is configured as a L3 bus interface.

After a reset, all internal parameter are set to their default values.

4.5.1 L3 Bus Description

The L3 bus interface is a 3-wire microcontroller interface with a higher rate than other common interfaces. It allows connection of a microcontroller to several slave devices.

The signals L3MODE and L3CLK are driven by the microcontroller, L3DATA is bi-directional.

The preliminary L3 interface description offers 4 different types of instructions to handle the data transfer between a master (microcontroller) and one or several slave devices:

- Write command (command instruction)
- Read command (command instruction)
- Write data (data instruction)
- Read data (data instruction)

Table 7 describes the controlling process (mode selection and application channel selection) and the read-out process (FIC, EFC).

Table 6. L3 interface signal definition

Signal Name	Description	Microcontroller	U2758M–B (slave device)
L3MODE	Defines the operation mode LOW –> address mode HIGH –> data mode	output	input
L3CLK	Is a gated bit clock for transfer synchronization Maximum clock 2 MHz	output	input
L3DATA	Carries the transferred serial data LSB first, MSB last, Basic data transfer 8 bit byte	output / input	input / output

Table 7. L3 bus instructions
AM: address mode; HM: halt mode; DM: data mode; ( ) optional / depends on function

Controlling Device MCU –> U2758M-B			Read-Out Information U2758M-B –> MCU		
Instruction Sequence	Mode	L3 Bus Programming	Instruction Sequence	Mode	L3 Bus Programming
Write command	AM	Address byte	Read command	AM	Address byte
	(HM)			(HM)	
	DM	Data byte		DM	Data byte
Write data	AM	Address byte	Read data	AM	Address byte
	(HM)			(HM)	
	DM	Data byte 0		DM	Data byte 0
	...			HM	
	...			DM	Data byte 1
	...			...	
	(HM)			HM	
	(DM)	Data byte n		DM	Data byte 31

Table 8. Address-mode byte of command and data instruction

Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
SADR2 MSB	SADR1	SADR0 LSB	SDEV2 MSB	SDEV1	SDEV0 LSB	DOM1 MSB	DOM0 LSB

A command instruction is always followed by a data instruction. Its purpose is to identify the desired slave device on the bus, to specify the type of instruction applied and to define the type of data which are accessed by the data instruction to follow. These data can be addressed by the selection of so-called ports. All these instructions consist of an address-mode byte and one or several data-mode bytes which are marked by the L3MODE signal. In the address-mode byte system address, system-device select bit and the instruction type are specified. The data-mode byte of a command instruction consists of a single byte which characterizes the selected device and the port where those data are or have to be located, which are processed in the data instruction to follow. The data-mode byte of a data instruction consists of a defined number of bytes which contain the data to be transferred.

During **adressing mode,** a single byte is sent by the microcontroller. The structure of this byte is shown in table 8, the timing is given in figure 5.

The system address bits (SADR) indicate the DAB system, the system-device selection bits (SDEV) define the U2758M-B component and the data operation-mode bits(DOM) describe the data transfer instruction.

For DAB applications, the system address is defined as follows:

Table 9. System-address configuration

System address	SADR2	SADR1	SADR0	Comment
DAB	0	1	1	Reserved for DAB

In a DAB receiver, several system devices are accessed by a L3 bus interface.These devices can be distinguished by means of the SDEV0, SDEV, SDEV2 bits:

Table 10.DAB system-device configuration

DAB System Device	SDEV2	SDEV1	SDEV0	Comment
	0	0	0	MPEG audio source decoder
U2758M-B	0	0	1	De-interleaving, depuncturing and Viterbi decoding; This system-device address is a fixed hardware implementation.
t.b.d.	0	1	0	DAB data decoder
i.e. MT 56166	0	1	1	DSP, synchronization
tbd.	1	0	0	tbd.
tbd.	1	0	1	tbd.
tbd.	1	1	0	tbd.
tbd.	1	1	1	tbd.

Table 11.Data operation mode instructions

DOM1	DOM0	Data Operation Mode	Instruction
0	0	Data transfer from MC to U2758M	Write data
0	1	Data transfer from U2758M to MC	Read data
1	0	Register(IC) selection for write data transfer	Write command
1	1	Register(IC) selection for read data transfer	Read command

Table 12.Data-mode byte in write- or read-command instruction

Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
IC_SEL2 MSB	IC_SEL1	IC_SEL0 LSB	PORT4 MSB	PORT3	PORT2	PORT1	PORT0 LSB

The bits DOM0, DOM1 in the address byte characterize the type of instruction according to table 11. As already mentioned, the **data mode** of a command instruction consists of a single byte. Its structure is shown in table 12. An IC connected to the L3 bus reacts on the command of the microcontroller if the IC select **bits** IC_SEL0, IC_SEL1 and IC_SEL2 with the signal levels applied to the corresponding IC select **pins** IC_SEL(0:2). The bits PORT0, PORT1, PORT2, PORT3, PORT4 are used to define the port of those data which are processed in the data instruction to follow. Table 15 and 18 give an over-view of those ports which can be addressed by a write command or a read command, respectively. During data mode, the microcontroller sends or receives information to or from the U2758M-B. The L3MODE signal is high, the L3CLK signal consist of 8 pulses which indicate the 8 transferred bits. L3DATA carries the data (LSB first) and must be stable during the low phase of the L3CLK signal. To separate two transferred bytes, the interface protocol uses a so-called halt mode where the L3CLK remains high.

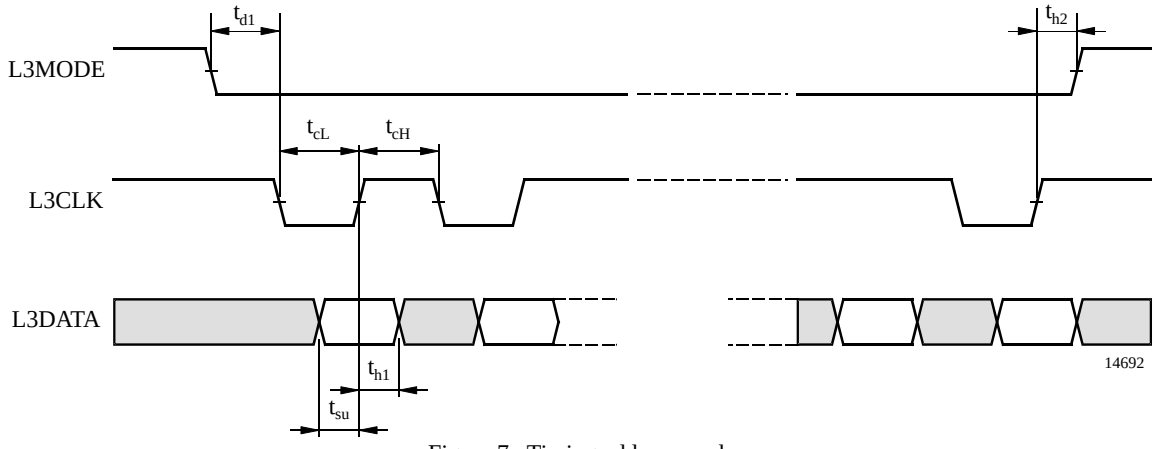


Figure 7. Timing address mode

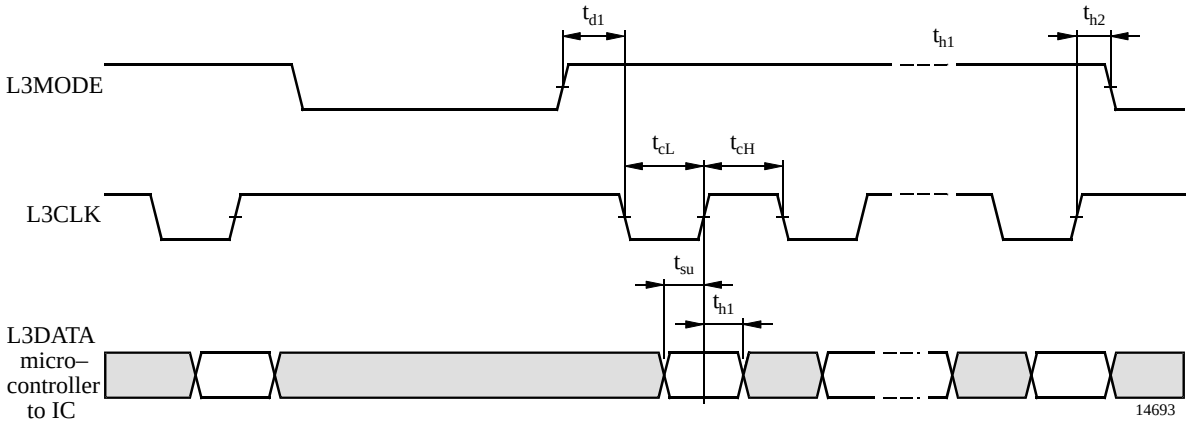


Figure 8. Timing data mode (slave receiver)

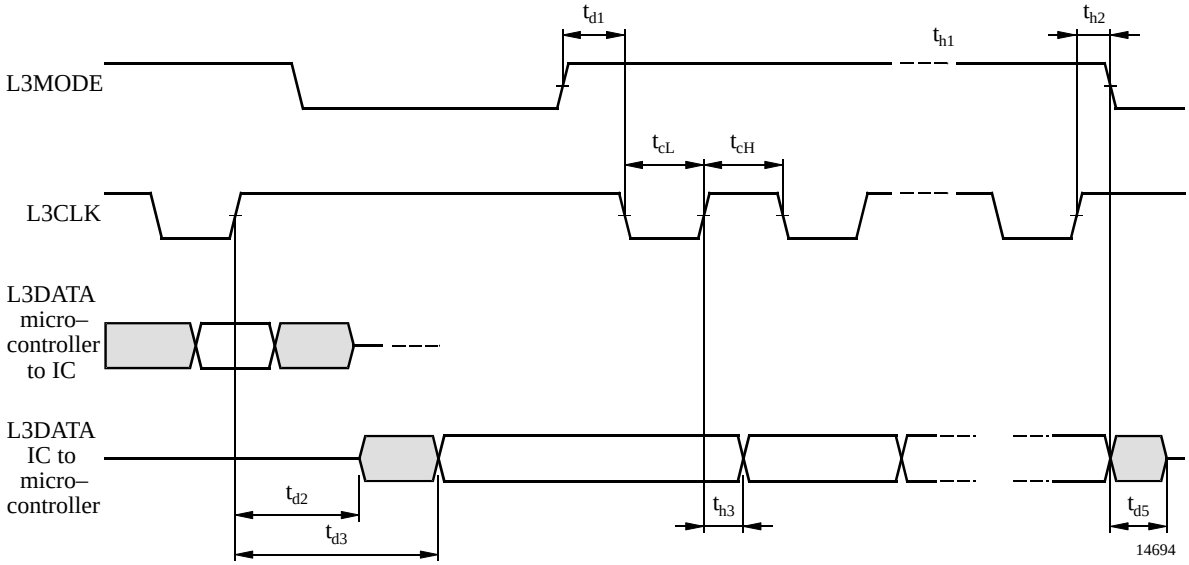


Figure 9. Timing data mode (slave transmitter)

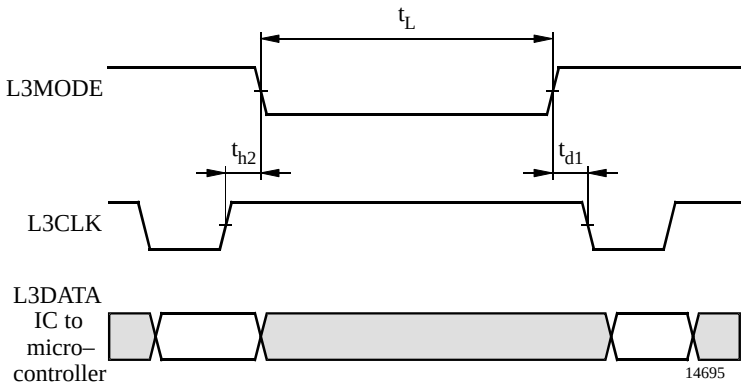


Figure 10. Timing halt mode

Table 13.L3 bus interface delay, set-up and hold times

Parameters	Symbol	Min.	Typ.	Max.	Unit
Delay time between L3MODE and L3CLK	t_{d1}		≥ 190		ns
Hold time between L3MODE and L3CLK	t_{h2}		≥ 190		ns
Low phase of L3CLK	t_{cL}		≥ 250		ns
High phase of L3CLK	t_{cH}		≥ 250		ns
Set-up time between L3CLK and L3DATA	t_{su}		≥ 190		ns
Hold time between L3CLK and L3DATA	t_{h1}		≥ 30		ns
Delay time between L3MODE and L3DATA	t_{d2}	240	300	360	ns
Delay time between L3MODE and valid L3DATA	t_{d3}	440	500	560	ns
Hold time between L3CLK and L3DATA	t_{h3}	80	100	120	ns
Delay time between L3MODE and L3DATA	t_{d5}	240	300	360	ns
L3MODE LOW time	t_L		≥ 190		ns

4.5.2 U2758M–B Operation in Parallel

In one channel decoder system, up to 8 U2758M-B can be used in parallel. They can be separately addressed by means of the data mode of a command instruction as desribed in the section “L3 Bus Description”. A typical IC selection configuration is shown in table 14.

4.5.3 Application Channel Selection

The application channel is either a UEP or an EEP sub channel. Up to 7 application channels can be programmed in one U2758M-B with a maximum data rate below 384 kHz. The FIC processing is fixed programmed on application channel 1. Depending on the selected write port address, a defined number of bytes follows. The definition of the write port addresses including these numbers are shown in table 15. The 3 data bytes, which follow the address byte in a write data instruction, depend on the chosen application.

Table 14. IC selection configuration

IC Selection	IC_SEL2	IC_SEL1	IC_SEL0	Comment
0 (even)	0	0	0	U2758M number 0
1 (odd)	0	0	1	U2758M number 1
2 (even)	0	1	0	U2758M number 2
3 (odd)	0	1	1	U2758M number 3
4 (even)	1	0	0	U2758M number 4
5 (odd)	1	0	1	U2758M number 5
6 (even)	1	1	0	U2758M number 6
7 (odd)	1	1	1	U2758M number 7

Table 15. Write port selection configuration and following byte acount

Write Port Address	PORT4	PORT3	PORT2	PORT1	PORT0	Bytes
Mode selection	0	0	0	0	0	1
FIC (fixed)	0	0	0	0	1	–
Application channel 2	0	0	0	1	0	3
Application channel 3	0	0	0	1	1	3
Application channel 4	0	0	1	0	0	3
Application channel 5	0	0	1	0	1	3
Application channel 6	0	0	1	1	0	3
Application channel 7	0	0	1	1	1	3

UEP Application

For UEP applications, the switch-on/off information, the first capacity unit C0...C9 and the corresponding unequal-error protection profile index A0...A6 must be programmed. Also the EEP or UEP selection $\overline{\text{UEP}}$/EEP must be announced as shown in table 16. For the U2758M-B the FIC is processed as application channel 1, so the application channel 1 can not be programmed by the MC.

L3 bus programming:

MSB address mode LSB

0	**1**	**1**	**0**	**0**	**1**	**1**	**0**
DAB			U2758M			write command	

MSB data mode LSB

S2	**S1**	**S0**	**P4**	**P3**	**P2**	**P1**	**P0**
IC_SEL			write port				

MSB address mode LSB

0	**1**	**1**	**0**	**0**	**1**	**0**	**0**
DAB			U2758M			write data	

MSB data mode LSB

1	**0**	**x**	**x**	**x**	**x**	**C9**	**C8**
on	$\overline{\text{UEP}}$ / EEP	x	x	x	x	MSB	CU

MSB data mode LSB

C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
CU							LSB

MSB data mode LSB

x	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
x	UEP entry address						

EEP Application

For EEP applications, the switch-on/off information and the first capacity unit number are also transferred. Additionally, EEP option, code rate and the net bit rate must be programmed by the microcontroller.

L3 bus programming:

MSB address mode LSB

0	**1**	**1**	**0**	**0**	**1**	**1**	**0**
DAB			U2758M			write command	

MSB data mode LSB

S2	**S1**	**S0**	**P4**	**P3**	**P2**	**P1**	**P0**
IC_SEL			write port				

MSB address mode LSB

0	**1**	**1**	**0**	**0**	**1**	**0**	**0**
DAB			U2758M			write data	

MSB data mode LSB

1	**1**	**x**	**x**	**x**	**O**	**C9**	**C8**
on	A / D	x	x	x	option	MSB	CU

MSB data mode LSB

C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
CU							LSB

MSB data mode LSB

R1	**R0**	**N5**	**N4**	**N3**	**N2**	**N1**	**N0**
code rate		net bit rate					

Table 16. Application channel programming for UEP and EEP sub-channels

Signal Name	Description
on	0 switch application channel off 1 switch application channel on
$\overline{\text{UEP}}$ / EEP	0 UEP application 1 EEP application
C(9:0)	First capacity unit number (**Start Address**, ETS 300 401, figure 13)
A(6:0)	UEP entry address corresponds to the **Table switch** A(6) and the **Table index** A(5:0) (ETS 300 401, table 7).
O	EEP long form **option** 0 option 0 (protection level x–A) 1 option 1 (protection level x–B)
R(1:0)	Convolutional coding rate for data application If O = 0 / If O = 1 1–A 00 code rate 2/8 — 1–B 00 code rate 4/9 2–A 01 code rate 3/8 — 2–B 01 code rate 4/7 3–A 10 code rate 4/8 — 3–B 10 code rate 4/6 4–A 11 code rate 6/8 — 4–B 11 code rate 4/5
N(5:0)	If O=0; **EEP set A**; Net bit rate in multiples of 8 kbit/s N = n–1 000000 → n × 8 kbit/s = 8 kbit/s 000001 → n × 8 kbit/s = 16 kbit/s ... N_{max} (< (384 kbit/s –Data $rate_{allAppl.Channel}$ – $Datarate_{FIC}$))/8) For mode III: 101001 → 42 × 8 kbit/s = 336 kbit/s For mode I, II and IV: 101010 → 43 × 8 kbit/s = 344 kbit/s If O=1; **EEP set B**; Net bit rate in multiples of 32 kbit/s N = n–1 000000 → n × 32 kbit/s = 32 kbit/s 000001 → n × 64 kbit/s = 64 kbit/s ... 001001 → 10 × 32 kbit/s = 320 kbit/s

The value N can be derived from the sub–channel size which is transmitted in the FIG 0/1 and Table 8 or 9 of DAB standard (ETS 300 401, Jan. 1997).

Example:

Option 0 indicates multiples of 8 kbit/s.
Protection level 3–A indicates code rate 1/2 (see table 8)
SbChSize 48 CU correspond to 48 = 6 × n (table 8) and therefore n = 48 / 6 = 8.
Further N is defined by n –1 = 7.
Data rate = n × 8 kbit/s = 64 kbit/s

4.5.4 Mode Selection

The U2758M-B supports all 4 DAB modes. The mode must be set in advance to the application channel processing. If a new mode setting is programmmed, the complete apllication-channel programming information is removed. So the mode selection can be used as an initialization procedure for the U2758M-B.

L3 bus programming:

MSB address mode LSB

0	**1**	**1**	**0**	**0**	**1**	**1**	**0**
DAB			U2758M			write command	

MSB data mode LSB

S2	**S1**	**S0**	**0**	**0**	**0**	**0**	**0**
IC_SEL			write port				

MSB address mode LSB

0	**1**	**1**	**0**	**0**	**1**	**0**	**0**
DAB			U2758M			write data	

MSB data mode LSB

M1	**M0**	**x**	**x**	**x**	**x**	**x**	**x**
M1	M0	x	x	x	x	x	x

The mode bits (M1, M0) are defined as shown in the table below:

Table 17.Mode selection

M1 (MSB)	M0 (LSB)	Mode
0	0	Mode IV
0	1	Mode I
1	0	Mode II
1	1	Mode III

4.5.5 Carrier Shift Programming

Due to the AFC function on U2757M-C, the carrier shift function is not supported any longer.

4.5.6 Microcontroller Memory (MCM) Access

During the processing of the selected application channels, some information is stored in the MC memory. A read block data transfer allows access to this memory. The MC memory has 5 ports with 32 bytes per port. A read block data transfer delivers a complete 32-byte block from the MC memory.

Table 18.Read port selection configuration and following byte account

Read Port Address	PORT4 P4	PORT3 P3	PORT2 P2	PORT1 P1	PORT0 P0	Bytes
FIB port 1	0	0	0	0	0	32
FIB port 2	0	0	0	0	1	32
FIB port 3	0	0	0	1	0	32
FIB port 4	0	0	0	1	1	32
EFC	0	0	1	0	0	32

Fast Information Channel

The size of the FIC depends on the mode and is at most 128 bytes, which correspond to 4 Fast Information Blocks (FIB). These FIBs can be read out after the corresponding DAB3 window signal, window number 1, is deactivated. Additionally, the last two bytes of every FIB in the MC memory, not at the serial DAB3 interface, are replaced by the comparison of the received CRC signature and the recalculated CRC signature inside the U2758M-B. For FIC verification, these last two bytes indicate a correct transmisson at an early stage. If these two bytes are all zero, the received FIC information is correct.

The order of the FIB bytes corresponds to the serial DAB3_DATA output. For example, the DAB3_DATA index for mode I (3 FIBs = 3 x 32 byte = 96 x 8 bit = 768 bit) is from 0 (first output) up to 767 (last serial output bit). These data are stored in the MC memory as FIB1 (first 32 bytes) at port 1, FIB2 (second 32 bytes) at port 2 and FIB3 (third 32 bytes) at port 3. The byte 0 (0:7) of the port 1 (FIB1) corresponds to index 0 to 7, byte 1 to index 8 to 15 and so on.

L3 bus programming:

MSB address mode LSB

0	**1**	**1**	**0**	**0**	**1**	**1**	**0**
DAB			U2758M			read command	

MSB data mode LSB

S2	**S1**	**S0**	**P4**	**P3**	**P2**	**P1**	**P0**
IC_SEL			read port				

MSB address mode LSB

0	**1**	**1**	**0**	**0**	**1**	**0**	**0**
DAB			U2758M			read data	

MSB data mode LSB

FIC	**FIC**	**FIC**	**FIC**	**FIC**	**FIC**	**FIC**	**FIC**
index7			byte 0				index0

MSB data mode LSB

FIC	**FIC**	**FIC**	**FIC**	**FIC**	**FIC**	**FIC**	**FIC**
index15			byte 1				index8

• • •

MSB data mode LSB

FIC	**FIC**	**FIC**	**FIC**	**FIC**	**FIC**	**FIC**	**FIC**
byte 31							

32 bytes delivered by U2758M-B

Error Flag Count

Furthermore, the MC memory includes the sum of error flags per application. This result is achieved by summing up the DAB3_ERRORFLAG bit over the application duration, which corresponds to the time duration of the DAB3_W signal. The error flag information is calculated through a re-encoding and comparing process.

The read block transfer again delivers 32 bytes at the EFC port. From these 32 bytes, however, only 14 bytes contain real EFC information as shown in table 19. The EFC of one application channel is a 16-bit-wide sum which is valid for 24 ms after the falling edge of the corresponding DAB3 window signal. It can be used for a rough BER estimation.

Table 19. Port 4 configuration

Byte	Error Flag Count
0	Not used
1	Not used
2	Least significant byte EFC FIC
3	Most significant byte EFC FIC
4	Least significant byte EFC application channel 2
5	Most significant byte EFC application channel 2
6	Least significant byte EFC application channel 3
7	Most significant byte EFC application channel 3
8	Least significant byte EFC application channel 4

Byte	Error Flag Count
9	Most significant byte EFC application channel 4
10	Least significant byte EFC application channel 5
11	Most significant byte EFC application channel 5
12	Least significant byte EFC application channel 6
13	Most significant byte EFC application channel 6
14	Least significant byte EFC application channel 7
15	Most significant byte EFC application channel 7
16 – 31	Not used

L3 bus programming:

MSB address mode LSB

0	**1**	**1**	**0**	**0**	**1**	**1**	**0**
DAB			U2758M			read command	

MSB data mode LSB

S2	**S1**	**S0**	**P4**	**P3**	**P2**	**P1**	**P0**
IC_SEL			read port				

MSB address mode LSB

0	**1**	**1**	**0**	**0**	**1**	**0**	**0**
DAB			U2758M			read data	

MSB data mode LSB

EFC	**EFC**	**EFC**	**EFC**	**EFC**	**EFC**	**EFC**	**EFC**
MSB			byte 0				LSB

• • •

MSB data mode LSB

EFC	**EFC**	**EFC**	**EFC**	**EFC**	**EFC**	**EFC**	**EFC**
MSB			byte 31				LSB

32 bytes delivered by U2758M-B

4.5.7 DAB3 Interface Description

This section describes the data output interface between the U2758M-B and a source decoder to follow. It is a windowed 384-kHz interface with single data bit line and a single error flag line. For every selected application channel, a window signal is generated. Depending on the flag DAB3_WFORMAT, the window signals are binary or decimal coded. Furthermore, a multiplex reconfiguration mode can be performed. The output frame length of the data burst is 24 ms for all 3 DAB modes.

Table 20. DAB3 interface signal description

Signal Name	Description
DAB3_DATA	Serial output data carries the decoded data burst at 384 kHz.
DAB3_FLAG	Error flag signal, output reliability information which corresponds to the serial data DAB3_DATA signal. A ‘0’ indicates an error-free transmisson.
DAB3_CLK	Is a gated 384-kHz clock, output
DAB3_WFORMAT	Defines the window (DAB3_W) format, input 0 decimal-coded window format DAB3_W[1:7] single window line for every application channel 1 binary-coded window format DAB3_W[1] LSB, DAB3_W[2] , DAB3_W[3] MSB binary-coded window signals for the application channels
DAB3_W[1:7]	The active window signal defines the processed application channel, output DAB3_WFORMAT 0 1 (binary coded) DAB3_W[1] FIC bit 0 (LSB) DAB3_W[2] application channel 2 bit 1 DAB3_W[3] application channel 3 bit 2 (MSB) DAB3_W[4] application channel 4 0 DAB3_W[5] application channel 5 0 DAB3_W[6] application channel 6 0 DAB3_W[7] application channel 7 0
MRC_MODE	Multiplex reconfiguration mode, input 0 U2758M-B operation in parallel mode Up to 8 U2758M-B can be programmed separately with normal DAB3 output behavior. 1 multiplex reconfiguration mode With a pair of even and odd U2758M-B, a multiplex reconfiguration can be handled without mute state. DAB3 interface is tri-stated for the inactive U2758M–B. If a multiplex reconfiguration occurs, the signal MRC_TOGGLE exchanges the inactive and active U2758M.
MRC_TOGGLE	Multiplex reconfiguration toggle signal, input MRC_MODE = 1; 0 U2758M–B even (IC_SEL[0] low) is active and U2758M–B odd (IC_SEL[0] high) is inactive with a tri-stated DAB3 interface. 1 U2758M–B odd (IC_SEL[0] high) is active and U2758M–B even (IC_SEL[0] low) is inactive with a tri-stated DAB3 interface. MRC_MODE = 0 Do not care

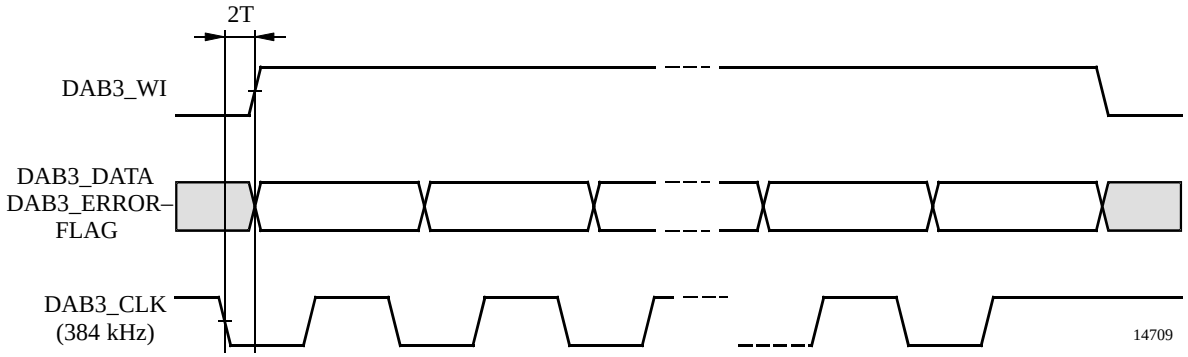


Figure 11. Timing DAB3 interface

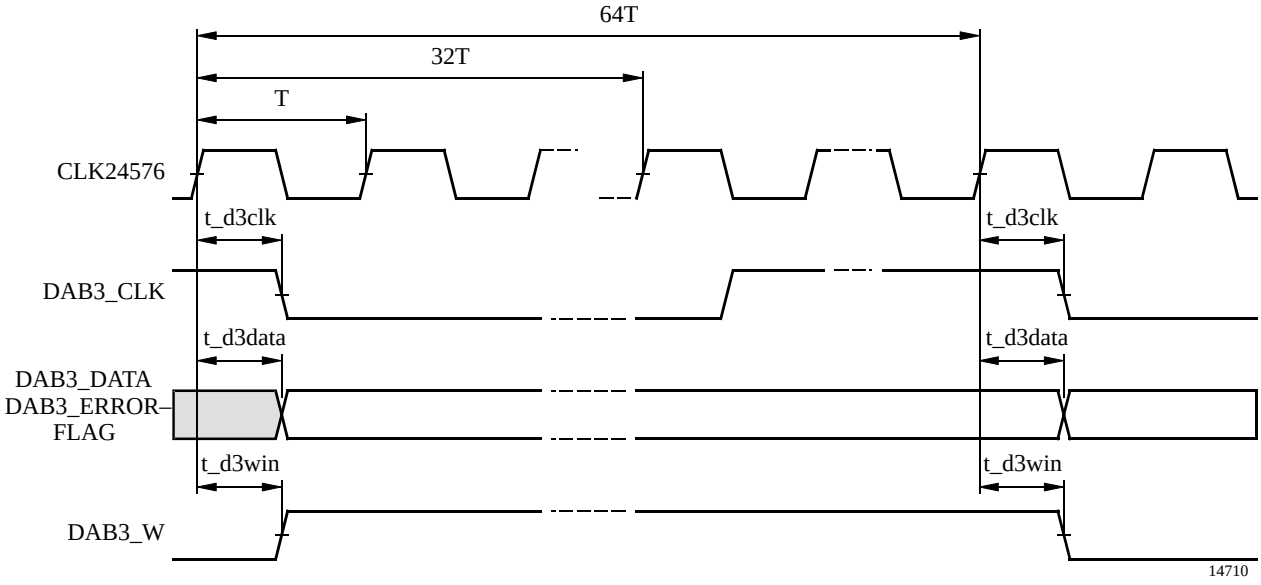


Figure 12. Detailed timing DAB3 interface

Table 21. DAB3 interface hold times

Parameters	Symbol	Min.	Typ.	Max.	Unit
Delay time of DAB3_CLK	t_{d3clk}	5	15	35	ns
Delay time of DAB3_DATA and DAB3_ERRORFLAG	t_{d3data}	5	15	35	ns
Delay time of DAB3_W	t_{d3win}	5	15	35	ns

Operation in Parallel Mode (MRC_MODE = 0)

The operation in parallel mode increases the maximum data rate of the channel decoder and can be used for a system with source decoder and data decoder. Every U2758M–B can be programmed freely and separately.

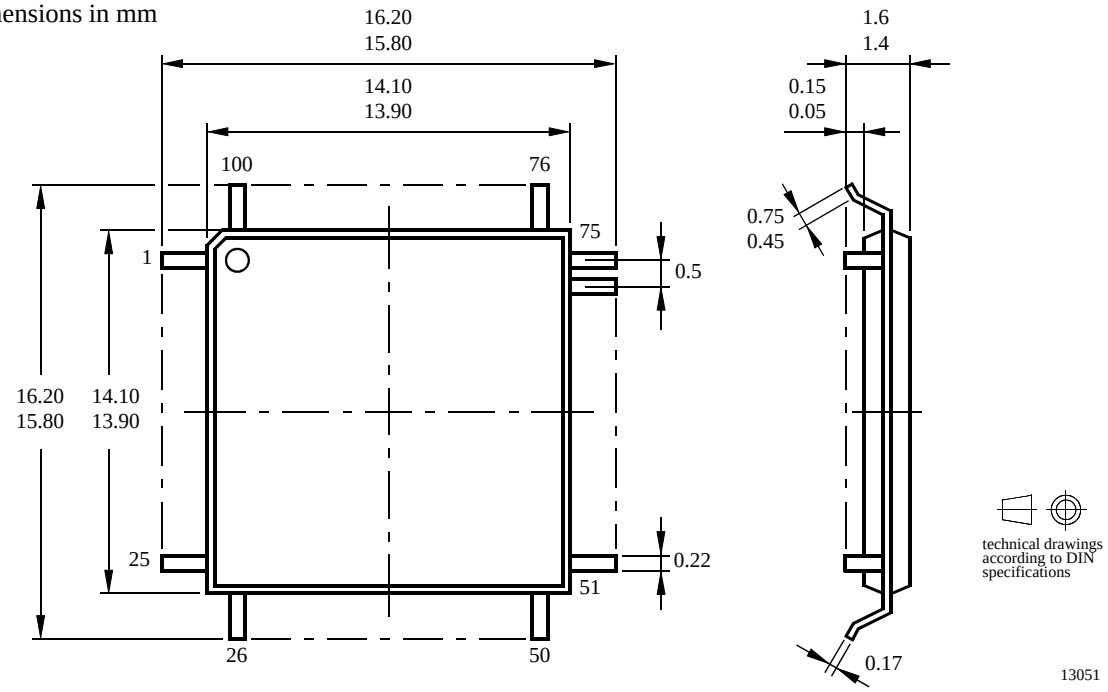
Multiplex Reconfiguration Mode (MRC_MODE = 1)

The U2758M-B offers the possibility handling a multiplex reconfiguration under certain circumstances without audio data loss. The limitation results from the different behavior of increasing and decreasing data rate of a sub-channel. In this mode the complete DAB3 interface can be set active or tri-stated with the MRC_TOGGLE signal as described in table 20.

5 Package Information

Package plastic TQFP 100

Dimensions in mm



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1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

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1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423