NEC
NEC Electronics Inc.

μPD23C2000
2,097,152-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C2000 is a 2,097,152-bit ROM fabricated with CMOS silicon-gate technology. The device is static in operation and can be organized as 131,072 words by 16 bits (word configuration) or as 262,144 words by 8 bits (byte configuration). In word configuration, pins $O_0 - O_{15}$ are active. In byte configuration, pin O_{15}/A_{-1} becomes the additional bit required to address 256K bytes.

The μPD23C2000 has three-state outputs, fully TTL-compatible inputs and outputs, and an output enable pin which is mask-programmable and can be specified as active low, active high, or don't care. The choice between word or byte configuration must also be specified for mask programming.

The μPD23C2000 is available in 40-pin plastic DIP or 52-pin plastic quad flatpack packaging.

Features

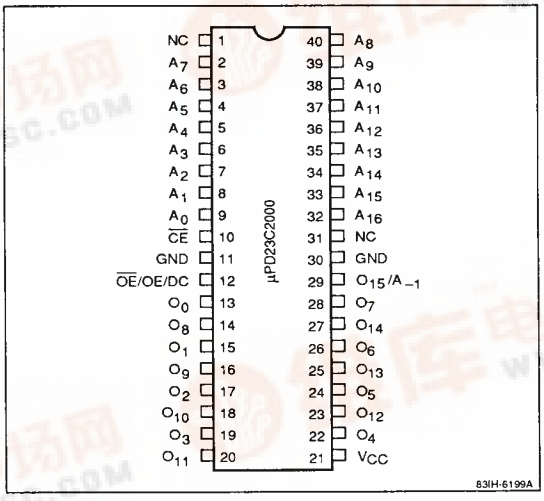
- Programmable organization
  - 131,072 words by 16 bits (word)
  - 262,144 words by 8 bits (byte)
- Fast access time of 250 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS technology
- Fully static operation
- Low power dissipation
  - 220 mW (active)
  - 550 μW (standby)
- 40-pin plastic DIP or 52-pin plastic QFP packaging

Ordering Information

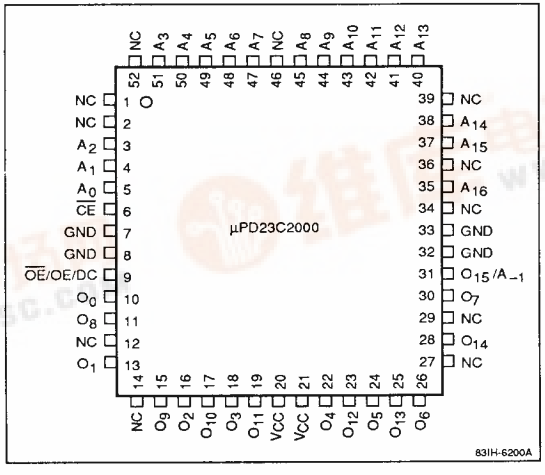
Part Number	Access Time (max)	Power Consumption (max) Active	Standby	Package
μPD23C2000C	250 ns	40 mA	100 μA	40-pin plastic DIP
μPD23C2000GC	250 ns	40 mA	100 μA	52-pin plastic QFP

Pin Configurations

40-Pin Plastic DIP



52-Pin Plastic Quad Flatpack



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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

Truth Table

$\overline{CE}$	OE	Function	Output	I_{CC}
V_{IH}	Don't Care	Not Selected	High-Z	Standby
V_{IL}	Inactive	Not Selected	High-Z	Active
V_{IL}	Active	Read	D_{OUT}	Active

Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
O_0 - O_{14}	Data outputs
O_{15}/A_{-1}	Output 15 (word)/LSB address (byte)
$\overline{CE}$	Chip enable
$\overline{OE}$/OE/DC	Output enable (Note 1)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

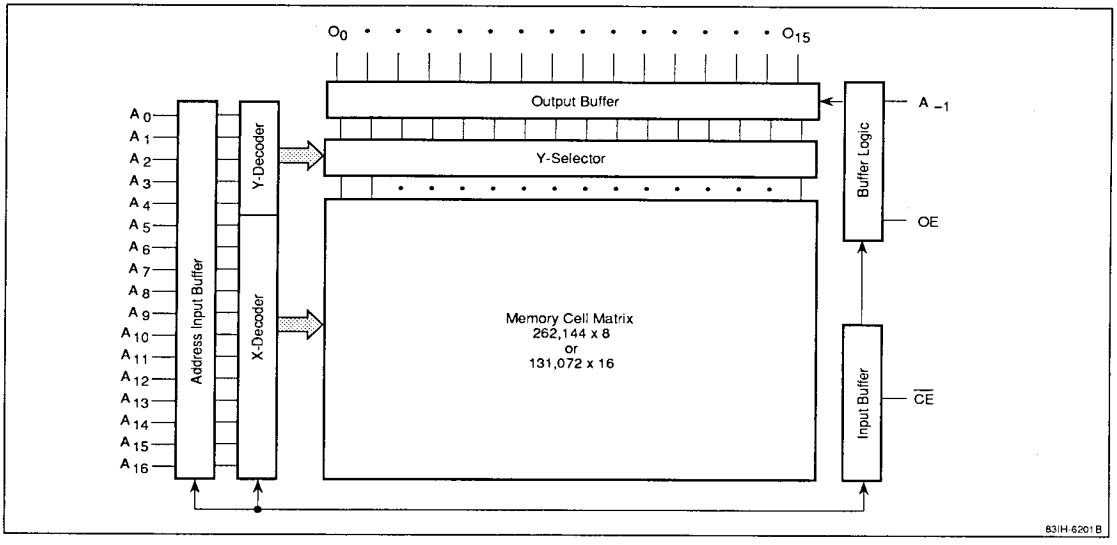
Notes:

(1) This pin is user-definable as active low, active high, or don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.5 mA
Input leakage current	I_{LI}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10		10	μA	V_O = 0 V to V_{CC}; chip deselected
Power supply current	I_{CC1}			40	mA	$\overline{CE}$ = V_{IL}
	I_{CC2}			1.5	mA	$\overline{CE}$ = V_{IH} (standby)
	I_{CC3}			100	μA	$\overline{CE}$ ≥ V_{CC} − 0.2 V (standby)

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			250	ns	
Chip enable access time	t_{CE}			250	ns	
Output enable access time	t_{OE}			110	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		70	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL + 100 pF.

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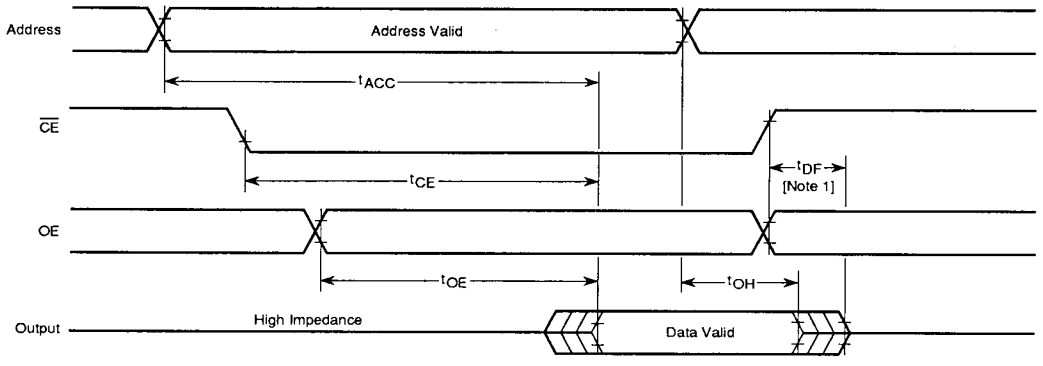
Timing Waveform



Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

[2] For byte operation, $O_8 - O_{14}$ are high impedance and O_{15}/A_{-1} is the least significant address input.

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